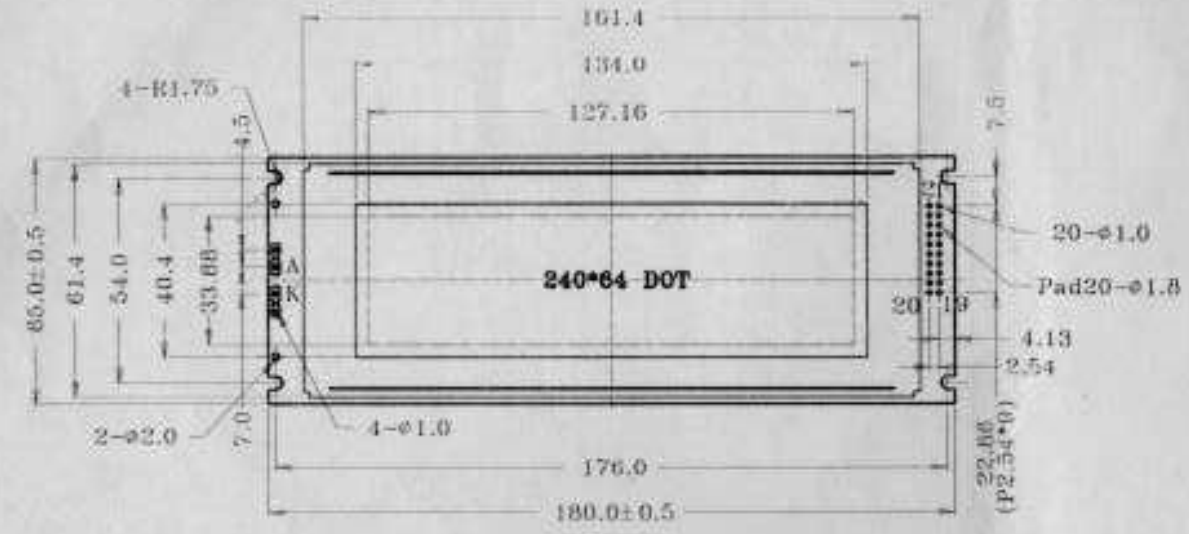
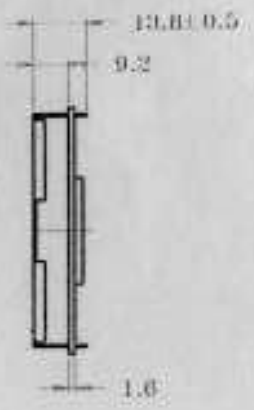
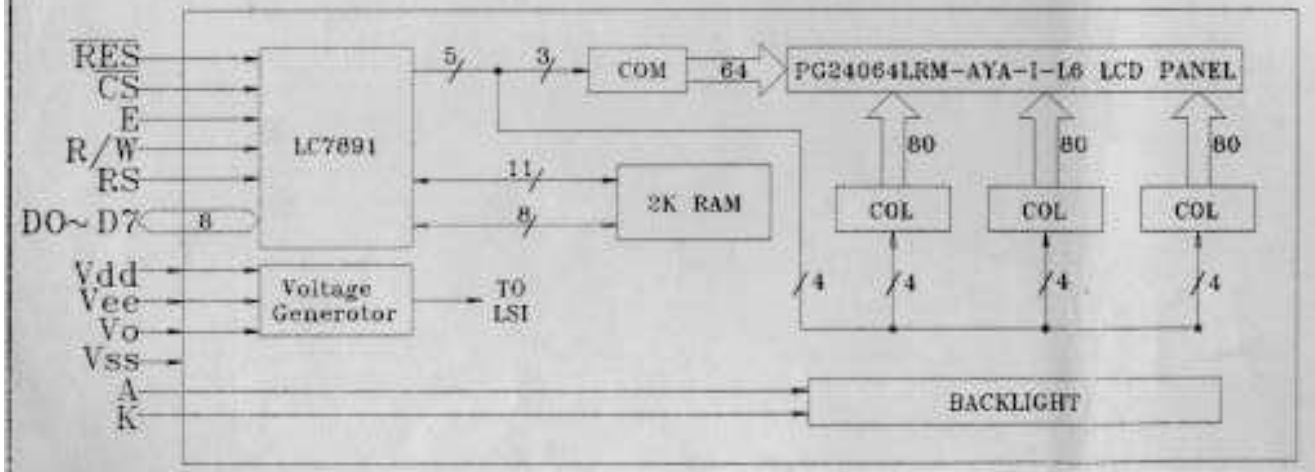
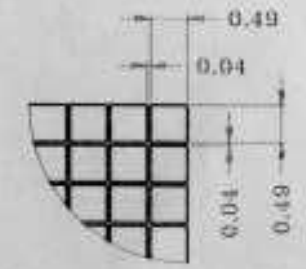




PIN NO.	SIGNAL
1	Vss
2	Vdd
3	Vo
4	RS
5	R/$\overline{W}$
6	E
7	DB0
8	DB1
9	DB2
10	DB3
11	DB4
12	DB5
13	DB6
14	DB7
15	$\overline{CS}$
16	$\overline{RES}$
17	Vee
18	N.C
19	A
20	K





The tolerance unless classified ±0.3mm

SCALE:10/1

POWERTIP TECHNOLOGY		
SCALE: 1/2		MODEL NAME: PG 24064LRM-AYA-I-L6
UNIT: mm		TITTLE: COUNTER DRAWING
EDI: 0	PAGE: 1/1	DRAWN NO.: PG-95003-017
APPROVED: 陳	CHECKER: 工程	DRAWN: 工程

Absolute Maximum Ratings/T_a=25°C, GND=0V

				unit
Maximum Supply Voltage	V_{DD} max		−0.3to+7.0	V
Input Voltage	V_I		−0.3toV_{DD}+0.3	V
Output Voltage	V_O		−0.3toV_{DD}+0.3	V
Allowable Power Dissipation	Pd max	Ta=75℃	200	mW
Operating Temperature	Topg		−20to+75	℃
Storage Temperature	Tstg		−55to+125	℃

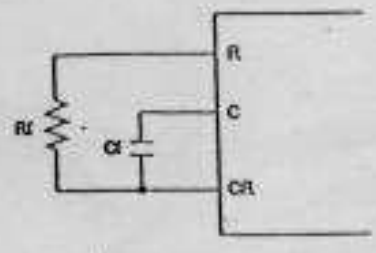
Allowable Operating Ranges/T_a=−20 to +75°C, GND=0V

			min	typ	max	unit
Supply Voltage	V_{DD}		4.75		5.25	V
Input "H"-Level Voltage	V_{IH1}	All input, I/O terminals except for $\overline{SYNC}$, CR	2.2		V_{DD}	V
Input "L"-Level Voltage	V_{IL1}	" "	0		0.8	V
Input "H"-Level Voltage	V_{IH2}	$\overline{SYNC}$, CR	0.7V_{DD}		V_{DD}	V
Input "L"-Level Voltage	V_{IL2}	$\overline{SYNC}$, CR	0		0.3V_{DD}	V
Output "H"-Level Voltage	V_{OH1}	I_{OH}=−0.6mA DB0to7, $\overline{WE}$, MA0to15, MD0to7	2.4		V_{DD}	V
Output "L"-Level Voltage	V_{OL1}	I_{OL}=1.6mA DB0to7, $\overline{WE}$, MA0to15, MD0to7	0		0.4	V
Output "H"-Level Voltage	V_{OH2}	I_{OH}=−0.6mA $\overline{SYNC}$, CPO, FLM, CL1, CL2, D1, D2, MA, MB	V_{DD}−0.4		V_{DD}	V
Output "L"-Level Voltage	V_{OL2}	I_{OL}=0.6mA $\overline{SYNC}$, CPO, FLM, CL1, CL2, D1, D2, MA, MB	0		0.4	V
Internal Clock Operation Clock OSC Frequency	fOSC	Cf=15pF±5%, Rf=39kΩ±2%, Note 1	500	600	700	kHz
External Clock Operation Clock Frequency	fCP	Note 2			2.5	MHz
Clock Duty	Duty	Note 3	47.5	50	52.5	%
Clock Rise Time	trcp	Note 3			50	ns
Clock Fall Time	tfcp	Note 3			50	ns

Electrical Characteristics/T_a=−20 to +75°C, GND=0V, V_{DD}=5V±5%

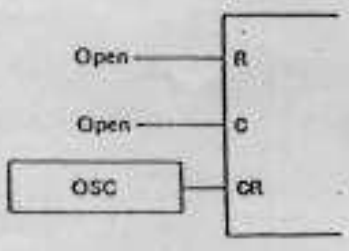
Input Leak Current	I_{IN}	V_{IN}=0 toV_{DD}, $\overline{CS}$, E, RS, R/$\overline{W}$, $\overline{RES}$	−5		5	μA
Current Dissipation	I_{CC1}	CR oscillation, fosc=600kHz		2	4	mA
Current Dissipation	I_{CC2}	External clock, fCP=2.5MHz		3	5	mA
Pull-up Current	I_{PL}	V_{IN}=GND, DB0to7, RD0to7, MD0to7		10	20	μA

(Note 1)

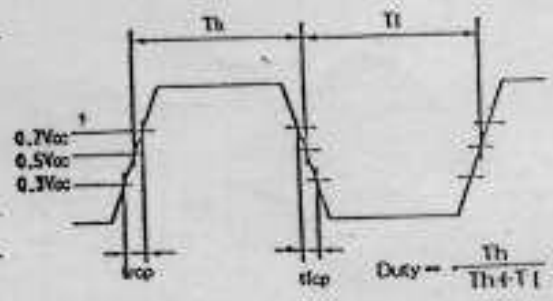


Cf=15pF±5%
Rf=39kΩ±2%
(at fOSC=600kHz typ.)

(Note 2)



(Note 3)



■ Description of Terminals

Symbol	Input/ Output	External Connection	Function
RS	Input	MPU	Register selext --- RS=1 --- instruction register RS=0 --- data register
R/W	Input	MPU	Read/write ---R/W=1 --- MPU← LC7981 R/W=0 --- MPU→ LC7981
E	Input	MPU	Enable --- Data is written on the negative transition of E. Data can be read while E=1.
DB0 | DB7	Input/ Output	MPU	Data bus --- Three-stste I/O common terminal , terminal for transmitting/ receiving data to/from the MPU.
$\overline{CS}$	Output	MPU .	Chip selsct --- Selection allowed when $\overline{CS}$=0
$\overline{RES}$	Input	MPU	Reset --- Setting RES to 0 selects display OFF, slave mode,and Hp=6.
VDD VSS		Power Supply	VDD: +5V VSS: GND
Vo		Power Supply	Contrast adjustment voltage
VEE		Power Supply	Negative voltage output (-10V)

FILENAME=B:\DATE1

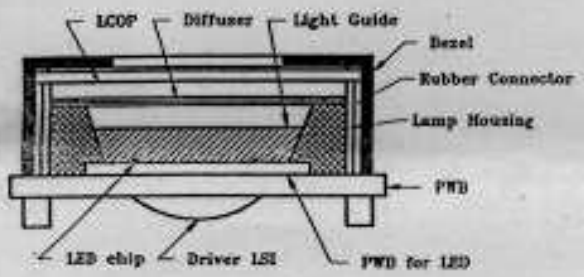
■ LED BACKLIGHT

Long life, low power consumption and simple power supply. Three different color of red, green and orange are available, or color can be changed alternatively.2 back light methods are available, beneath illumination and side illumination.

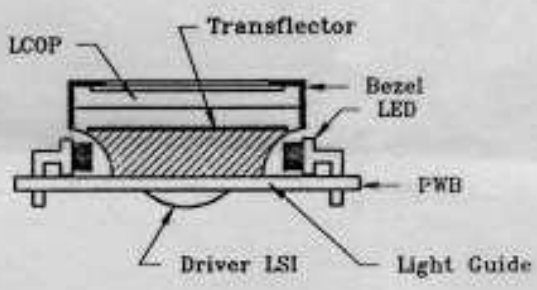
Features

- Low voltage deiving(DC) is available.
- Lovg life time 100,000 hours (average).
- No noise occurrence.
- Various color of red, green and orange etc. (multi-color by alternative switch is also available)
- Operating characteristics of PC-2002-A series is 4.2V, 210mA, 250 cd/㎡.

■ Beneath Illumination
Less quantity of chip even illumination.

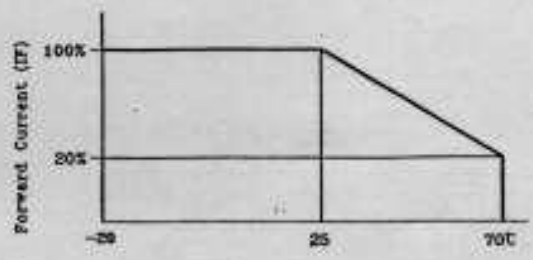


■ Side Illumination
Combination LED with light guide offers thin structure type of illumination.

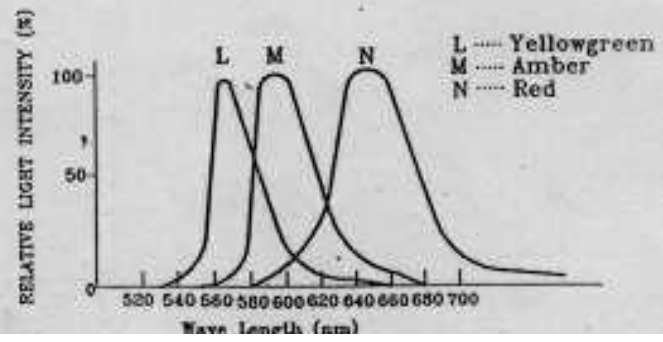


Electrical Characteristics
(Reference Date)

- Forward current Derating Curve

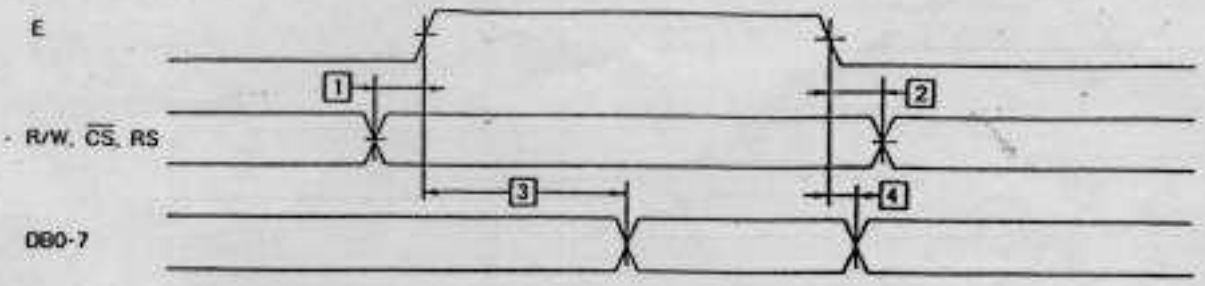


- Wave Length vs Relative Light Intensity

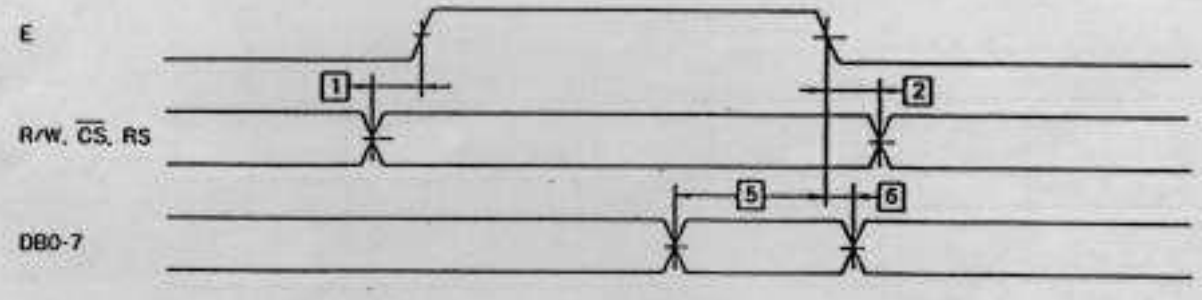


- Bus read/write operation 1

READ CYCLE



WRITE CYCLE



Ta=−20to+75℃, V_{DD}=5 V±5 %, GND=0 V

No	Item	Symbol	min	typ	max	unit	Conditions
1	Address set-up time	tAS	90			ns	
2	Address hold time	tAH	10			ns	
3	Data delay time (read)	tDDR			140	ns	C_L=50pF
4	Data hold time (read)	tDHR	10			ns	
5	Data set-up time (write)	tDSW	220			ns	
6	Data hold time (wirte)	tDHW	20			ns	

Note: Definition of the test waveform

The input terminals are driven at 2.4V and 0.45V. Timing is measured at 1.5V.

10) Writing display data

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction Reg	0	1	0	0	0	0	1	1	0	0
RAM	0	0	MSB (pattern data, character code)							LSB

Write code "0DH" in the instruction register. Then, write 8-bit data with RS=0, and the data is written into RAM as display data or character codes at the address specified by the cursor address counter. After writing, the count of the cursor address counter increments by 1.

11) Reading display data

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction Reg	0	1	0	0	0	0	1	1	0	1
RAM	1	0	MSB (pattern data, character code)							LSB

W "0CH" in the instruction register. Then, establish the read status with RS=0, and data in the RAM can be read. The procedure for reading data is as follows:

This instruction outputs the contents of the data output register to DB0 to 7, then transfers the RAM data indicated by the cursor address to the data output register. It then increments the cursor address by 1, which means that correct data cannot be read in the first read operation. The specified value is output in the second read operation. Accordingly, a dummy read operation must be performed once when reading data after setting the cursor address.

12) Bit clear

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction Reg	0	1	0	0	0	0	1	1	1	0
Bit clear	0	0	0	0	0	0	0	(NB−1) Binary		

1 Bit set

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction Reg	0	1	0	0	0	0	1	1	1	1
Bit set	0	0	0	0	0	0	0	(NB−1) Binary		

As the bit-clear or bit-set instruction, 1 bit of a 1 byte of data in display RAM is set to 0 or 1. The bit specified by NB is set to 0 for the bit-clear instruction and 1 for the bit-set instruction. The RAM address is specified by the cursor address, which is automatically incremented by 1 at the completion of the instruction. NB is a value in the range from 1 to 8. The LSB is indicated by NB=1, and the MSB by NB=8.

14) Reading the BUSY flag

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
busy flag	1	1	1 / 0	*						

2) Setting the character pitch

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction Reg	0	1	0	0	0	0	0	0	0	1
Character pitch Reg	0	0	(Vp − 1) Binary				0	(Hp − 1) Binary		

Vp is the number of vertical dots per character. Determine Vp with the pitch between two vertically placed characters taken into consideration. This value is meaningful only in the character display mode: it is invalid in the graphic mode.
In character mode, Hp indicates the number of horizontal dots per character, from the leftmost part of one character to the leftmost part of the next. In the graphic mode, Hp indicates how many bits (or dots) from RAM appear in a 1-byte display.
Hp must take one of the following three values.

Hp	DB2	DB1	DB0	
6	1	0	1	Horizontal character pitch 6
7	1	1	0	" 7
8	1	1	1	" 8

3) Setting the number of characters

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction Reg	0	1	0	0	0	0	0	0	1	0
Character number Reg	0	0	(HN − 1) Binary							

In the character display mode, H_N indicates the number of characters in the horizontal direction. In the graphic mode, it indicates the number of bytes in the horizontal direction. The total number of dots positioned horizontally on the screen n is given by the formula

$$n = Hp \times H_N.$$

Even numbers in the range 2 to 256 (decimal) can be set as H_N.

4) Setting the time division number (display duty)

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction Reg	0	1	0	0	0	0	0	0	1	1
Time division Reg	0	0	(Nx − 1) Binary							

Consequently, 1/Nx is the display duty.
Decimal numbers within the range 1 to 256 can be set as Nx.

5) Setting the cursor position

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction Reg	0	1	0	0	0	0	0	1	0	0
Cursor position Reg	0	0	0	0	0	0	(Cp − 1) Binary			

In the character display mode, Cp indicates the line at which the cursor is displayed. For example, when Cp=8 (decimal) is specified, the cursor is displayed beneath the character of the 5 x 7 dot-font. The horizontal length of the cursor equals Hp (the horizontal character pitch). Decimal values in the range 1 to 16 can be assigned to Cp. When the value is less than the vertical character pitch Vp (Cp ≦ Vp), display priority is given to the cursor (provided the cursor display is ON). The cursor is not displayed when CP > Vp. The horizontal length of the cursor equals Hp.

6) Setting the display start lower address

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction Reg	0	1	0	0	0	0	1	0	0	0
Display start address Reg (lower byte)	0	0	(start address lower byte) binary							

7) Setting the display start upper address

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction Reg	0	1	0	0	0	0	1	0	0	1
Display start address Reg (upper byte)	0	0	(start address upper byte) binary							

This instruction writes the display start address value in the display start address register. The display start address is the RAM address at which data to be displayed at the leftmost position of the top line of the screen is stored. The start address consists of 16 bits (upper and lower).

8) Setting the cursor (lower) address (RAM read/write lower address)

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction Reg	0	1	0	0	0	0	1	0	1	0
Cursor address counter (lower byte)	0	0	(cursor address lower byte) binary							

9) Setting the cursor (upper) address (RAM read/write upper address)

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction Reg	0	1	0	0	0	0	1	0	1	1
Cursor address counter (upper byte)	0	0	(cursor address upper byte) binary							

This instruction writes the cursor address value in the cursor address counter. The cursor address indicates the address for exchanging display data and character codes with RAM. In other words, data at the address specified by the cursor address is read from or written into RAM. In character display, the cursor is displayed at the position specified by the cursor address.

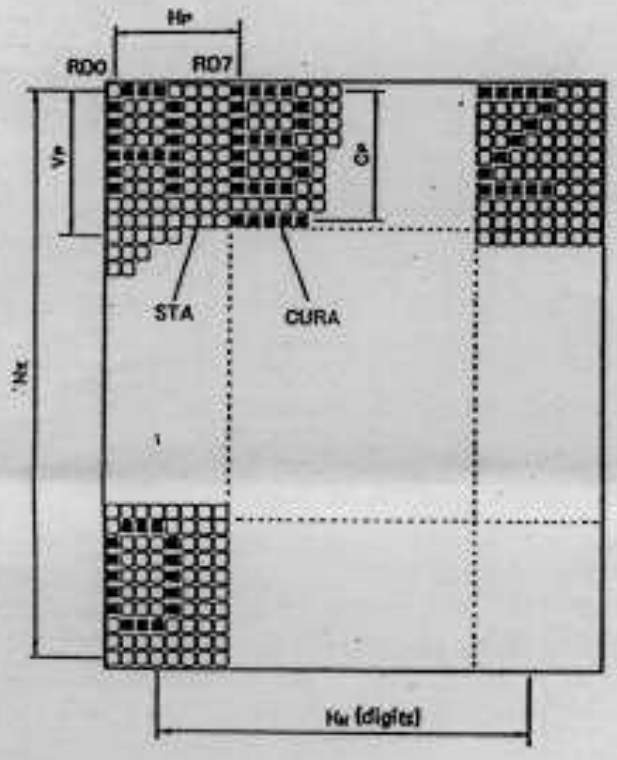
The cursor address is divided into a lower address (8 bits) and an upper address (8 bits). It should be set in accordance with the following rules.

1	To rewrite (set) both lower and upper addresses:	First set the lower address, then the upper.
2	To rewrite the lower address:	Always reset the upper address after setting the lower address.
3	To rewrite the upper address only:	Set the upper address. It is necessary to reset the lower address.

The cursor address counter is a 16-bit up-counter with set/reset functions: when the Nth bit goes from 1 to 0, the count of the (N + 1)th bit increments by one. Accordingly, when the lower address is set so that the lower MSB (8th bit) changes from 1 to 0, the LSB (1st bit) of the upper counter must increment by one. When setting the

The Busy flag is output to DB7 when read mode is established with RS=1. The Busy flag is set to 1 while any of the instructions 1) through 13) is being executed. It is set to 0 at the completion of the execution, allowing the next instruction to be accepted. No other instruction can be accepted when the Busy flag is 1. Accordingly, before writing an instruction and data, it is necessary to ensure that the Busy flag is 0. However, the next instruction can be executed without checking the Busy flag when the maximum read cycle time or the write cycle time has been exceeded after execution of the previous data read instruction or the data write instruction.
The Busy flag does not change when data is written into the instruction register (RS=1). Therefore, the Busy flag need not be checked immediately after writing data into the instruction register.
Specification of the instruction register is unnecessary to read the Busy flag.

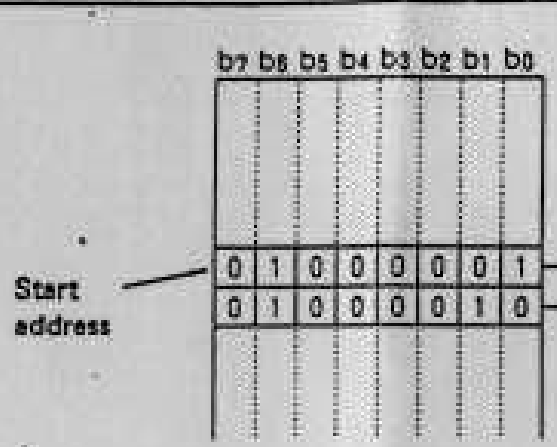
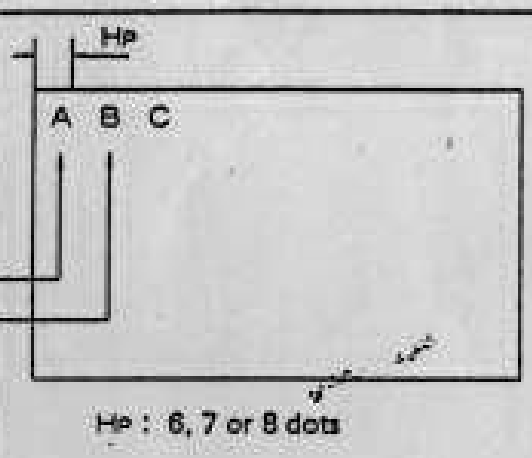
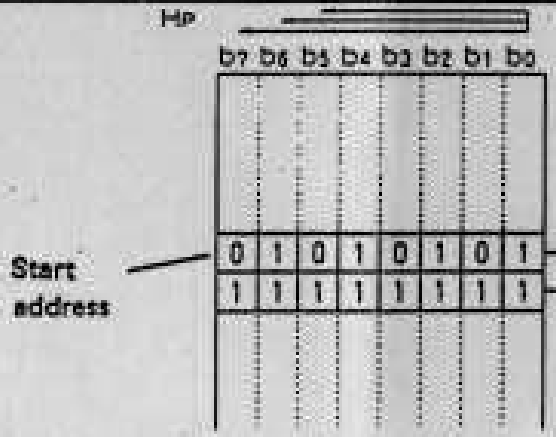
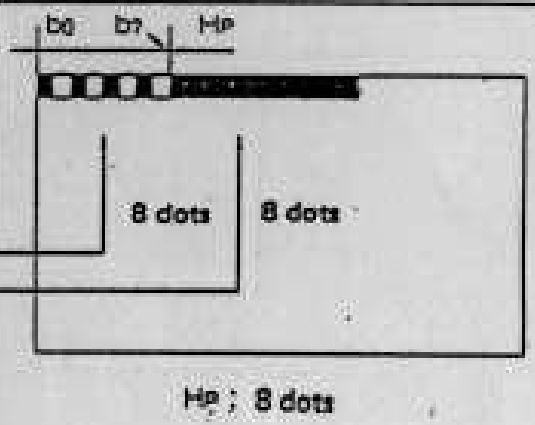
The relation between the LCD panel display and Hp, H_N, Vp, Cp, and Nx.



Symbol	Description	Contents	Value
Hp	Horizontal character pitch	Character pitch in the horizontal direction	6 to 8 dots
H_N	Number of characters in the horizontal direction	Number of characters (digits) per horizontal line or the number of words per line (graphic)	Even digits in the range 2 to 256
V_p	Vertical character pitch	Character pitch in the vertical direction	1 to 16 dots
Cp	Cursor position	The line number at which the cursor is to be displayed	1 to 16 lines
Nx	Number of lines in the vertical direction	Display duty	1 to 256 lines

Note)
When the number of vertical dots on the screen is m and that of horizontal dots is n,

1/m = 1/Nx = display duty
n = Hp x H_N
m/Vp = number of display lines
Cp≦Vp

Display mode	Display data from the MPU	RAM	LC Panel
Character display	Display pattern (8 bits)		
Graphic	Character code (8 bits)		

e Display control instruction

Display is controlled by writing data into the instruction register and 13 data registers. The instruction register and the data register are distinguished by the RS signal. First, write 4-bit data in the instruction register when RS=1, then specify the code of the data register. Next, with RS=0, write 8-bit data in the data register, which executes the specified instruction.

A new instruction cannot be accepted while an old instruction is being executed. As the Busy flag is set under this condition, write an instruction only after reading the Busy flag and making sure that it is 0.

However, the next instruction can be executed without checking the Busy flag when the maximum read cycle time or the write cycle time has been exceeded after execution of the previous data read instruction or the data write instruction. The Busy flag does not change when data is written into the instruction register (RS=1). Therefore, the Busy flag need not be checked immediately after writing data into the instruction register.

1) Mode control

Write code "00H" (in hexadecimal notation) in the instruction register and specify the mode control register.

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction Reg	0	1	0	0	0	0	0	0	0	0
Mode control Reg	0	0	0	0	MODE Data					

DB5	DB4	DB3	DB2	DB1	DB0	Cursor/blink	CG	Graphic/character display
1/0	1/0	0	0	0	0	Cursor OFF	Built-in CG	Character display
		0	1			Cursor ON		
		1	0			Cursor OFF character blink		
		1	1			Cursor blink		
		0	0		1	Cursor OFF	External CG	
		0	1			Cursor ON		
		1	0			Cursor OFF character blink		
		1	1			Cursor blink		
		0	0	1	0			Graphic mode
Display ON/OFF	Master/slave	Blink	Cursor	Mode	External/ builtin CG			

1 : master mode
0 : slave mode

1 : display ON
0 : display OFF