2.Features

Item	Specifications
Number of dots	97(W) * 32(H) DOTS
Duty	1 / 33
BIAS	1 / 6
Type	FSTN-Positive
Display mode	Transflective-Black & White
Viewing direction	6H
Input data	Parallel
Backlight	LED - Yellow Green

3.Mechanical specifications

Item	Specifications	Unit
Outline dimension	42.0(W) * 28.9(H) * 4.7 MAX(T)	mm
Viewing area	36.0(W) * 21.0(H)	mm
Active area	31.0(W) * 13.72(H)	mm
Dot size	0.28(W) * 0.39(H)	mm
Dot pitch	0.32(W) * 0.43(H)	mm

■ 4.Maximum rating

Item		Symbol	Min	Max	Unit	Note
Supply voltage	Logic	Vdd-Vss	2.4	6.0	V	—
	LCD drive	Vdd-Vee	4.5	16.0	V	—
Input voltage		Vi	-0.3	Vdd+0.3	V	—
Operating temperature		Topr	-20	70	℃	—
Storage temperature		Tstg	-30	80	℃	—
Humidity		Hd	—	90	%RH	1

Note:1.No dew to be found.

5. Driver IC SPEC. (EPSON SED1530)

PIN DESCRIPTION

Power Supply

Name	I/O	Description	Number of pins
V_{DD}	Supply	+5V power supply. Connect to microprocessor power supply pin V_{CC}.	2
V_{SS}	Supply	Ground	1
V1, V2 V3, V4 V5	Supply	LCD driver supply voltages. The voltage determined by LCD cell is impedance-converted by a resistive driver or an operational amplifier for application. Voltages should be the following relationship: $V_{DD} \geq V1 \geq V2 \geq V3 \geq V4 \geq V5$ When the master operating power supply is on, the following voltages are given to V1 to V4 by the on-board power supply. Voltage selection is performed by the Set LCD Bias command.	5

	SED1530	SED1531	SED1532
V1	1/5-V5 1/6-V5	1/6-V5 1/8-V5	1/6-V5 1/8-V5
V2	2/5-V5 2/6-V5	2/6-V5 2/8-V5	2/6-V5 2/8-V5
V3	3/5-V5 4/6-V5	4/6-V5 6/8-V5	4/6-V5 6/8-V5
V4	4/5-V5 5/6-V5	5/6-V5 7/8-V5	5/6-V5 7/8-V5

LCD Driver Supplies

Name	I/O	Description	Number of pins
CAP1+	O	DC/DC voltage converter capacitor 1 positive connection	1
CAP1-	O	DC/DC voltage converter capacitor 1 negative connection	1
CAP2+	O	DC/DC voltage converter capacitor 2 positive connection	1
CAP2-	O	DC/DC voltage converter capacitor 2 negative connection	1
CAP3-	O	DC/DC voltage converter capacitor 1 negative connection	1
V_{OUT}	O	DC/DC voltage converter output	1
VR	I	Voltage adjustment pin. Applies voltage between V_{DD} and V5 using a resistive divider.	1

Microprocessor Interface

Name	I/O	Description	Number of pins
D0 to D7 (SI) (SCL)	I/O	8-bit bi-directional data bus to be connected to the standard 8-bit or 16-bit microprocessor data bus. When the serial interface selects: D7: Serial data input (SI) D6: Serial clock input (SCL)	8
A0	I	Control/display data flag input. It is connected to the LSB of microprocessor address bus. When low, the data on D0 to D7 is control data. When high, the data on D0 to D7 is display data.	1
RES		When RES is caused to go low, initialization is executed. A reset operation is performed at the RES signal level.	1
CS1 CS2	I	Chip select input. Data input/output is enabled when -CS1 is low and CS2 is high. When chip select is non-active, D0 to D7 will be "Hi-Z".	2
RD (E)	I	· When interfacing to an 8080 series microprocessor: Active low. This input connects the RD signal of the 8080 series microprocessor. While this signal is low, the SED1530 series data bus output is enabled. · When interfacing to a 6800 series microprocessor: Active high. This is used as an enable clock input pin of the 6800 series microprocessor.	1

■ Driver IC SPEC.(EPPSON SED1530) countine.

Name	I/O	Description	Number of pins
WR (R/W)	I	- Write enable input. When interfacing to an 8080-series microprocessor, WR is active low. - When interfacing to an 6800-series microprocessor, it will be read mode when R/W is high and it will be write mode when R/W is low. R/W = "1":Read R/W = "0":Write	1
C86	I	Microprocessor interface select terminal. C86 = high: 6800 series microprocessor interface C86 = low: 8080 series microprocessor interface	1
P/S	I	Serial data input/parallel data input select pin.	1

P/S	Chip select	Data/command	Data	Read/write	Serial clock
"H"	CS1, CS2	A0	D0–D7	RD, WR	—
"L"	CS1, CS2	A0	SI(D7)	Write only	SCL(D6)

* In serial mode, no data can be read from RAM.
When P/S = low, D0 to D5 are HZ and RD and WR must be fixed high or low.

LCD Driver Outputs

Name	I/O	Description	Number of pins
M/S	I	SED1530 series master/slave mode select input. When a necessary signal is output to the LCD, the master operation is synchronized with the LCD system, while when a necessary signal is input to the LCD, the slave operation is synchronized with the LCD system. M/S = high: Master operation M/S = low : Slave operation The following is provided depending on the M/S status.	1

Model	Status	OSC circuit	Power supply circuit	CL	FR	DYO	FRS	DOF
SED1530*0*	Master	Enabled	Enabled	Output	Output	Output	Output	Output
	Slave	Disabled	Disabled	Input	Input	HZ	HZ	Input

CL	I/O	Display clock input/output. When the SED1530 series selects master/slave mode, each CL pin is connected. When it is used in combination with the common driver, this input/output is connected to common driver YSCL pin. M/S = high: Output M/S = low: Input	1
FR	I/O	LCD AC signal input/output. When the SED1530 series selects master/slave mode, each FR pin is connected. When the SED1530 series selects master mode this input/output is connected to the common driver FR pin. M/S = high: Output M/S = low: Input	1
DYO	I/O	Common drive signal output. This output is enabled for only at master operation and connects to the common driver DIO pin. It becomes HZ at slave operation.	1
VS1	O	Internal power supply voltage monitor output.	1
DOF	I/O	LCD blanking control input/output. When the SED1530 series selects master/slave mode, the respective DOF pin is connected. When it is used in combination with the common driver (SED1635), this output/input is connected to the common driver DOFF pin. M/S = high: Output M/S = low: Input	1
FRS	O	Static drive output. This is enabled only at master operation and used together with the FR pin. This output becomes HZ at slave operation.	1

Driver IC SPEC.(EPPSON SED1530) countine.

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th><th>Number of pins</th></tr>
<tr><td>On
(SEG n)
(Com n)</td><td>O</td><td>LCD drive output. The following assignment is made depending on the model.
<table>
<tr><td></td><td>SEG</td><td>COM</td></tr>
<tr><td>SED1530Dx</td><td>O0–O99</td><td>O100–O131</td></tr>
<tr><td>SED1530Dx</td><td>O16–O115</td><td>O0–O15, O116–O131</td></tr>
<tr><td>SED1531Dx</td><td>O0–O131</td><td></td></tr>
<tr><td>SED1532Dx</td><td>O0–O99</td><td>O100–O131</td></tr>
<tr><td>SED1532Dx</td><td>O32–O131</td><td>O0–O31</td></tr>
</table>
SEG output. LCD segment drive output. One of VDD, V2, V3 and V5 levels is selected by combination of the contents of display RAM and FR signal.
<table>
<tr><td rowspan="2">RAM data</td><td rowspan="2">FR</td><td colspan="2">On output voltage</td></tr>
<tr><td>Normal display</td><td>Reverse display</td></tr>
<tr><td rowspan="2">H</td><td>H</td><td>V_{DD}</td><td>V2</td></tr>
<tr><td>L</td><td>V5</td><td>V3</td></tr>
<tr><td rowspan="2">0</td><td>H</td><td>V2</td><td>V_{DD}</td></tr>
<tr><td>L</td><td>V3</td><td>V5</td></tr>
<tr><td>Power save</td><td>–</td><td colspan="2">V_{DD}</td></tr>
</table>
COM output. LCD common drive output. One of VDD, V1, V4 and V5 levels is selected by combination of scan data and FR signal.
<table>
<tr><td>Scan data</td><td>FR</td><td>On output voltage</td></tr>
<tr><td rowspan="2">H</td><td>H</td><td>V5</td></tr>
<tr><td>L</td><td>V_{DD}</td></tr>
<tr><td rowspan="2">L</td><td>H</td><td>V1</td></tr>
<tr><td>L</td><td>V4</td></tr>
<tr><td>Power save</td><td>–</td><td>V_{DD}</td></tr>
</table></td><td></td></tr>
<tr><td>COMS</td><td>O</td><td>Indicator COM output. When it is not used, it is made open. This output is enabled only in the SED1530 and SED1532. When SED1531 is used, it becomes HZ. When multiple SED1530S or SED1532S are used, the same COMS signal is output to both master and slave units.</td><td>1</td></tr>
<tr><td></td><td></td><td>Total</td><td>172</td></tr>
</table>

FUNCTIONAL DESCRIPTION

Microprocessor Interface

Interface type selection

The SED1530 series can transfer data via 8-bit bi-directional data buses (D7 to D0) or via serial data input (SI). When high or low is selected for the polarity of PIS pin, either 8-bit parallel data input or serial data input can be selected as shown in Table 1. When serial data input is selected, RAM data cannot be read out.

Table 1

PIS	Type	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	C86	D7	D6	D0–D5
H	Parallel input	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	C86	D7	D6	D0–D5
L	Serial input	$\overline{CS1}$	CS2	A0	–	–	–	SI	SCL	(HZ)

"–" must always be high or low.

Parallel input

When the SED1530 series selects parallel input (PIS = high), the 8080 series microprocessor or 6800 series microprocessor can be selected by causing the C86 pin to go high or low as shown in Table 2.

Table 2

C86	Type	$\overline{CS1}$	CS2	A0	$\overline{RD}$	WR	D0 –D7
H	6800 micro-processor bus	$\overline{CS1}$	CS2	A0	E	R/W	D0–D7
L	8080 micro-processor bus	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	D0–D7

Data Bus Signals

The SED1530 series identifies the data bus signal according to A0, E, R/W, ($\overline{RD}$, $\overline{WR}$) signals.

Table 3

Common	6800 processor	8080 processor		Function
A0	(R/W)	$\overline{RD}$	$\overline{WR}$	
1	1	0	1	Reads display data.
1	0	1	0	Writes display data.
0	1	0	1	Reads status.
0	0	1	0	Writes control data in internal register. (Command)

Serial Interface (PIS is low)

The serial interface consists of an 8-bit shift register and a 3-bit counter. The serial data input and serial clock input are enabled when $\overline{CS1}$ is low and CS2 is high (in chip select status). When chip is not selected, the shift register and counter are reset.

Serial data of D7, D6, ..., D0 is read at D7 in this sequence when serial clock (SCL) goes high. They are converted into 8-bit parallel data and processed on rising edge of every eighth serial clock signal.

The serial data input (SI) is determined to be the display data when A0 is high, and it is control data when A0 is low. A0 is read on rising edge of every eighth clock signal.

Figure 1 shows a timing chart of serial interface signals. The serial clock signal must be terminated correctly against termination reflection and ambient noise. Operation checkout on the actual machine is recommended.

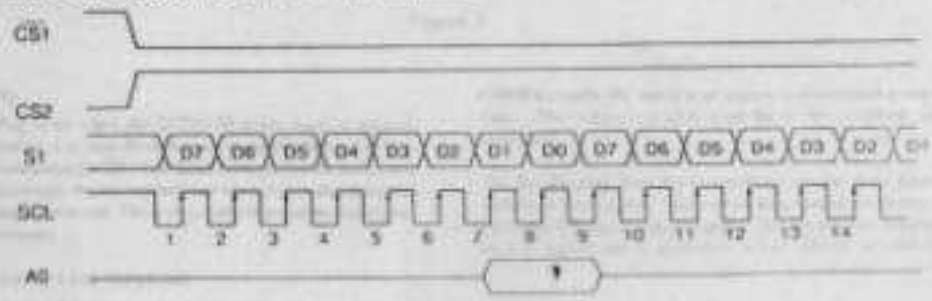


Figure 1

Column Address Counter

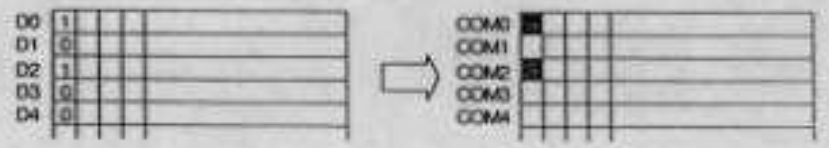
This is a 8 bit presettable counter that provides column address to the display RAM (refer to Figure 4). It is incremented by 1 when a Read/Write command is entered. However, the counter is not incremented but locked if a non-existing address above 84H is specified. It is unlocked when a column address is set again. The Column Address counter is independent of Page Address register.
When ADC Select command is issued to display inverse display, the column address decoder inverts the relationship between RAM column address and display segment output.

Page Address Register

This is a 4-bit page address register that provides page address to the display RAM (refer to Figure 4). The microprocessor issues Set Page Address command to change the page and access to another page. Page address 8 (D3 is high, but D2, D1 and D0 are low) is RAM area dedicate to the indicator, and display data D0 is only valid.

Display Data RAM

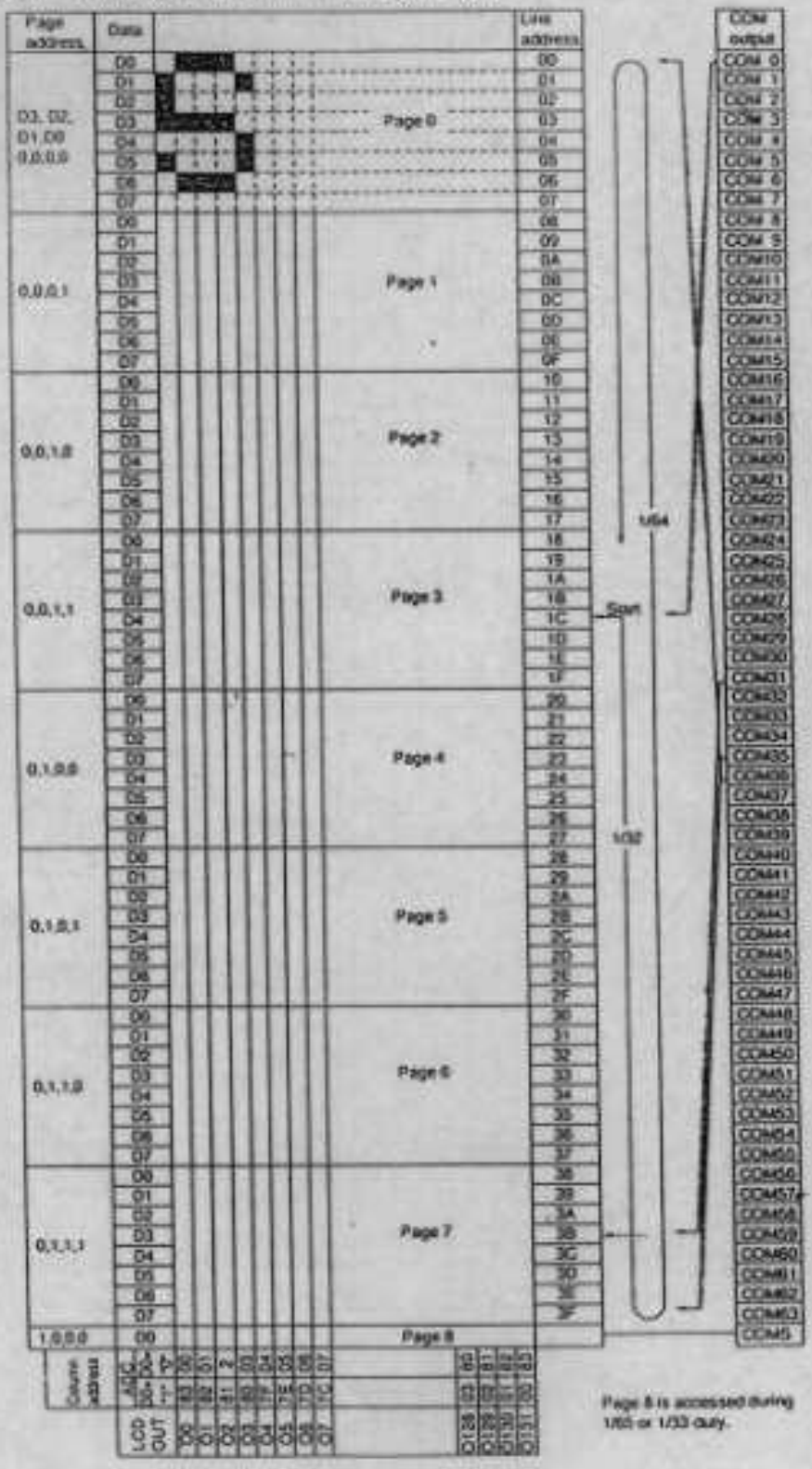
The display data RAM stores pixel data for LCD. It is a 65-column by 132-row (8-page by 8 bit+1) addressable array. Each pixel can be selected when page and column addresses are specified.
The time required to transfer data is very short because the microprocessor enters D0 to D7 corresponding to LCD common lines as shown in Figure 3. Therefore, multiple SED1530's can easily configure a large display having the high flexibility with very few data transmission restriction.
The microprocessor writes and reads data to/from the RAM through I/O buffer. As LCD controller operates independently, data can be written into RAM at the same time as data is being displayed, without causing the LCD to flicker.



Display data RAM　　Display on LCD

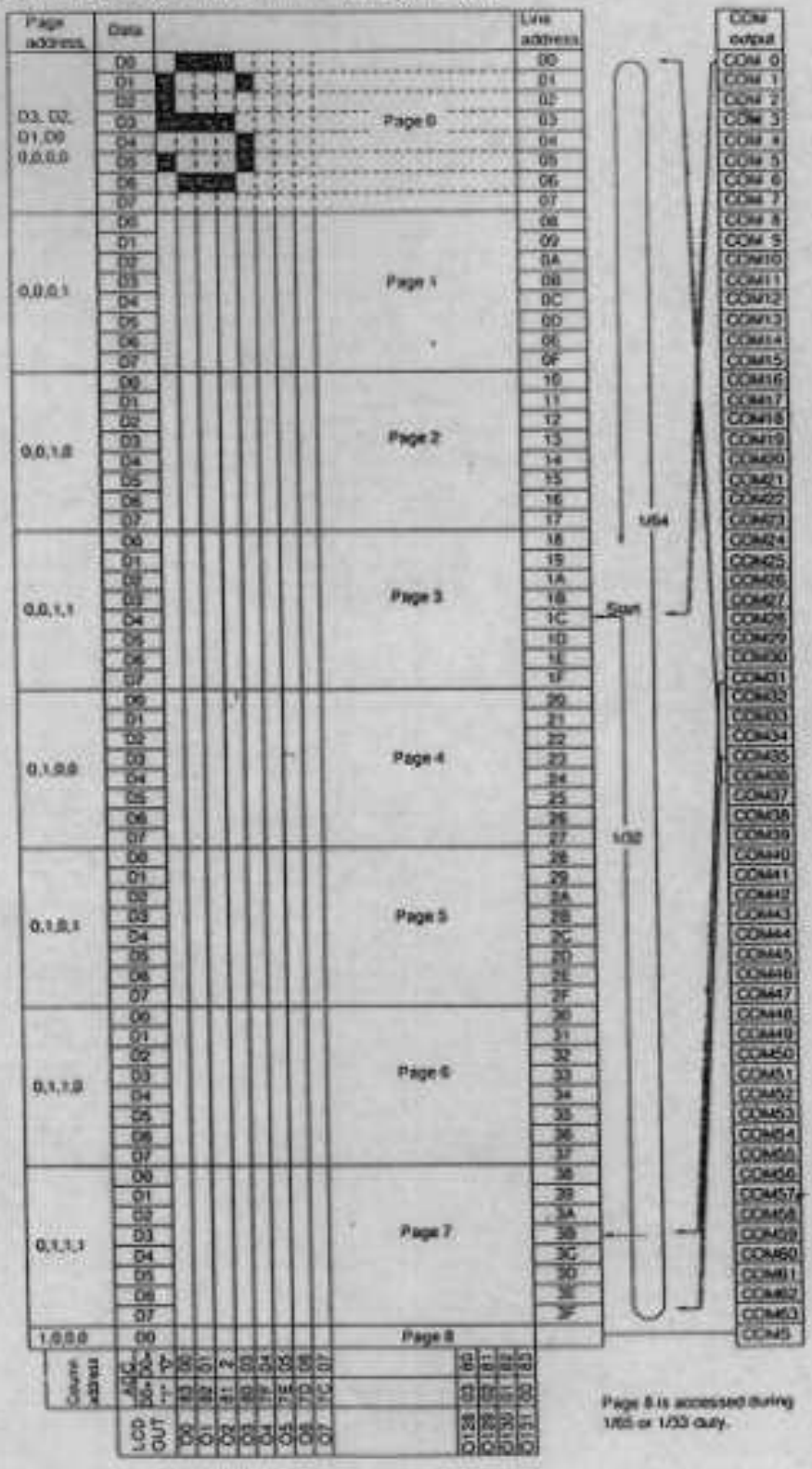
Driver IC SPEC.(EPPSON SED1530) countine.

Relationship between display data RAM and addresses (if initial display line is 1CH):



Driver IC SPEC.(EPPSON SED1530) countine.

Relationship between display data RAM and addresses (if initial display line is 1CH):



Output Status Selector Circuit

The SED1530 series except SED1531 can set a COM output scan direction to reduce restrictions at LCD module assembly. This scan direction is set by setting "1" or "0" in the output status register D3.

Fig. 5 shows the status.

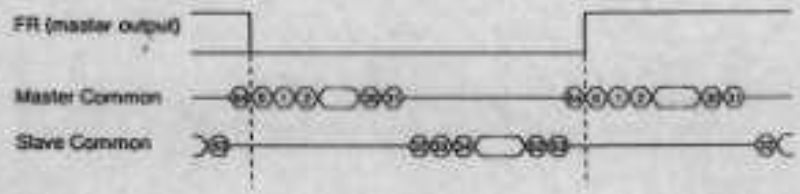
LCD output		O0		O131
ADC (D0)	"0"	0 (H) →	Column address	→ 83 (H)
	"1"	83 (H) ←		← 0 (H)

Display data RAM

	D3			
SED1530Dxx	0	SEG100		COM0 ---------- COM31
SED1530Dxx	1	SEG100		COM31 ---------- COM0
SED1530Dxx	0	COM15 -- 0	SEG100	COM16 -- 31
SED1530Dxx	1	COM16 -- 31	SEG100	COM15 -- 0
SED1531Dxx	–	SEG132		
SED1532Dxx	0	SEG100		COM0 ---------- COM31
SED1532Dxx	1	SEG100		COM31 ---------- COM0
SED1532Dxx	0	COM31 ---------- 0	SEG100	
SED1532Dxx	1	COM0 ---------- 31	SEG100	

The COM5 pin is assigned to COM32 on SED1530 and it is assigned to COM64 on SED1532 independent from their output status.

Figure 5 shows the COM output pin numbers of SED1532D0* and SED1532D8* in the master mode. In the slave mode, COM0 to COM31 must be replaced by COM32 to COM63.



Display Timing Generator Circuit

This section explains how the display timing generator circuit operates.

Signal generation to line counter and display data latch circuit

The display clock (CL) generates a clock to the line counter and a latch signal to the display data latch circuit.
The line address of the display RAM is generated in synchronization with the display clock. 132-bit display data is latched by the display data latch circuit in synchronization with the display clock and output to the segment LCD drive output pin.
The display data is read to the LCD drive circuit completely independent of access to the display data RAM from the microprocessor.

LCD AC signal (FR) generation

The display clock generates an LCD AC signal (FR). The FR causes the LCD drive circuit to generate a AC drive waveform.
It generates a 2-frame AC drive waveform.

When the SED1530 is operated in slave mode on the assumption of multi-chip, the FR pin and CL pin become input pins.

Common timing signal generation

The display clock generates an internal common timing signal and a start signal (DYO) to the common driver. A display clock resulting from frequency division of an oscillation clock is output from the CL pin.
When an AC signal (FR) is switched, a high pulse is output at a DYO output at the training edge of the previous display clock.
Refer to Fig. 6. The DYO output is output only in master mode.
When the SED1530 series is used for multi-chip, the slave requires to receive the FR, CL, DOF signals from the master.
Table 4 shows the FR, CL, DYO and DOF states.

Table 4

Model	Operation mode	FR	CL	DYO	DOF
SED153*D0*	Master	Output	Output	Output	Output
	Slave	Input	Input	Hz	Input

HZ denotes a high-impedance status.

Example of SED1530D0B 1/33 duty
•. Dual-frame AC driver waveforms

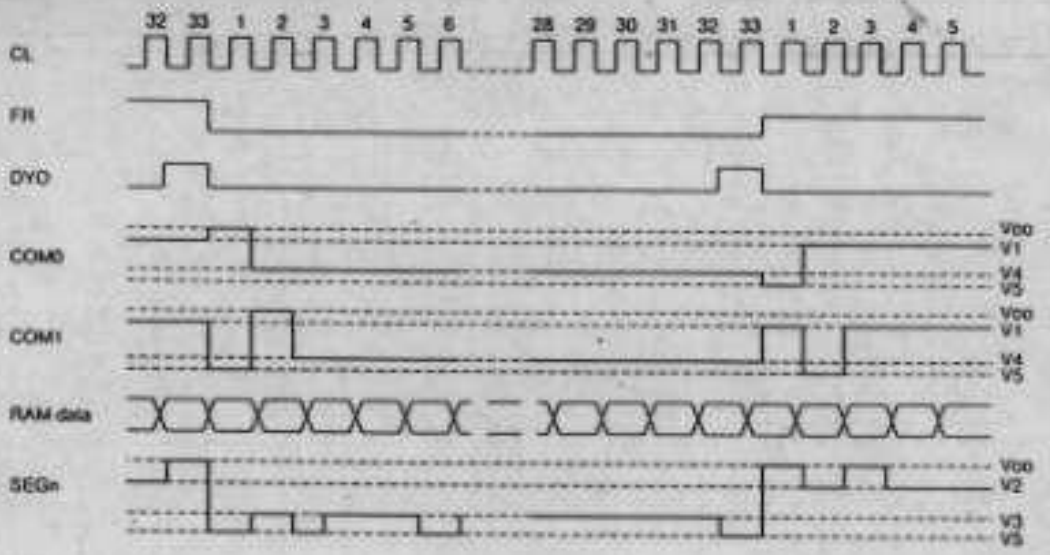


Fig. 6

Display Data Latch Circuit.

This circuit temporarily stores (or latches) display data (during a single common signal period) when it is output from display RAM to LCD panel driver circuit. This latch is controlled by Display in normal/in reverse Display ON/OFF and Static All-display on commands. These commands do not alter the data.

LCD Driver

This is a multiplexer circuit consisting of 133 segment outputs to generate four-level LCD panel drive signals. The LCD panel drive voltage is generated by a specific combination of display data, COM scan signal, and FR signal. Figure 8 gives an example of SEG and COM output waveforms.

Oscillator Circuit

This is an oscillator having a complete built-in type CR, and its output is used as the display timing signal source or as the clock for voltage booster circuit of the LCD power supply.
The oscillator circuit is available in master mode only.
The oscillator signal is divided and output as display clock at CL pin.

Power Supply Circuit

The power supply circuit generates voltage to drive the LCD panel at low power consumption, and is available in SED1530 master mode only. The power supply circuit consists of a quadruple booster circuit, voltage regulator, and LCD drive voltage follower.
The power supply circuit built in the SED1530 series is set for a small-scale LCD panel and is inappropriate to a large-pixel panel and a large-display-capacity LCD panel using multiple chips. As the large LCD panel has the dropped display quality due to a large load capacity, it must use an external power source.
The power circuit is controlled by Set Power Control command. This command sets a three-bit data in Power Control register to select one of eight power circuit functions. The external power supply and part of internal power circuit functions can be used simultaneously. The following explains how the Set Power Control command works.

[Control by Set Power Control command]

D2 turns on when triple booster control bit goes high, and D2 turns off when this bit goes low.

D1 turns on when voltage regulator control bit goes high, and D1 turns off when this bit goes low.

D0 turns on when voltage follower control bit goes high, and D0 turns off when this bit goes low.

[Practical combination examples]
Status 1: To use only the internal power supply.
Status 2: To use only the voltage regulator and voltage follower.
Status 3: To use only the voltage follower.
Status 4: To use only an external power supply because the internal power supply does not operate.

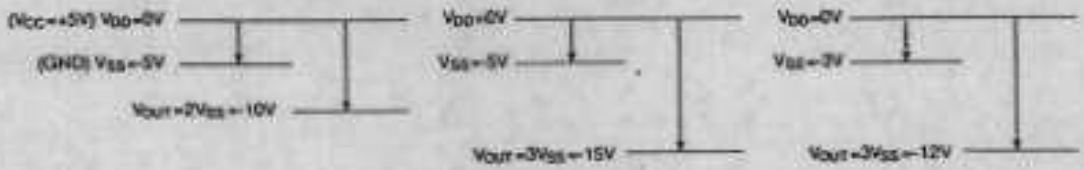
* The voltage booster terminals are CAP1+, CAP1-, CAP3+, CAP2- and CAP3-.
* Combinations other than those shown in the above table are possible but impractical.

	D2 D1 D0	Voltage booster	Voltage regulator	Voltage follower	External voltage input	Voltage booster terminal	Voltage regulator terminal
①	1 1 1	ON	ON	ON	—	Used	Used
②	0 1 1	OFF	ON	ON	V_{OUT}	OPEN	Used
③	0 0 1	OFF	OFF	ON	V5	OPEN	OPEN
④	0 0 0	OFF	OFF	OFF	V1 to V5	OPEN	OPEN

Booster circuit

If capacitors C1 are inserted between CAP1+ and CAP1-, between CAP2+ and CAP2-, CAP1+ and CAP3- and VSS and VOUT, the potential between VDD and VSS is boosted to quadruple toward the negative side and it is output at VOUT.
For triple boosting, remove only capacitor C1 between CAP+1 and CAP3- from the connection of quadruple boosting operation and jumper between CAP3- and VOUT. The triple boosted voltage appears at VOUT (CAP3-).

For double boosting, remove only capacitor C1 between CAP2+ and CAP2- from the connection of triple boosting operation, open CAP+3 and jumper between CAP2- and VOUT (CAP3-). The double boosted voltage appears at VOUT (CAP3-, CAP2-).
For quadruple boosting, set a VSS voltage range so that the voltage at VOUT may not exceed the absolute maximum rating.
As the booster circuit uses signals from the oscillator circuit, the oscillator circuit must operate.
Subsection 10.1.1 gives an external wiring example to use master and slave chips when on-board power supply is active.

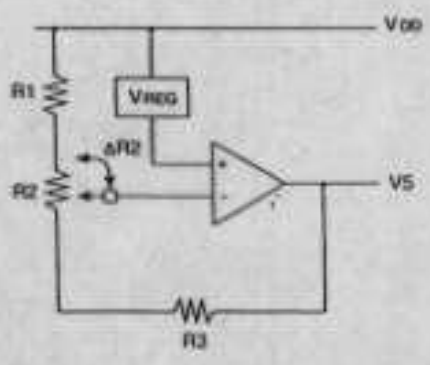


Potential during double boosting　　Potential during triple boosting　　Potential during quadruple boosting

Voltage regulator circuit

The boosted voltage at V_{OUT} is passed through voltage regulator circuit and V5 LCD drive voltage is output for LCD panel. This power is obtained by adjusting registers Ra and Rb within |V5|<|V_{OUT}| as follows:

$$V5=\left(1+\frac{R1+R2-\Delta R2}{R1+\Delta R2}\right) V_{REG} \cdots ①$$



V_{REG} is the internal constant voltage source of the IC, and it is fixed to V_{REG} =-2.5 V (if V_{DD} =0 V).

To adjust the V5 output voltage, insert a VR variable resistor between V_{DD} and V5 (Figure 7). For voltage fine-adjustment, a combination of R1 and R3 fixed resistors and R2 variable resistor is recommended to use.

R1, R2 and R3 setup example:
(Determined depending on the current flowing between VDD and V5)
R1 + R2 + R3 = 5M (Ω) ..... ②

Variable voltage range by R2: V5=-6 to -10 V
(Determined depending on the LCD characteristics)

If ΔR2=0 Ω and V REG=-2.5 V,
the following is obtained from equation (1) to set V5=-10 V.
R2 + R3 = 3 × R1 ..... ③

If ΔR2=R2 and V REG=-2.5 V,
the following is obtained from equation (1) to set V5=-6 V.
1.4 × (R1 + R2) = R3 ..... ③'

The following are determined from equations (2), (3) and (4):
R1= 1.25MΩ
R2= 0.83MΩ
R3= 2.92MΩ

The voltage regulator circuit has the temperature gradient of approximately -0.2%/oC for V REG output. To get another temperature gradient, use an electronic control for software change by MPU.

As the VR terminal has a high input impedance, an elimination of noise occurring at jumpers and shield lines is required.

Voltage regulator circuit using the electronic control function

The electronic control function can control the V5 LCD drive voltage using commands and adjust the LCD brightness.
The electronic control sets 5-bit data in the electronic control register, and the V5 LCD voltage can be set to one of up to 32 different voltages.
During electronic control, at least the voltage regulator circuit and voltage follower circuit must be activated by the Power Control Set command.
If the voltage booster circuit is off, the voltage must be supplied via V_{OUT}. When the electronic control is used, the V5 voltage can be as follows:

$$V5=\left(1+\frac{R3}{R1}\right) VREG+R3\times\Delta I\,REF$$
Variable voltage width

The V5 voltage boost is controlled by the I REF IC internal current source. (Δ I REF=I REF/32 for 32 voltage levels)

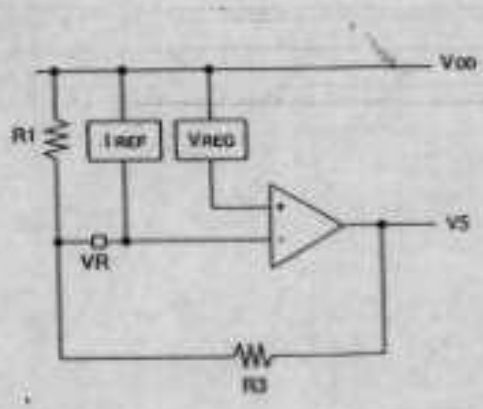
The minimum setup voltage of the V5 absolute value depends on the ratio of R1 and R3 external resistance. The voltage increase by the electronic control depends on the R3 resistance. Each resistance can be set as follows:

(1) Determine the R3 resistance based on the V5 variable voltage width of electronic control.

$$R3=\frac{\text{V5 variable voltage width}}{\text{IREF}}$$

(2) Determine the R1 resistance using R3 so have the minimum voltage of V5 absolute value.

$$R1 = \frac{R3}{\frac{V5}{VREF} - 1} \quad [V5 - (1+R3/R1) \times VREG]$$



i) The V REG reference voltage and I REF current source of the SED1530 series are fixed during voltage variation. However, the following variations may exist due to IC manufacturing and temperature conditions:
R1 and R3 of the LCD must be set by considering these variations.

VREG=-2.50V±0.25V VREG=-0.2%/°C
IREF=-3.2μA±40% IREF=-0.0324μA/°C
(during 16-level setup)
-6.5μA±40% IREF=-0.0525μA/°C
(during 32-level setup)

i) R1 is recommended to be a variable resistor and the contrast is adjusted for each IC chip for V5 voltage correction due to the V REG and I REF variation.
The contrast can be adjusted by setting the electronic control resistance to (D4, D3, D2, D1, D0)=(1, 0, 0, 0, 0) or (0, 1, 1, 1, 1).
To disable the electronic control function, set (D4, D3, D2, D1, D0)=(0, 0, 0, 0, 0) using the -RES signal or using the electronic control resistor setup command.

A constant setup example when electronic control is used:

Conditions
Absolute value of V5 voltage (Min): VDD-V5=6 V
V5 variable voltage width: 4 V
No. of variable voltage levels: 32

1) Calculating the R3 resistance

$$R3 = \frac{\text{V5 variable voltage width}}{|IREF|} = \frac{4V}{6.5\mu A}$$

R3=625kΩ

2) Calculating the R1 resistance

$$R1 = \frac{R3}{\frac{V5}{VREF} - 1} = \frac{625k\Omega}{\frac{-6V}{-2.5V} - 1}$$

R1=440kΩ

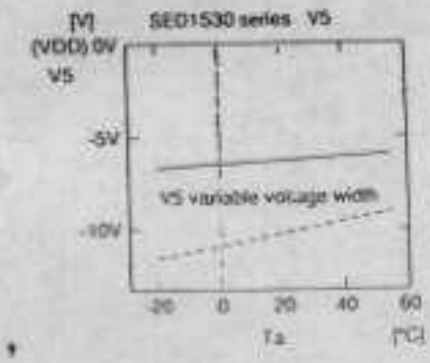
The V5 voltage due to temperature variation can be determined as follows using equation (5) (if VDD=0 V as reference):

Ta=25°C
V5min = (1+R3/R1) × VREG
= (1+625k/440k) × (-2.5V)
= -6.0V
V5max = V5min + R3 × IREF
= -6V + 625k × (-6.5μA)
= -10.0V

Ta=-10°C
V5min = (1+R3/R1) × VREG (Ta=-10°C)
= (1+625k/440k) × (-2.5V)
× {1+(-0.2%/°C) × (-10°C-25°C)}
= -6.42V
V5max = V5min + R3 × IREF (Ta=-10°C)
= -6.42V + 625k
× (-6.5μA+(0.052μA/°C) × (-10°C-25°C))
= -11.63V

Ta=-50°C
V5min = (1+R3/R1) × VREG (Ta=50°C)
= (1+625k/440k) × (-2.5V)
× {1+(-0.2%/°C) × (50°C-25°C)}
= -5.7V
V5max = V5min + R3 × IREF (Ta=50°C)
= -5.7V + 625k
× (-6.5μA+(0.052μA/°C) × (50°C-25°C))
= -8.95V

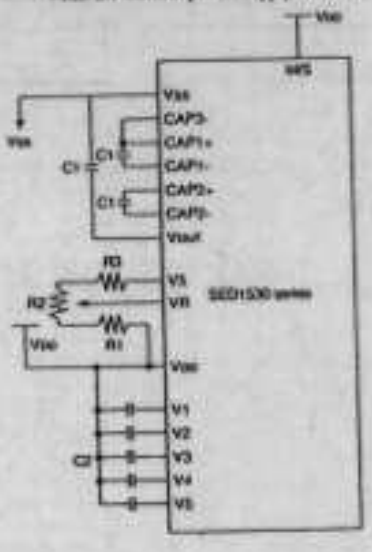
The margin voltage can also be determined by considering the I REF variation and using the same calculation procedure above. This margin calculation shows that the V5 center value is affected by the V REG and I REF variation.
The voltage adjustment step of electronic control may vary depending on the I REF variation. If the adjustment step is set to 0.2 V (Typ), for example, the voltage variation may reach 0.12 to 0.28 V Max.



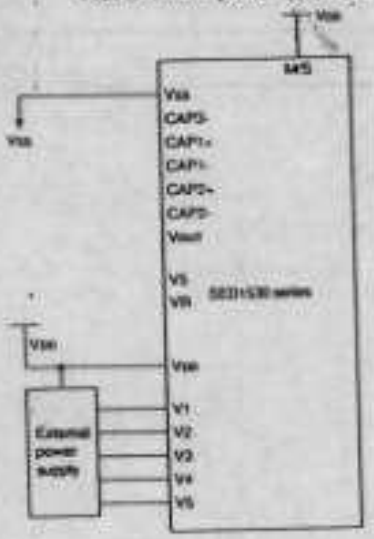
Driver IC SPEC. (EPPSON SED1530) countine.

Voltage generator circuit

when the internal power supply is used



when the internal power supply is used



Reference setup value: SED1530 V5 = -7 to -9 V
SED1531 V5 = -11 to -13 V (variable)
SED1532 V5 = -11 to -13 V (variable)

	SED1530	SED1531	SED1532
C1	1.0–4.7 uF	1.0–4.7 uF	1.0–4.7 uF
C2	0.22–0.47 uF	0.47–1.0 uF	0.47–1.0 uF
R1	700 KΩ	1 MΩ	1 MΩ
R2	200 KΩ	200 KΩ	200 KΩ
R3	1.6 MΩ	4 MΩ	4 MΩ
LCD SIZE	16 × 50 mm	32 × 64 mm	32 × 100 mm
DOT CONFIGURATION	32 × 100	64 × 128	64 × 200

*1: As the input impedance of VR is high, a noise protection using short wire and cable shield is required.

*2: C1 and C2 depend on the capacity of the LCD panel to be driven. Set a value so that the LCD drive voltage may be stable.

[Setup example]
Turn on the voltage regulator and voltage follower and give an external voltage to VOUT. Display a horizontal-stripe LCD heavy load pattern and determine C2 so that the LCD drive voltage (V1 to V5) may be stable. However, the capacity value of C2 must be all equal. Next, turn on all the on-board power supplies and determine C1.

*3: LCD SIZE means the length and breadth of the display portion of the LCD panel.

Model	LCD drive voltage
SED1530	1/5 or 1/6 bias
SED1531 SED1532	1/6 or 1/8 bias

Reset Circuit

When the RES input goes low, this LSI is initialized.

Initialized states

1. Display OFF
2. Normal display
3. ADC select: Normal display (ADC command D0 = low)
4. Read modify write OFF
5. Power control register (D2, D1, D0) = (0, 0, 0)
6. Register data clear in serial interface
7. LCD power supply bias ratio 1/6 (SED1530), 1/8 (SED1531, SED1532)
8. Static indicator: OFF
9. Display start line register set at line 1
10. Column address counter set at address 0
11. Page address register set at page 0
12. Output status register: (D3) = (0)
13. Electronic control register set at 0
14. Test command OFF

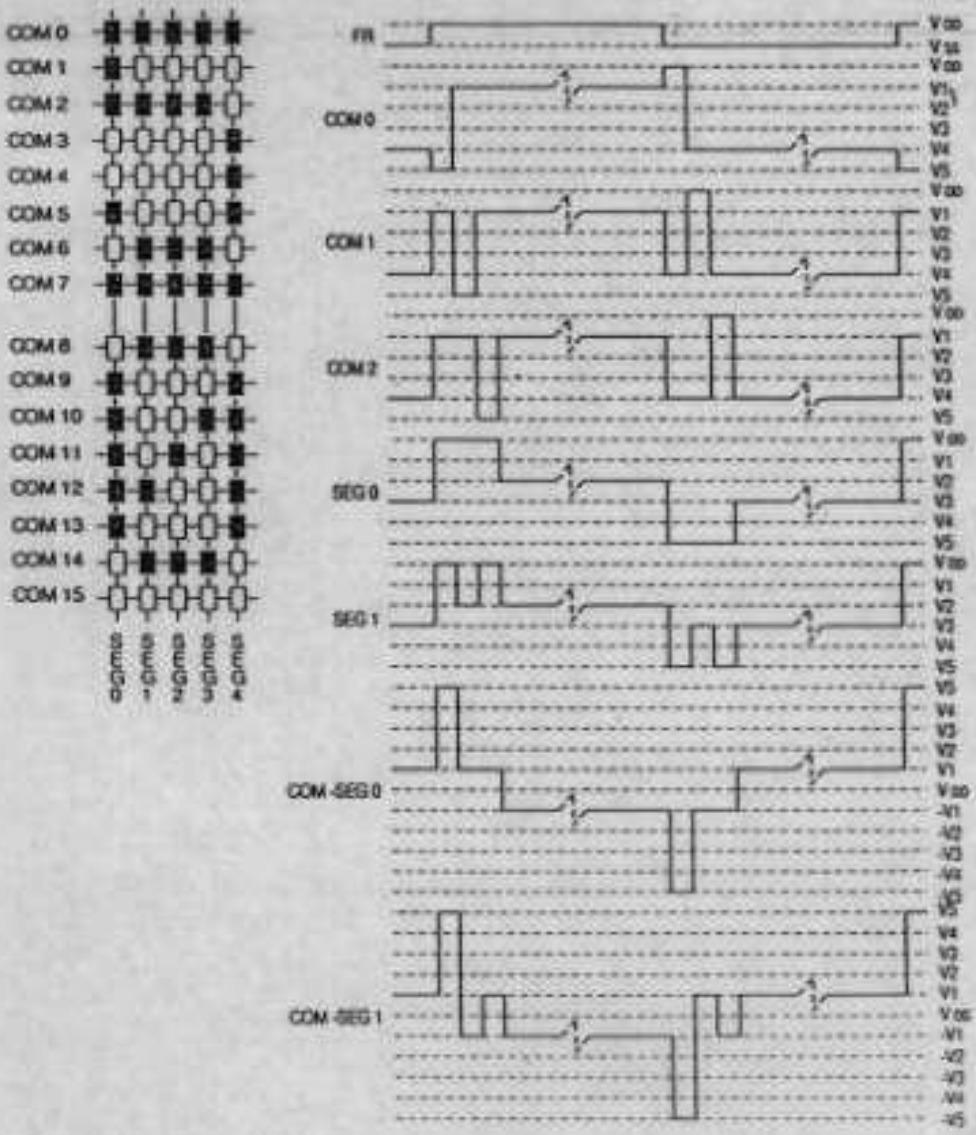
As seen in 11. Microprocessor Interface (Reference Example), connect the RES pin to the reset pin of the microprocessor and initialize the microprocessor at the same time.

In case the SED1530 series does not use the internal LCD power supply circuit, the RES must be low when the external LCD power supply is turned on.

When RES goes low, each register is cleared and set to the above initialized status. However, it has no effect on the oscillator circuit and output pins (FR, CL, DYO, D0 to D7).
If the LSI is not initialized by RES pin when power is applied, it may be put into an undesirable status. The initialization by RES pin signal is always required during power on. If the control signal from the MPU is Hz, an overcurrent may flow through the IC. A protection is required to prevent the Hz signal at the input pin during power on.

Be sure to initialize it by RES pin when turning on the power supply. When the reset command is used, only parameters 8 to 14 in the above initialization are executed.

Driver IC SPEC.(EPPSON SED1530) countine.



COMMANDS

The SED1530 series uses a combination of A0, $\overline{RD}$ (E) and $\overline{WR}$ (R/$\overline{W}$) signals to identify data bus signals. As the chip analyzes and executes each command using internal timing clock only regardless of external clock, its processing speed is very high and its busy check is usually not required. The 8080 series microprocessor interface enters a read status when a low pulse is input to the $\overline{RD}$ pin and a write status when a low pulse is input to the $\overline{WR}$ pin. The 6800 series microprocessor interface enters a read status when a high pulse is input to the R/$\overline{W}$ pin and a write status when a low pulse is input to this pin. When a high pulse is input to the E pin, the command is activated. (For timing, see 10. Timing Characteristics.) Accordingly, in the command explanation and command table, $\overline{RD}$ (E) becomes 1 (high) when the 6800 series microprocessor interface reads status or display data. This is an only different point from the 8080 series microprocessor interface.

Taking the 8080 series microprocessor interface as an example, commands will be explained below.
When the serial interface is selected, input data starting from D7 in sequence.

- Command set

(1) Display ON/OFF
Alternatively turns the display on and off.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	1	1	D

The display turns off when D goes low, and it turns on when D goes high.

(2) Start Display Line
Specifies line address (refer to Figure 4) to determine the initial display line, or COM0. The RAM display data becomes the top line of LCD screen. It is followed by the higher number of lines in ascending order, corresponding to the duty cycle. When this command changes the line address, the smooth scrolling or page change takes place.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	1	A5	A4	A3	A2	A1	A0

← High-order bit

A5	A4	A3	A2	A1	A0	Line address
0	0	0	0	0	0	0
0	0	0	0	0	1	1
0	0	0	0	1	0	2
:						:
1	1	1	1	1	0	62
1	1	1	1	1	1	63

(3) Set Page Address
Specifies page address to load display RAM data to page address register. Any RAM data bit can be accessed when its page address and column address are specified. The display remains unchanged even when the page address is changed.
Page address 8 is the display RAM area dedicate to the indicator, and only D0 is valid for data change.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	1	A3	A2	A1	A0

A3	A2	A1	A0	Page Address
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8

(4) Set Column Address
Specifies column address of display RAM. Divide the column address into 4 higher bits and 4 lower bits. Set each of them successively. When the microprocessor repeats to access to the display RAM, the column address counter is incremented by 1 during each access until address 132 is accessed. The page address is not changed during this time.

	A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
Higher bits	0	1	0	0	0	0	1	A7	A6	A5	A4
Lower bits	0	1	0	0	0	0	0	A3	A2	A1	A0

A7	A6	A5	A4	A3	A2	A1	A0	Column address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
:								:
1	0	0	0	0	0	1	1	131

(5) Read Status

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0

BUSY: When high, the SED1526 series is busy due to internal operation or reset. Any command is rejected until BUSY goes low. The busy check is not required if enough time is provided for each cycle.

ADC: Indicates the relationship between RAM column address and segment drivers. When low, the display is normal and column address "131 to" corresponds to segment driver a. When high, the display is reversed and column address a corresponds to segment driver a.

ON/OFF: Indicates whether the display is on or off. When goes low, the display turns on. When goes high, the display turns off. This is the opposite of Display ON/OFF command.

RESET: Indicates the initialization is in progress by $\overline{RES}$ signal or by Reset command. When low, the display is on. When high, the chip is being reset.

(6) Write Display Data
Writes 8-bit data in display RAM. As the column address is incremented by 1 automatically after each write, the microprocessor can continue to write data of multiple words.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	Write data							

(7) Read Display Data

Reads 8-bit data from display RAM area specified by column address and page address. As the column address is incremented by 1 automatically after each write, the microprocessor can continue to read data of multiple words. A single dummy read is required immediately after column address setup. Refer to the display RAM section of FUNCTIONAL DESCRIPTION for details. Note that no display data can be read via the serial interface.

A0	E RD	R/W WR	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	Read data							

(8) ADC Select

Changes the relationship between RAM column address and segment driver. The order of segment driver output pins can be reversed by software. This allows flexible IC layout during LCD module assembly. For details, refer to the column address section of Figure 4. When display data is written or read, the column address is incremented by 1 as shown in Figure 4.

A0	E RD	R/W WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	0	0	D

When D is low, the right rotation (normal direction). When D is high, the left rotation (reverse direction).

(9) Normal/Reverse Display

Reverses the Display ON/OFF status without rewriting the contents of the display data RAM.

A0	E RD	R/W WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	1	1	D

When D is low, the RAM data is high, being LCD ON potential (normal display).
When D is high, the RAM data is low, being LCD ON potential (reverse display).

(10) Entire Display ON

Forcibly turns the entire display on regardless of the contents of the display data RAM. At this time, the contents of the display data RAM are held.
This command has priority over the Normal/Reverse Display command. When D is low, the normal display status is provided.

A0	E RD	R/W WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	1	0	D

When D is high, the entire display ON status is provided.
If the Entire Display ON command is executed in the display OFF status, the LCD panel enters Power Save mode. Refer to the Power Save section for details.

(11) Set LCD Bias

Selects a bias ratio of the voltage required for driving the LCD. This command is enabled when the voltage follower in the power supply circuit operates.

A0	E RD	R/W WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	0	1	0

Model	D	Bias ratio of LCD power supply
SED1530	0	1/6 bias
	1	1/5 bias
SED1531	0	1/6 bias
SED1532	1	1/6 bias

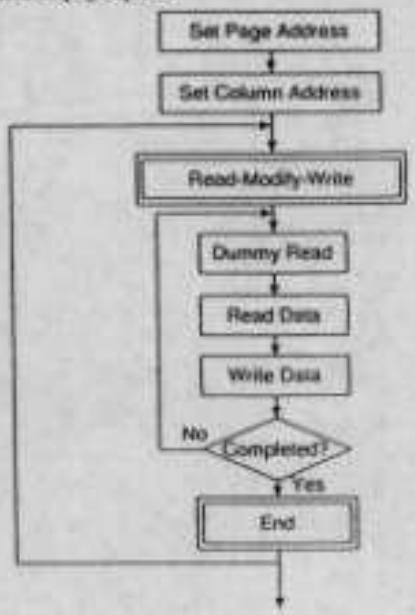
(12) Read-Modify-Write

A pair of Read-Modify-Write and End commands must always be used. Once Read-Modify-Write is issued, column address is not incremented by Read Display Data command but incremented by Write Display Data command only. It continues until End command is issued. When the End is issued, column address returns to the address when Read-Modify-Write was issued. This can reduce the microprocessor load when data of a specific display area is repeatedly changed during cursor blinking or others.

A0	E RD	R/W WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

Note: Any command except Read/Write Display Data and Set Column Address can be issued during Read-Modify-Write mode.

- Cursor display sequence



(7) Read Display Data
Reads 8-bit data from display RAM area specified by column address and page address. As the column address is incremented by 1 automatically after each write, the microprocessor can continue to read data of multiple words. A single dummy read is required immediately after column address setup. Refer to the display RAM section of FUNCTIONAL DESCRIPTION for details. Note that no display data can be read via the serial interface.

A0	E RD	R/W WR	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	Read data							

(8) ADC Select
Changes the relationship between RAM column address and segment driver. The order of segment driver output pins can be reversed by software. This allows flexible IC layout during LCD module assembly. For details, refer to the column address section of Figure 4. When display data is written or read, the column address is incremented by 1 as shown in Figure 4.

A0	E RD	R/W WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	0	0	D

When D is low, the right rotation (normal direction). When D is high, the left rotation (reverse direction).

(9) Normal/Reverse Display
Reverses the Display ON/OFF states without rewriting the contents of the display data RAM.

A0	E RD	R/W WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	1	1	D

When D is low, the RAM data is high, being LCD ON potential (normal display).
When D is high, the RAM data is low, being LCD ON potential (reverse display).

(10) Entire Display ON
Forcibly turns the entire display on regardless of the contents of the display data RAM. At this time, the contents of the display data RAM are held.
This command has priority over the Normal/Reverse Display command. When D is low, the normal display status is provided.

A0	E RD	R/W WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	1	0	0

When D is high, the entire display ON status is provided.
If the Entire Display ON command is executed in the display OFF status, the LCD panel enters Power Save mode. Refer to the Power Save section for details.

(11) Set LCD Bias
Selects a bias ratio of the voltage required for driving the LCD. This command is enabled when the voltage follower in the power supply circuit operates.

A0	E RD	R/W WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	0	1	0

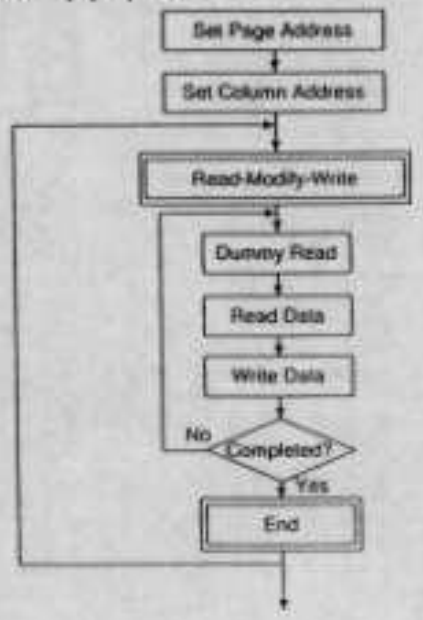
Model	D	Bias ratio of LCD power supply
SED1530	0	1/6 bias
	1	1/5 bias
SED1531	0	1/8 bias
SED1532	1	1/6 bias

(12) Read-Modify-Write
A pair of Read-Modify-Write and End commands must always be used. Once Read-Modify-Write is issued, column address is not incremented by Read Display Data command but incremented by Write Display Data command only. It continues until End command is issued. When the End is issued, column address returns to the address when Read-Modify-Write was issued. This can reduce the microprocessor load when data of a specific display area is repeatedly changed during cursor blinking or others.

A0	E RD	R/W WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

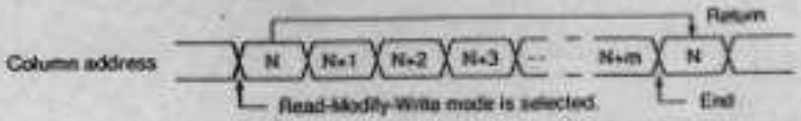
Note: Any command except Read/Write Display Data and Set Column Address can be issued during Read-Modify-Write mode.

- Cursor display sequence



(13) End
Cancels Read-Modify-Write mode and returns column address to the original address (when Read-Modify-Write was issued).

A0	E RD	R/W WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0



(14) Reset
Resets the Initial Display Line register, Column Address counter, Page Address register, and output status selector circuit to their initial status. The Reset command does not affect on the contents of display RAM. Refer to the Reset circuit section of FUNCTIONAL DESCRIPTION.

A0	E RD	R/W WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	0

The Reset command cannot initialize LCD power supply. Only the Reset signal to the RES pin can initialize the supplies.

(15) Output Status Select Register
Applicable to the SED1530 and SED1532. When D is high or low, the scan direction of the COM output pin is selectable. Refer to Output Status Selector Circuit in Functional Description for details.

A0	E RD	R/W WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	0	D	*	*	*

D: Selects the scan direction of COM output pin
*: Invalid bit
D1 must be set to "1"

(16) Set Power Control
Selects one of eight power circuit functions using 3-bit register. An external power supply and part of internal power supply functions can be used simultaneously. Refer to Power Circuit section of FUNCTIONAL DESCRIPTION for details.

A0	E RD	R/W WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	0	1	A2	A1	A0

When A0 goes low, voltage follower turns off. When A0 goes high, it turns on.
When A1 goes low, voltage regulator turns off. When A1 goes high, it turns on.
When A2 goes low, voltage booster turns off. When A2 goes high, it turns on.

(17) Set Electronic Control
Adjusts the contrast of LCD panel display by changing V5 LCD drive voltage that is output by voltage regulator of on-board power supply.
This command selects one of 32 V5 LCD drive voltages by storing data in 5-bit register. The V5 voltage adjusting range should be determined depending on the external resistance. Refer to the Voltage Regulator Circuit section of FUNCTIONAL DESCRIPTION for details.

A0	RD	R/W WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	A4	A3	A2	A1	A0

D4	D3	D2	D1	D0	| V5 |
0	0	0	0	0	Low
0	0	0	0	1	
0	0	0	1	0	
		:			↓
1	1	1	0	1	
1	1	1	1	0	
1	1	1	1	1	High

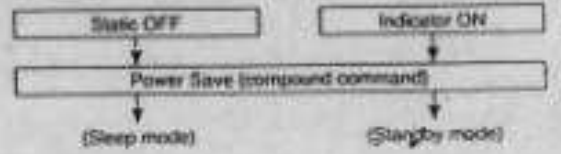
Set register to (D4,D3,D2,D1,D0)=(0,0,0,0,0) to suppress electronic control function.

(18) Static Indicator
This command turns on or off static drive indicators. The indicator display is controlled by this command only, and it is not affected by the other display control commands.
Either FR or FRS terminal is connected to either of static indicator LCD drive electrodes, and the remaining terminal is connected to another electrode. When the indicator is turned on, the static drive operates and the indicator blinks at an interval of approximately one second. The pattern separation between indicator electrodes are dynamic drive electrodes is recommended. A closer pattern may cause an LCD and electrode deterioration.

A0	E RD	R/W WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	1	0	D

D: 0: Static indicator OFF
1: Static indicator ON

(19) Power Save (Compound Command)
When all displays are turned on during indicator off, the Power Save command is issued so greatly reduce the current consumption.
If the static indicators are off, the Power Save command sleeps the system. If on, this command stands by the system.



Sleep mode
This mode stops every operation of the LCD display system and can reduce current consumption nearly to a static current value if no access is made from the microprocessor. The internal states in the sleep mode is as follows:

(1) Stops the oscillator circuit and LCD power supply circuit.
(2) Stops the LCD drive and outputs the VDD level as the segment/common driver output.
(3) Holds the display data and operation mode provided before the start of the sleep mode.
(4) The MPU can access to the built-in display RAM.

Standby mode
Stops the operation of the duty LCD display system and turns on only the static drive system to reduce current consumption to the minimum level required for static drive.
The ON operation of the static drive system indicates that the SED1530 series is in the standby mode. The internal status in the standby mode is as follows:

(1) Stops the LCD power supply circuit.
(2) Stops the LCD drive and outputs the VDD level as the segment/common driver output. However, the static drive system operates.
(3) Holds the display data and operation mode provided before the start of the standby mode.
(4) The MPU can access to the built-in display RAM.

When the LCD drive voltage level is given by an external resistive driver, the current of this resistor must be cut so that it may be fixed to floating or VDD level, prior to or concurrently with causing the 1530 series to go to the sleep mode or standby mode.
When an external power supply is used, likewise, the function of this external power supply must be stopped so that it may be fixed to floating or VDD level, prior to or concurrently with causing the SED1530 series to go to the sleep mode or standby mode.

When the common driver SED1635 is combined with the SED1531 in the configuration, the DOF pin of the SED1531 must be connected to the DOFF pin of the SED1635.

(20) Test Command
This is the dedicate IC chip test command. It must not be used for normal operation. If the Test command is issued erroneously, set the -RES input to low or issue the Reset command to release the test mode.

A0	E RD	R/W WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	1	*	*	*	*

*: Invalid bit

Caution: The SED1530 Series holds an operation status specified by each command. However, the internal operation status may be changed by a high level of ambient noise. It must be considered to suppress the noise on the its package and system or to prevent an ambient noise insertion. To prevent a spike noise, a built-in software for periodical status refreshment is recommended to use.

Driver IC SPEC.(EPPSON SED1530) countine.

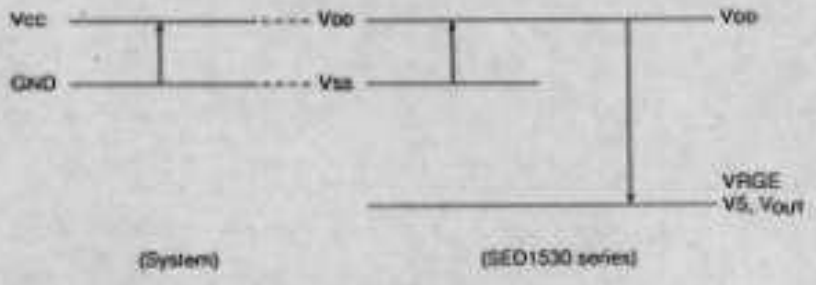
SED1530 Series Command Table

Command	Code											Function
	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	
(1) Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0 1	Turns on LCD panel when goes high, and turns off when goes low.
(2) Initial Display Line	0	1	0	0	1	Start display address						Specifies RAM display line for COM0.
(3) Set Page Address	0	1	0	1	0	1	1	Page address				Sets the display RAM page in Page Address register.
(4) Set Column Address 4 higher bits	0	1	0	0	0	0	1	Higher column address				Sets 4 higher bits of column address of display RAM in register
(4) Set Column Address 4 lower bits	0	1	0	0	0	0	0	Lower column address				Sets 4 lower bits of column address of display RAM in register
(5) Read Status	0	0	1	Status				0	0	0	0	Reads the status information.
(6) Write Display Data	1	1	0	Write data								Writes data in display RAM.
(7) Read Display Data	1	0	1	Read data								Reads data from display RAM.
(8) ADC Select	0	1	0	1	0	1	0	0	0	0	0 1	Sets normal relationship between RAM column address and segment driver when low, but reverses the relationship when high.
(9) Normal/Reverse Display	0	1	0	1	0	1	0	0	1	1	0 1	Normal indication when low, but full indication when high.
(10) Entire Display ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	Selects normal display (0) or Entire Display ON (1).
(11) Set LCD Bias	0	1	0	1	0	1	0	0	0	1	0 1	Sets LCD drive voltage bias ratio.
(12) Read-Modify-Write	0	1	0	1	1	1	0	0	0	0	0	Increments Column Address counter during each write when high and during each read when low.
(13) End	0	1	0	1	1	1	0	1	1	1	0	Releases the Read-Modify-Write.
(14) Reset	0	1	0	1	1	1	0	0	0	1	0	Resets internal functions.
(15) Set Output Status Register	0	1	0	1	1	0	0	0 1	*	*	*	Selects COM output scan direction. * Invalid data
(16) Set Power Control	0	1	0	0	0	1	0	1	Operation status			Selects the power circuit operation mode.
(17) Set Electronic Control Register	0	1	0	1	0	0	Electronic control value					Sets V5 output voltage to Electronic Control register.
(18) Set Standby	0	1	0	1	0	1	0	1	1	0	0 1	Selects standby status. 0: OFF 1: ON
(19) Power Save	-	-	-	-	-	-	-	-	-	-	-	Compound command of display OFF and entire display ON
(20) Test Command	0	1	0	1	1	1	1	*	*	*	*	IC Test command. Do not use!

Note: Do not use any other command, or the system malfunction may result.

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Rating	Unit
Supply voltage range		V_{DD}	−0.3 to +7.0	V
	Triple voltage conversion		−0.3 to +6.0	
	Quadruple voltage conversion		−0.3 to +4.5	
Supply voltage range (1) (V_{DD} Level)		V5	−18.0 to +0.3	V
Supply voltage range (2) (V_{DD} Level)		V1, V2, V3, V4	V5 to +0.3	V
Input voltage range		V_{IN}	−0.3 to V_{DD}+0.3	V
Output voltage range		V0	−0.3 to V_{DD}+0.3	V
Operating temperature range		T_{OPR}	−40 to +85	°C
Storage temperature range	TCP	T_{STR}	−55 to +100	°C
	Bear chip		−55 to +125	



(System) (SED1530 series)

Notes: 1. V1 to V5, V_{OUT}, and V5 voltages are based on V_{DD}=0 V.
2. Voltages $V_{DD} \geq V1 \geq V2 \geq V3 \geq V4 \geq V5$ must always be satisfied.
3. If an LSI exceeds its absolute maximum rating, it may be damaged permanently. It is desirable to use it under electrical characteristics conditions during general operation. Otherwise, an LSI malfunction or reduced LSI reliability may result.

ELECTRICAL CHARACTERISTICS

DC Characteristics

V_{SS} = 0 V, V_{DD} = 5 V ±10%, Ta = −40 to +85°C unless otherwise noted.

Item		Symbol	Condition		Min.	Typ.	Max.	Unit	Pin used
Power voltage (1)	Recommended Operation	V_{DD}			4.5	5.0	5.5	V	V_{SS} *1
	Operational				2.4	–	6.0		
Operating voltage (2)	Operational	V5	V_{DD} level (V_{DD} = 0 V)		−16.0	–	−4.5	V	V5 *2
	Operational	V1, V2	V_{DD} level (V_{DD} = 0 V)		0.4 × V5	–	V_{DD}	V	V1, V2
	Operational	V3, V4	V_{DD} level (V_{DD} = 0 V)		V5	–	0.6 × V5	V	V3, V4
CMOS	High-level input voltage	V_{IHC}			0.7 × V_{DD}	–	V_{DD}	V	*3
			V_{DD} = 2.7 V		0.8 × V_{DD}	–	V_{DD}		*3
	Low-level input voltage	V_{ILC}			V_{SS}	–	0.3 × V_{DD}	V	*3
			V_{DD} = 2.7 V		V_{SS}	–	0.2 × V_{DD}		*3
	High-level output voltage	V_{OHC}	I_{OH} = −1 mA		0.8 × V_{DD}	–	V_{DD}	V	*5
			V_{DD} = 2.7 V, I_{OH} = −0.5 mA		0.8 × V_{DD}	–	V_{DD}		*5
	Low-level output voltage	V_{OLC}	I_{OL} = 1 mA		V_{SS}	–	0.2 × V_{DD}	V	*5
			V_{DD} = 2.7 V, I_{OL} = 0.5 mA		V_{SS}	–	0.2 × V_{DD}		*5
Schmitt	High-level input voltage	V_{HS}			0.85 × V_{DD}	–	V_{DD}		*4
			V_{DD} = 2.7 V		0.8 × V_{DD}	–	V_{DD}		*4
	Low-level input voltage	V_{LS}			V_{SS}	–	0.15 × V_{DD}		*4
			V_{DD} = 2.7 V		V_{SS}	–	0.2 × V_{DD}		*4
Input leakage current		I_{LI}	V_{IN} = V_{DD} or V_{SS}		−1.0	–	1.0	μA	*6
Output leakage current		I_{LO}			−3.0	–	3.0	μA	*7
LCD driver ON resistance		R_{ON}	Ta = 25°C	V5 = −14.0 V	–	2.0	3.0	KΩ	SEG n COM n
			V_{DD} level	V5 = −8.0 V	–	3.0	4.5		*8
Static current consumption		I_{SSQ}	V_{IN} = V_{DD} or V_{SS}		–	0.01	5.0	μA	V_{SS}
		I_{SO}	V5 = −18.0 V (V_{DD} level)		–	0.01	15.0	μA	V5
Input pin capacity		C_{IN}	Ta = 25°C, f = 1 MHz		–	5.0	8.0	pF	*3 *4
Oscillation frequency		f_{OSC}	Ta = 25°C	V_{DD} = 5 V	19	22	25	kHz	*9
				V_{DD} = 2.7 V	19	22	25		

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Built-in power circuit	Input voltage	V_{DD}	Triple voltage conversion	2.4	–	6.0	V	*10
			Quadruple voltage conversion	2.4	–	4.5		
	Booster output voltage	V_{OUT}	Triple voltage conversion (V_{DD} level)	−16.0	–	–	V	V_{OUT}
	Voltage regulator operation voltage	V_{OUT}	(V_{DD} level)	−18.0	–	−6.0	V	V_{OUT}
	Voltage follower operation voltage	V5	(V_{DD} level)	−18.0	–	−6.0	V	*11
				−16.0	–	−4.5	V	
	Reference voltage	V_{REG}	Ta = 25°C (V_{DD} level)	−2.75	−2.55	−2.35	V	

Driver IC SPEC.(EPPSON SED1530) countine.

Dynamic current consuption value (1) Display status with the on-board power syppiy ON

No special specification Ta = -40 to +85°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
SED1530	I_{DD} (1)	V_{DD} = 5.0 V, V5 – V_{DD} = -8.0 V, 2-time voltage increase	—	41	70	μA	*13
		V_{DD} = 3.0 V, V5 – V_{DD} = -8.0 V, 3-time voltage increase	—	48	80	μA	
SED1531		V_{DD} = 5.0 V, V5 – V_{DD} = -11.0 V, 3-time voltage increase	—	96	160	μA	
		V_{DD} = 3.0 V, V5 – V_{DD} = -11.0 V, 4-time voltage increase	—	118	190	μA	
SED1532		V_{DD} = 5.0 V, V5 – V_{DD} = -11.0 V, 3-time voltage increase	—	95	160	μA	
		V_{DD} = 3.0 V, V5 – V_{DD} = -11.0 V, 4-time voltage increase	—	114	190	μA	

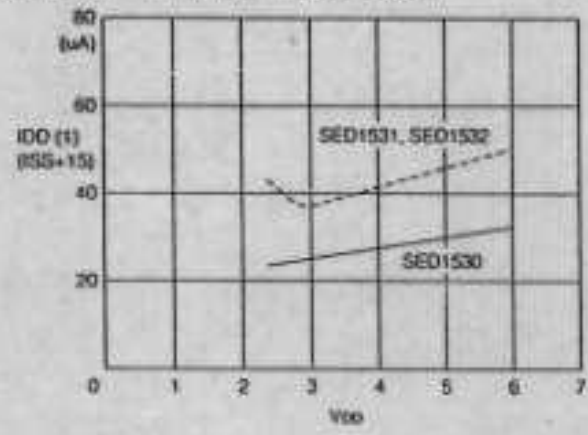
Current consuption in Power Save mode

Vss=0V, Vdd=2.7~5.5V Ta = 25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
Sleep	I_{DDS1}	SED1530, SED1531, SED1532	—	0.01	1	μA	
Standby	I_{DDS2}	SED1530, SED1531, SED1532	—	1.0	2.0	μA	

Typical current consuption characteristics

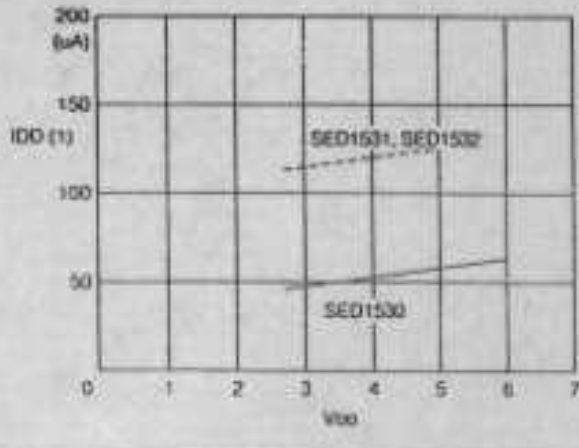
- Dynamic current consuption (1)
  LCD display status using an external power syupply



Condition: Internal power supply off using external power supply
SED1530 V5-Vdd=-8.0V
SED1531 V5-Vdd=-11.0V
SED1532 V5-Vdd=-11.0V

Remarks: *12

- Dynamic current consuption (1)
  LCD display status using internal power syupply



Condition: Internal power supply on
SED1530 V5-Vdd=-8.0V,
triple voltage conversion
SED1531 V5-Vdd=-11.0V,
quadruple voltage conversion
SED1532 V5-Vdd=-11.0V,
quadruple voltage conversion

Remarks: *13

*1 Though the wide range of operating voltages is guaranteed, a spike voltage change may affect the voltage assurance during access from the microprocessor.
*2 V_{DD} and V5 operating voltage range. (Refer to Fig. 10.)
The operating voltage range applies if an external power supply is used.
*3 A0, D0 - D5, D6, D7 (SI), RD (E), WR (R/W), CS1, CS2, FR, M/S, C86, P/S and DOF pins
*4 CL, SCL (D6) and RES pins
*5 D0 - D5, D6, D7 (SI), FR, FRS, DYO, DOF and CL pins
*6 A0, RD (E), WR (R/W), CS1, CS2, M/S, RES, C86 and P/S pins
*7 Applies when the D0 - D7, FR, CL, DYO and DOF pins are in high impedance.
*8 Resistance value when 0.1 V is applied between the output pin SEGn or COMn and each power supply pin (V1, V2, V3, V4).
This is specified in the operating voltage (2) range.
R ON = 0.1 V/ΔI (ΔI: Current flowing when 0.1 V is applint in the ON status.)
*9 For the relationship between oscillation frequency and frame frequency, refer to Fig. 9.
*10 For triple or quadruple voltage conversion using the on-board power supply, use the primary-side power supply V_{DD} within the input voltage range.
*11 The voltage regulator circuit adjusts V5 within the voltage follower operating voltage range.
*12, *13 Current that each IC unit consumes. It does not include the current of the LCD panel capacity, wiring capacity, etc.
This is current consumption under the conditions of display data = checker, display ON, SED1530 = 1/33 duty, and SED1531 and SED1532 = 1/65 duty.
*12 Applies to the case where the internal oscillator circuit is used and no access is made from the microprocessor.
*13 Applies to the case where the internal oscillator circuit and the on-board power supply circuit are used and no access is made from the microprocessor.
Measuring conditions: C1 = 4.7 µF, C2 = C3 = 1.0 µF, R1 + R3 = 2 MΩ, including the current flowing to the voltage regulation resistance (R1 + R3 = 2 MΩ).
The current consumption, when the on-board power booster circuit is used, is for the power supply V_{DD}.

- Relationship between oscillation frequency and frame frequency

The relationship between oscillation frequency f OSC and LCD frame frequency fF can be obtained by the following expression.

	Duty	f CL	f F
SED1530	1/33	f osc/8	f osc/(8*33)
SED1531 SED1532	1/65	f osc/4	f osc/(4*65)

(fF does not indicate the FR signal cycle but the AC cycle.)

Fig. 9

Relationship between clock (fCL) and frame frequency fF

- V_{SS} and V5 operating voltage range

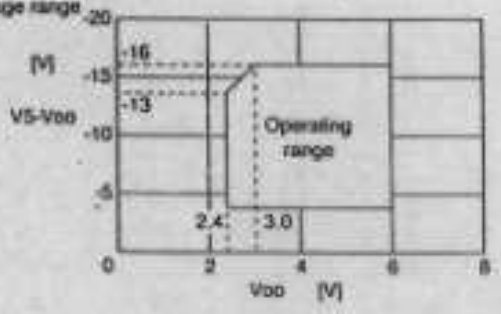
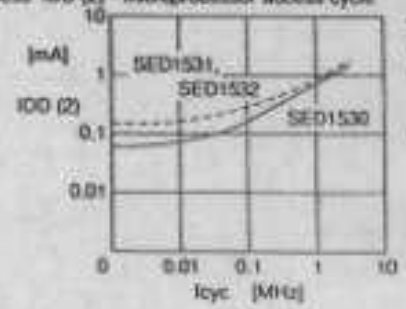


Fig 10

- Current consumption at access IDD (2) - Microprocessor access cycle



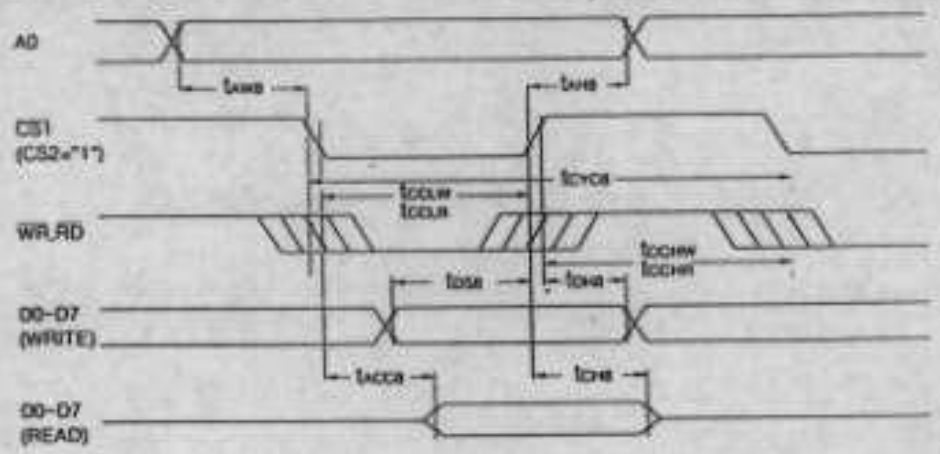
This indicates current consumption when data is always written on the vertical-strip pattern at fcyc. When no access is made, only IDD (1) occurs.

Condition: SED1530 V5-Voo=-8.0V, triple voltage conversion
SED1531 V5-Voo=-11.0V, quadruple voltage conversion
SED1532 V5-Voo=-11.0V, quadruple voltage conversion

AC Characteristics

(1) System buses

Read/write characteristics I (5080-series microprocessor)



V_{DD} = 5.0 V ±10%, Ta = −40 to +85°C

Parameter	Signal	Symbol	Condition	Min.	Max.	Unit
Address hold time Address setup time	A0	t_{AWR} t_{AWR}		10 10	– –	ns ns
System cycle time		t_{CYCS}		166	–	ns
Control L pulse width (WR) Control L pulse width (RD) Control H pulse width (WR) Control H pulse width (RD)	$\overline{WR}$ $\overline{RD}$ $\overline{WR}$ $\overline{RD}$	t_{CCLW} t_{CCLR} t_{CCHW} t_{CCHR}		30 70 100 70	– – – –	ns ns ns ns
Data setup time Data hold time		t_{DSR} t_{DHR}		20 10	– –	ns ns
$\overline{RD}$ access time Output disable time	D0–D7	t_{ACCR} t_{CHR}	CL=100pF	– 10	70 50	ns ns

V_{DD} = 2.7 V to 4.5 V, Ta = −40 to +85°C

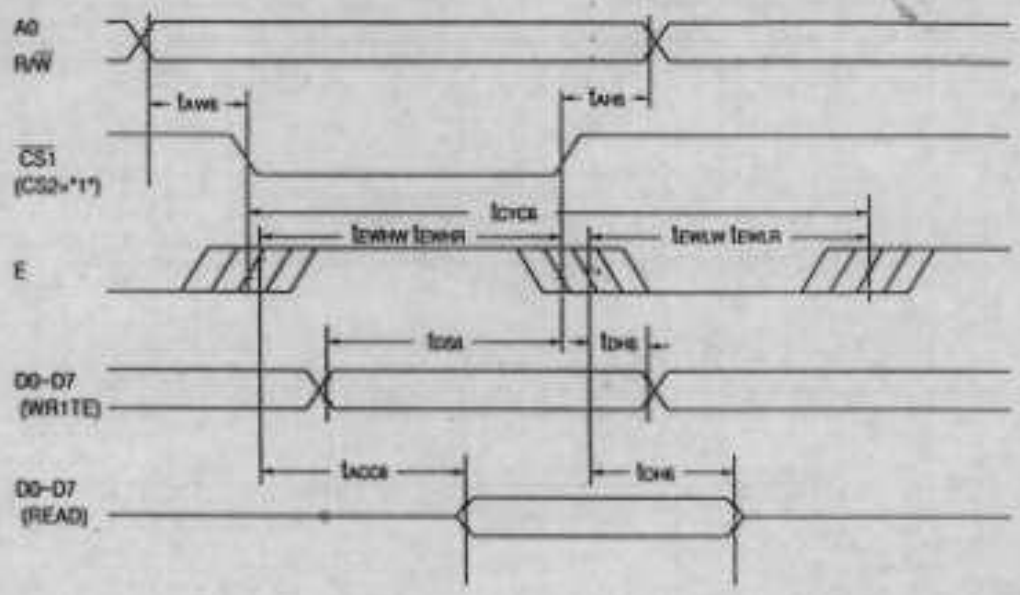
Parameter	Signal	Symbol	Condition	Min.	Max.	Unit
Address hold time Address setup time	A0	t_{AWR} t_{AWR}		25 25	– –	ns ns
System cycle time		t_{CYCS}		450	–	ns
Control L pulse width (WR) Control L pulse width (RD) Control H pulse width (WR) Control H pulse width (RD)	$\overline{WR}$ $\overline{RD}$ $\overline{WR}$ $\overline{RD}$	t_{CCLW} t_{CCLR} t_{CCHW} t_{CCHR}		60 140 200 140	– – – –	ns ns ns ns
Data setup time Data hold time		t_{DSR} t_{DHR}		40 20	– –	ns ns
$\overline{RD}$ access time Output disable time	D0–D7	t_{ACCR} t_{CHR}	CL=100pF	– 10	140 100	ns ns

Notes: 1. The input signal rise/fall time (tr, tf) is specified at 15 ns or less.
When system cycle time is used at a high speed, it is specified by tr + tf ≤ (t_{CYCS} − t_{CCLW} − t_{CCHW}) or
tr + tf ≤ (t_{CYCS} − t_{CCLR} − t_{CCHR}).
2. Every timing is specified on the basis of 20% and 80% of V_{DD}.
3. t_{CCLW} and t_{CCLR} are specified by the overlap period in which $\overline{CS1}$ is "0" (CS2 = "1") and $\overline{WR}$ and $\overline{RD}$ are "0".

■ Driver IC SPEC.(EPPSON SED1530) countine.

(2) System buses

Read/write characteristics II (6800-series microprocessor)



V_{DD} = 5.0 V ±10%, Ta = −40 to +85°C

Parameter		Signal	Symbol	Condition	Min.	Max.	Unit
System cycle time			t_{CYC6}		166	–	ns
Address setup time Address hold time		A0 R/W	t_{AWR} t_{AH6}		10 10	– –	ns ns
Data setup time Data hold time		D0-D7	t_{DS6} t_{DH6}		20 10	– –	ns ns
Output disable time Access time			t_{OH6} t_{ACC6}	CL=100pF	10 –	50 70	ns ns
Enable low pulse width	READ	E	t_{EWLR}		70	–	ns
	WRITE		t_{EWLW}		30	–	ns
Enable high pulse width	READ	E	t_{EWHR}		70	–	ns
	WRITE		t_{EWHW}		100	–	ns

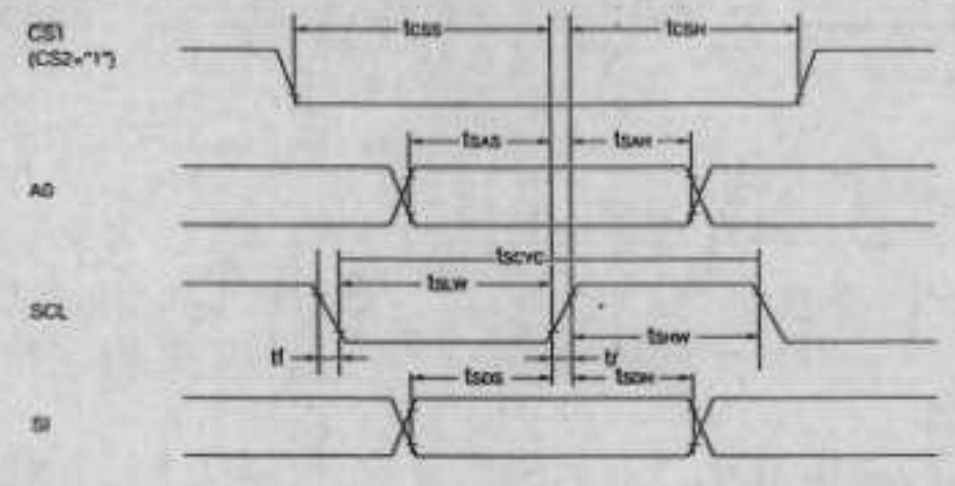
V_{DD} = 2.7 V to 4.5 V, Ta = −40 to +85°C

Parameter		Signal	Symbol	Condition	Min.	Max.	Unit
System cycle time			t_{CYC6}		450	–	ns
Address setup time Address hold time		A0 R/W	t_{AWR} t_{AH6}		25 25	– –	ns ns
Data setup time Data hold time		D0-D7	t_{DS6} t_{DH6}		40 20	– –	ns ns
Output disable time Access time			t_{OH6} t_{ACC6}	CL=100pF	10 –	100 140	ns ns
Enable low pulse width	READ	E	t_{EWLR}		140	–	ns
	WRITE		t_{EWLW}		60	–	ns
Enable high pulse width	READ	E	t_{EWHR}		140	–	ns
	WRITE		t_{EWHW}		200	–	ns

Notes: 1. The input rise/fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is used at a high speed, it is specified by tr + tf < (tCYC6 - tEWLW - tEWHW) or tr + tf < (tCYC6 - tEWLR - tEWHR).
2. Every timing is specified on the basis of 20% and 80% of VDD.
3. tEWHR and tEWHW are specified by the overlap period in which CS1 is "0" (CS2 = "1") and E is "1".

Driver IC SPEC.(EPPSON SED1530) countine.

(3) Serial interface



V_{DD} = 5.0 V ±10%, Ta = −40 to +85°C

Parameter	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock cycle Serial clock H pulse width Serial clock L pulse width	SCL	t_{SCYC} t_{SHW} t_{SLW}		500 150 150	- - -	ns ns ns
Address setup time Address hold time	A0	t_{SAS} t_{SAH}		120 200	- -	ns ns
Data setup time Data hold time	SI	t_{SDS} t_{SDH}		120 50	- -	ns ns
$\overline{CS}$ serial clock time	CS	t_{CSS} t_{CSH}		30 400	- -	ns

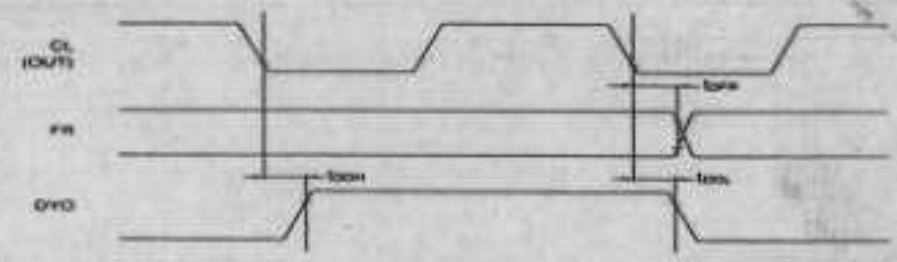
V_{DD} = 2.7 to 4.5V, Ta = −40 to +85°C

Parameter	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock cycle Serial clock H pulse width Serial clock L pulse width	SCL	t_{SCYC} t_{SHW} t_{SLW}		1000 300 300	- - -	ns ns ns
Address setup time Address hold time	A0	t_{SAS} t_{SAH}		250 400	- -	ns ns
Data setup time Data hold time	SI	t_{SDS} t_{SDH}		250 100	- -	ns ns
$\overline{CS}$ serial clock time	CS	t_{CSS} t_{CSH}		60 600	- -	ns

Notes: 1. The input signal rise and fall times must be within 15 nanoseconds.
2. All signal timings are limited based on 20% and 80% of V_{DD} voltage.

Driver IC SPEC.(EPPSON SED1530) countine.

(4) Display control timing



Output timing

V_{DD} = 5.0 V ±10%, Ta = -40 to +85°C

Parameter	Signal	Symbol	Condition	Min.	Typ.	Max.	Unit
FR delay time	FR	t_{DFR}	CL = 50 pF	-	60	150	ns
DYO "H" delay time	DYO	t_{DDH}		-	70	160	ns
DYO "L" delay time		t_{DDL}		-	70	160	ns

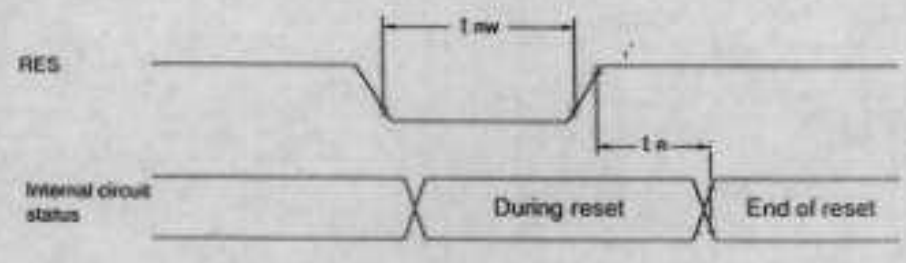
Output timing

V_{SS} = 0 V, V_{DD} = 2.7 V to 4.5 V, Ta = -40 to +85°C

Parameter	Signal	Symbol	Condition	Min.	Typ.	Max.	Unit
FR delay time	FR	t_{DFR}	CL = 50 pF	-	120	240	ns
DYO "H" delay time	DYO	t_{DDH}		-	140	250	ns
DYO "L" delay time		t_{DDL}		-	140	250	ns

Notes: 1. The open timing is valid in master mode.
2. Every timing is specified on the basis of 20% and 80% of V_{DD}.

(5) Reset timing



Output timing

V_{DD} = 5.0 V ±10%, Ta = -40 to +85°C

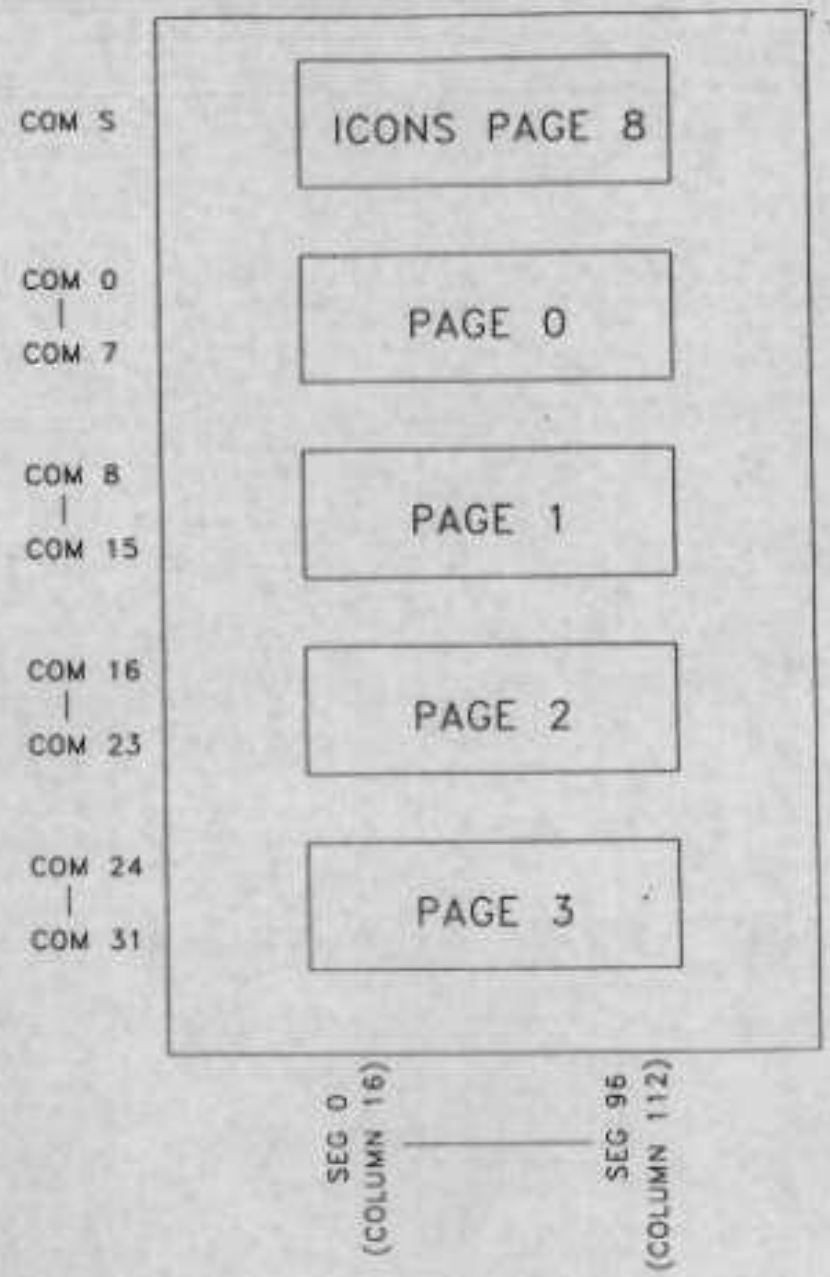
Parameter	Signal	Symbol	Condition	Min.	Typ.	Max.	Unit
Reset time		t_R		0.5	-	-	μs
Reset low pulse width	RES	t_{RW}		0.5	-	-	μs

V_{DD} = 2.7 V to 4.5 V, Ta = -40 to +85°C

Parameter	Signal	Symbol	Condition	Min.	Typ.	Max.	Unit
Reset time		t_R		1.0	-	-	μs
Reset low pulse width	RES	t_{RW}		1.0	-	-	μs

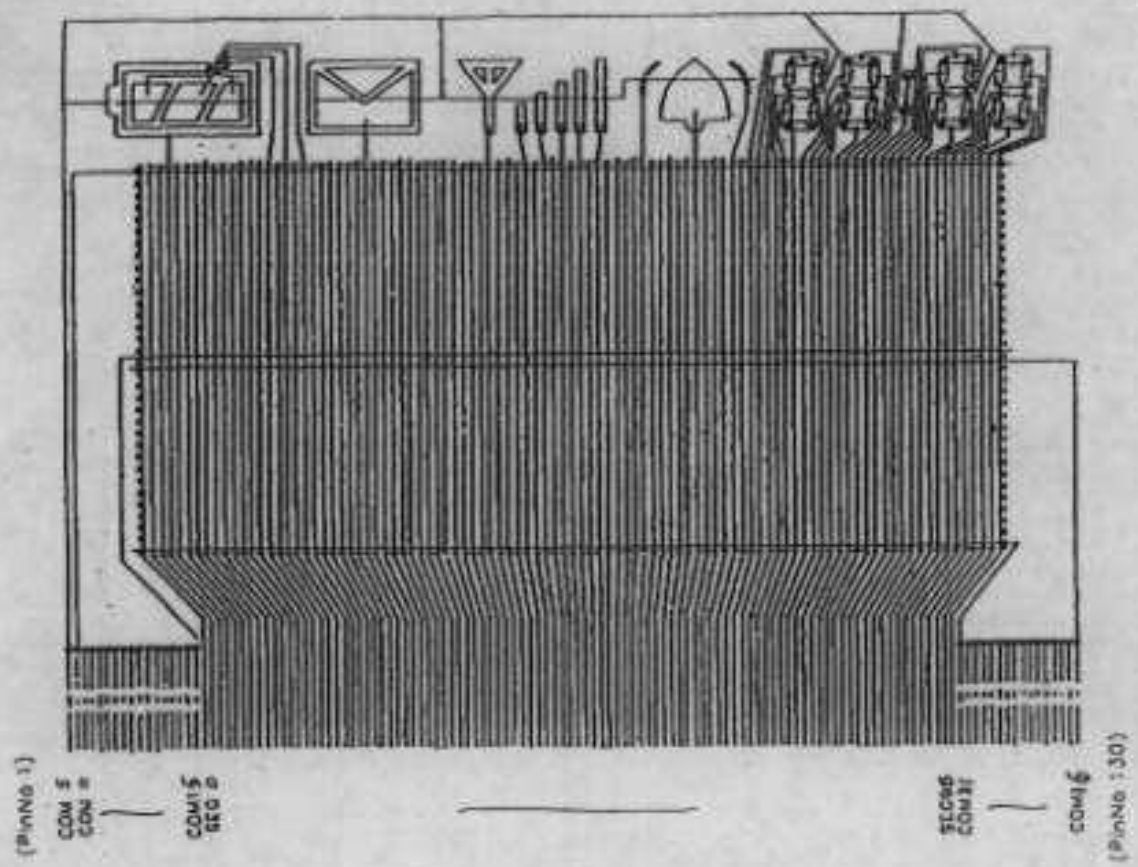
Note: The reset timing is specified on the basis of 20% and 80% of V_{DD}.

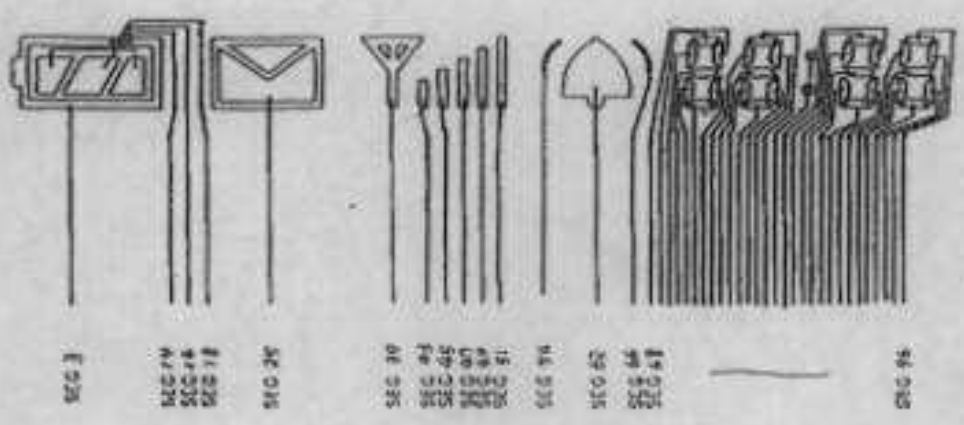
6. Page & column address setup



• "ADC SELECT" must be set 1 (DO)

7 LCD LAYOUT

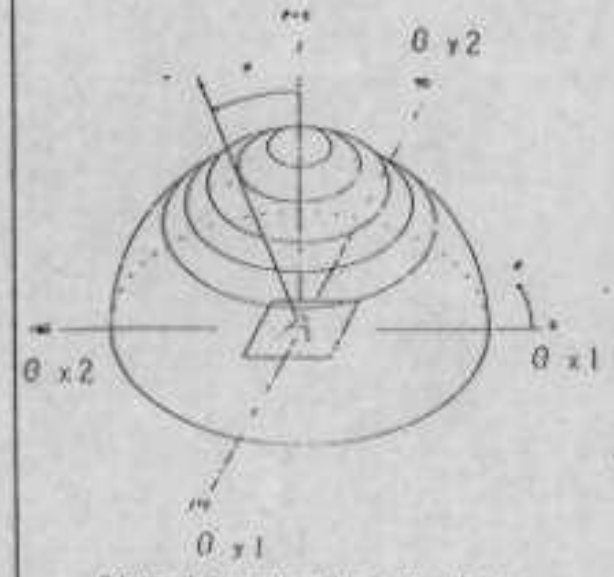




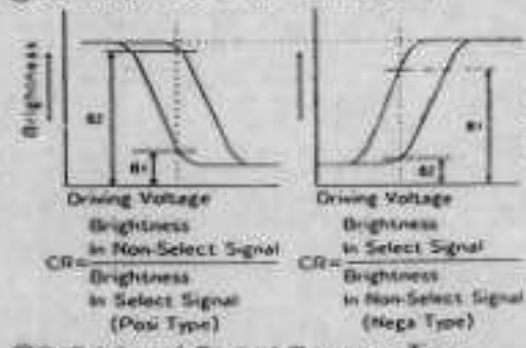
8. Optical characteristics

Prameter	Symbol	Temperature (℃)	Standard			Unit
			Min	Typ	Max	
Driving Voltage Vdd-Vlcd	Vop	-20	7.1	7.5	7.9	V
		25	6.3	6.7	7.1	
		70	5.4	5.8	6.2	
Response time	Tr	0	--	500	800	ms
		25		150	300	
	Tf	0		1100	1700	
		25		300	500	
frequency	Ff			64		Hz
Viewing angle range	θ y1	25	-30			Degree
	θ y2		30			
	θ x1		30			
	θ x2		-30			
Contrast	K	25		3		

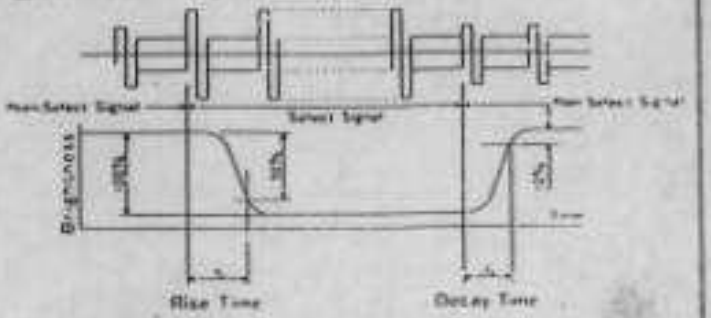
Ⓐ Definition of Viewing Angle θ and φ



Ⓑ Definition of Contrast Ratio (CR)



Ⓒ Definition of Optical Response Time



■ 9.LED Backlight characteristics

10-1.Maximum ratings

I t e m	Symbol	Condition	Min.	Max.	Unit
Forward current	If	Ta:25℃	—	200	mA
Reverse voltage	Vr	Ta:25℃	—	4	V
Power dissipation	Po	Ta:25℃	—	0.46	W
Operating temperature	Topr	—	-20	70	℃
Storage temperature	Tstg	—	-40	80	℃

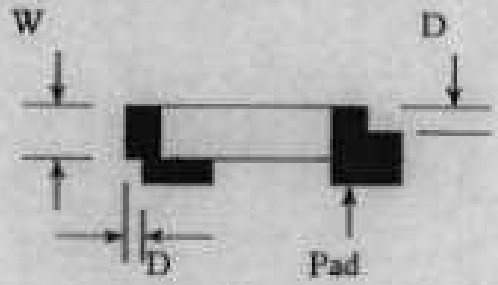
10-2.Electrical characteristics Ta=25℃

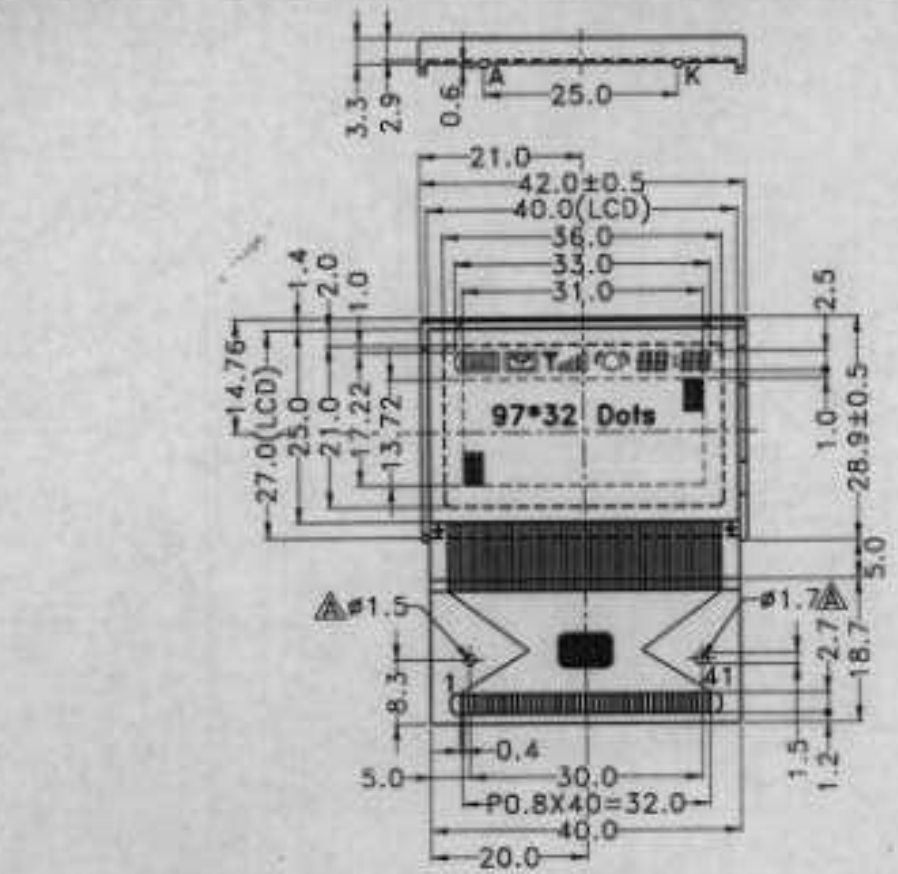
I t e m	Symbol	Condition	Min.	Typ	Max.	Unit
Forward voltage	Vf	If:80 mA	—	2.1	2.3	V
Reverse current	Ir	VR: 4 V	—	—	0.2	mA
Luminous intensity	Iv	If:80 mA	—	9	—	cd/㎡
Wavelength	λp	If:80 mA	—	570	—	nm
Color	Yellow Green					

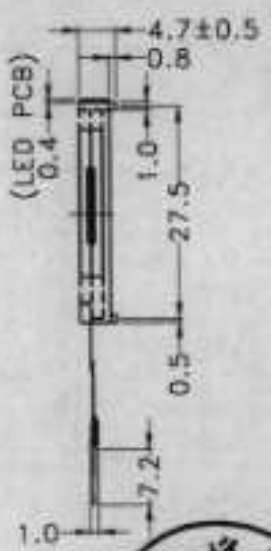
Out Going Inspection Specification

5-1. Inspection Standard : MIL-STD-105E Table Normal Inspection Single Sampling Level II .
5-2. Defect Level : Major Defect AQL 1.0 ; Minor Defect AQL 2.5 .
5-3. Equipment : Gauge . MIL-STD . Powertip Tester . Sample .
5-4. Specification :

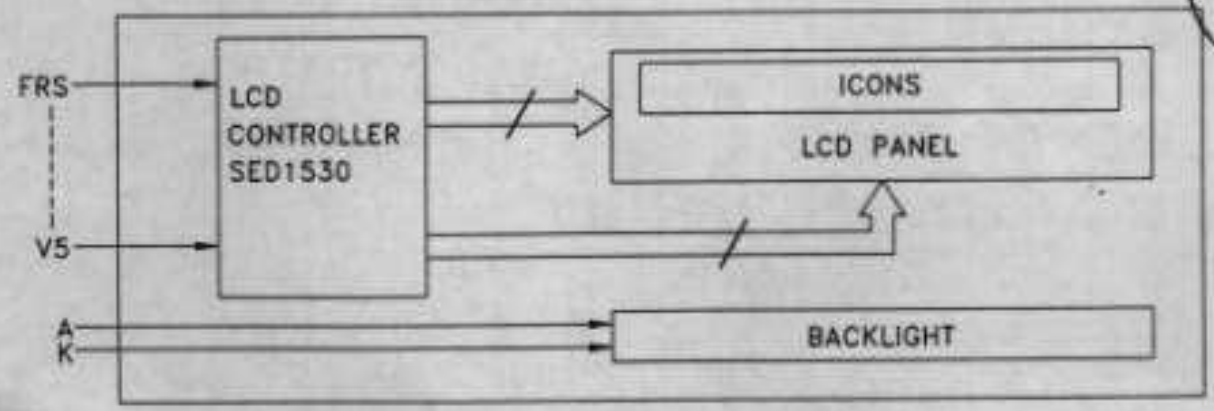
NO	Item	Specification	Judge	Level
1	Part Number	Inconsistent with the P/N on the flow chart of production	N.G.	Major
2	Quantity	Inconsistent Q'TY with the flow chart of production	N.G.	Major
3	Electronic characteristics A=(L + W) ÷ 2	Display short	N.G.	Major
		Missing line	N.G.	Major
		Dot missing A > 1/2 Dot size	N.G.	Major
		No function	N.G.	Major
		Out put data error	N.G.	Major
4	Appearance A=(L + W) ÷ 2	Material difference with flow chart	N.G.	Major
		LCD Assembled in opposite direction	N.G.	Major
		Bezel assembled in opposite direction	N.G.	Major
		Shadow within LCD V/A + 1.0 mm	N.G.	Major
	Dirty particle (Include scratch . bubble)	Dirty particle A > 0.4 mm	N.G.	Minor
		Dirty particle length > 3.0mm And 0.01mm < Width ≦ 0.05mm (Width > 0.05mm Measure by area)	N.G.	Minor
		Without protective film	N.G.	Minor
		Conductive rubber over bezel	N.G.	Minor
5	PCB Appearance A=(L + W) ÷ 2	Burned PCB	N.G.	Major
		Green paint stripped & visible circuit A > 1.0mm (Finish coat not counted in)	N.G.	Minor
		A particle across the circuit	N.G	Minor
		Circuit split > 1/2 Circuit width	N.G	Minor
		Any circuit risen	N.G	Minor
		0.2mm < Tin ball area A ≦ 0.4mm And Q'TY > 4 Pieces	N.G	Minor
		Tin ball area A > 0.4mm	N.G	Minor

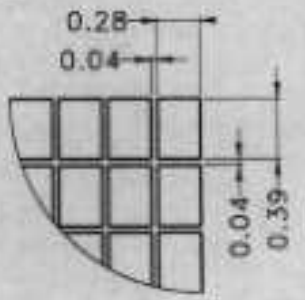
NO	Item	Specification	Judge	Level
6	Molding appearance A=(L + W) ÷ 2	Too soft : Shape by touch changed	N.G.	Major
		Insufficient epoxy : IC circuit or IC pad visible	N.G.	Minor
		Excessive epoxy : Diameter > 20mm Or High > 2.5mm	N.G.	Minor
		Pin hole through to IC and A > 0.2mm	N.G.	Minor
7	Bezel appearance A=(L + W) ÷ 2	Angle between frame and TAB > 45° +10°	N.G.	Minor
		Electroplate strip A > 1.0mm (Top view only)	N.G.	Minor
		Rust (Top view only)	N.G.	Minor
		Crack	N.G.	Minor
8	Backlight electric characteristics A=(L + W) ÷ 2	Error backlight color	N.G.	Major
		No function	N.G.	Major
		Any LED dot no function	N.G.	Major
		PIN soldering without tin A > 1/2 solder pad	N.G.	Minor
		Solder PIN high > 1.5mm	N.G.	Minor
9	LCD Appearance A=(L + W) ÷ 2	Polarize rise over V/A	N.G.	Minor
		Rainbow A > 1/3 bezel V/A	N.G.	Minor
10	Assembly parts A=(L + W) ÷ 2	Components mark unclearly	N.G.	Minor
		Components' distance more than 0.7mm firm the PCB	N.G.	Minor
		Error position not in center D > 1/2W 	N.G.	Minor
		Non- solder area > Twice solder area	N.G.	Minor
		Flux area A > 1/3 solder area	N.G.	Minor
		Component broken	N.G.	Minor





PIN NO.	SIGNAL	PIN NO.	SIGNAL
1	N.C	21	D3
2	FRS	22	D4
3	FR	23	D5
4	DYO	24	D6
5	CL	25	D7
6	$\overline{DOF}$	26	Vss
7	VS1	27	Vout
8	M/S	28	CAP3-
9	/RES	29	CAP1+
10	P/S	30	CAP1-
11	/CS1	31	CAP2+
12	CS2	32	CAP2-
13	C86	33	V5
14	A0	34	VR
15	/WR	35	Vdd
16	/RD	36	V1
17	Vdd	37	V2
18	D0	38	V3
19	D1	39	V4
20	D2	40	V5
		41	N.C





The tolerance unless classified ±0.3mm

SCALE:20/1

POWERTIP TECHNOLOG	
SCALE: 1/1	MODEL NAME PG 9732LRF-BE3-
UNIT: mm	TITLE COUNTER DRAWING
EDI: A / PAGE: 1/1	DRAWN NO. PG-97007-001
APPROVED	CHECKER