PT4301
Low Power High Sensitivity 315/434MHz OOK/ASK Superheterodyne Receiver

DESCRIPTION

The PT4301 is a very low power and highly sensitive single chip OOK/ASK super-heterodyne receiver for the 315MHz and 434MHz frequency bands that offers a high level of integration and requires only a few external components. The PT4301 consists of a low-noise amplifier (LNA), an image-rejection mixer, an on-chip phase-locked loop (PLL) with integrated voltage-controlled oscillator (VCO) and loop filter, a 10.7MHz intermediate frequency (IF) limiting amplifier stage with received-signal-strength indicator (RSSI), and analog baseband data recovery circuitry (data filter, peak detector, and data slicer). The PT4301 also implements a discrete one-step automatic gain control (AGC) that reduces the LNA gain by 20dB when the RF input signal is greater than -47dBm. The PT4301 is available in a 24-pin SSOP package.

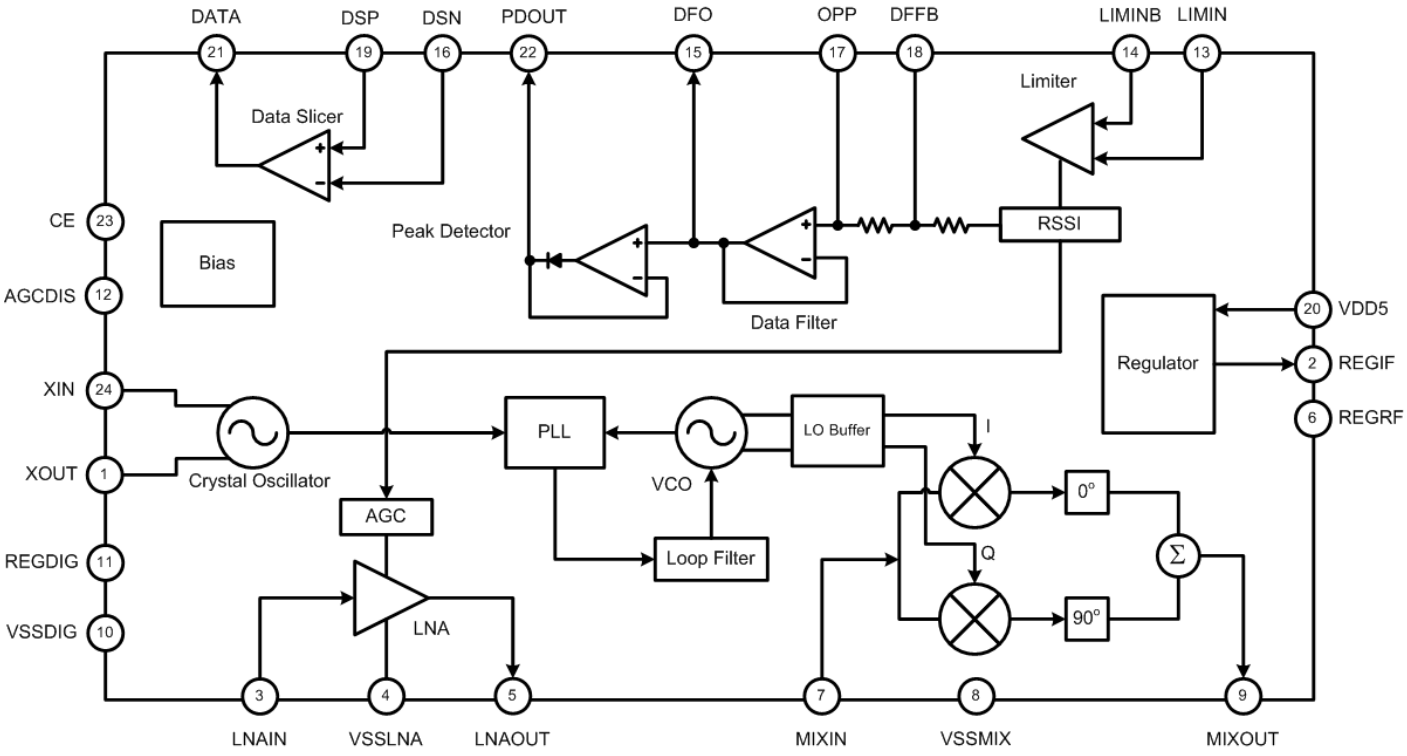
FEATURES

- Low current consumption (5mA fully active mode at 315MHz)
- 2.4V to 5.5V supply voltage operation range
- Optimized for 315MHz or 434MHz ISM Band
- On-chip image-rejection function
- High dynamic range with on-chip AGC
- Low power down mode current (<1μA)
- High sensitivity of -114dBm (315MHz, 2Kb/s AM 99%
  square-wave modulation)
- 24-pin SSOP package

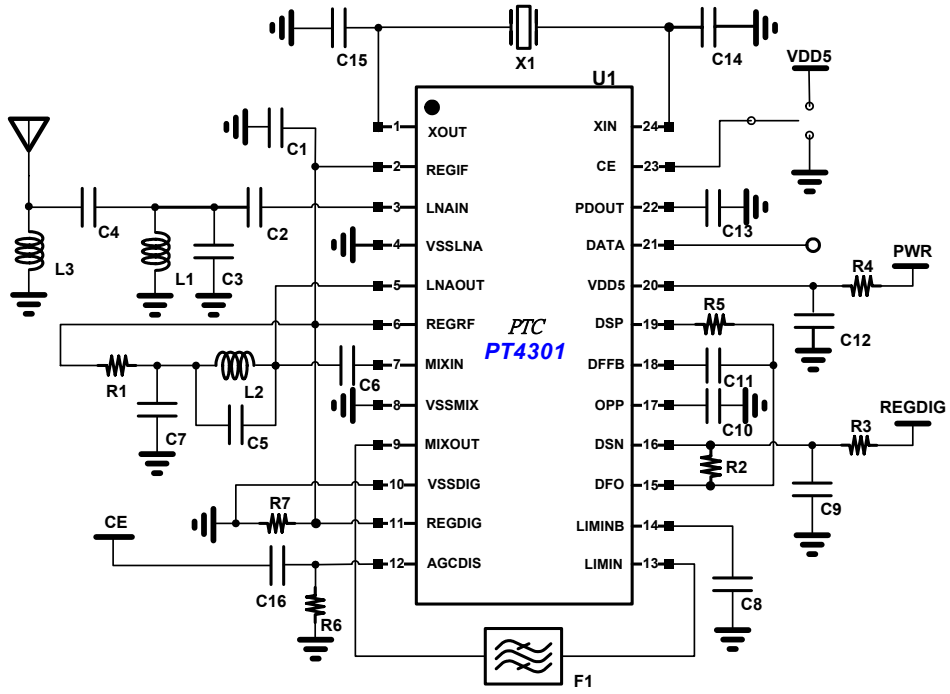
APPLICATIONS

- Remote keyless entry (RKE) systems
- Remote control systems including garage door and gate openers
- Alarm and security systems
- Wireless sensors

BLOCK DIAGRAM



APPLICATION CIRCUIT



BILL OF MATERIALS

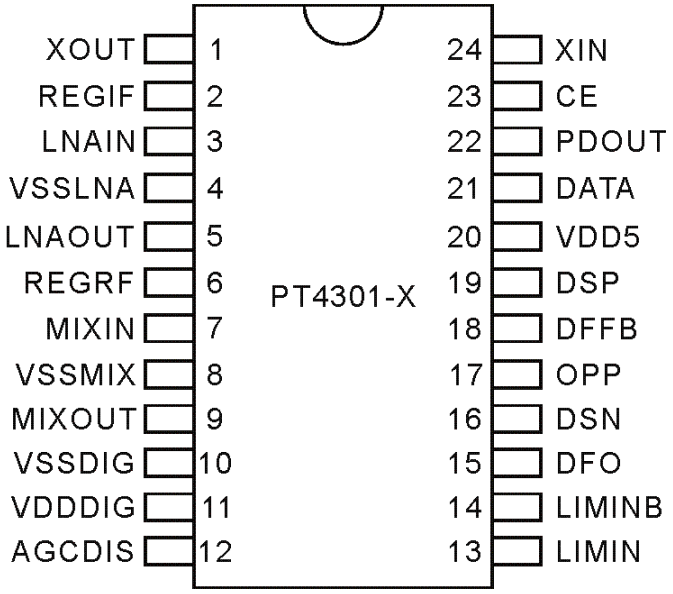
Component	Value		Unit	Description
	315MHz	434MHz		
R1, R4	10	10	Ω	Power supply de-coupling resistors (option)
R2	27K	27K	Ω	Data filter to data slicer interface resistor
R3	8.2M	8.2M	Ω	Data slicer threshold adjustment (option)
R5	220K	220K	Ω	Data filter to data slicer interface resistor
R6	100K	100K	Ω	AGC disable
R7	5.6K	5.6K	Ω	REGDIS discharge resistor (option)
L1	68n	39n	H	LNA input matching, coil inductor
L2	47n	27n	H	LNA output matching
L3	39n	27n	H	Antenna ESD protection, coil inductor (option)
C1[Note1] ,C7, C12	100n	100n	F	Power supply de-coupling resistors
C2	10p	10p	F	LNA input matching
C3	-	-	F	LNA input matching (option)
C4	1.8p	1.2p	F	LNA input matching
C5	-	-	F	LNA output matching (option)
C6	100p	100p	F	LNA to mixer interface capacitor
C8	1.5n	1.5n	F	IF amplifier de-coupling capacitor
C9	470n	470n	F	Data slicer threshold charge capacitor
C10	390p	390p	F	Data filter capacitor
C11	1.2n	1.2n	F	Data filter capacitor
C13	-	-	F	Peak mode charge capacitor (option)
C14, C15	27p	27p	F	Crystal oscillator frequency fine tune capacitors
C16	100n	100n	F	AGC high gain mode quick start capacitor
F1[Note2]	10.7	10.7	MHz	IF filter
X1	9.509	13.226	MHz	Reference crystal oscillator
U1	PT4301 IC	PT4301 IC	-	Receiver chip

Notes:
1. C1 could be separated into three de-coupling capacitors and connect them against the three VDD pins as close as possible.
2. F1 is the 10.7MHz ceramic filter. The recommended part number is Murata SFELA10M7HA00-B0.

ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT4301-X	24 Pins, SSOP, 150mil	PT4301-X

PIN CONFIGURATION



PIN DESCRIPTION

Pin Name	I/O	Description	Pin No.
XOUT	O	Crystal oscillator output	1
REGIF	P	Supply voltage for IF portion	2
LNAIN	I	LNA input	3
VSSLNA	G	Ground for LNA	4
LNAOUT	O	LNA output	5
REGRF	P	Supply voltage for RF portion	6
MIXIN	I	Mixer input	7
VSSMIX	G	Ground for image-rejection mixer	8
MIXOUT	O	Mixer output	9
VSSDIG	G	Ground for LO and digital portions	10
REGDIG	P	Supply voltage for LO and digital portions	11
AGCDIS	I	AGC control pin. Pull high (connect to VDD5) to disable AGC	12
LIMIN	I	Limiting amplifier input	13
LIMINB	I	Limiter amplifier de-coupling input	14
DFO	O	Data filter output	15
DSN	I	Negative data slicer input	16
OPP	I	Non-inverting op-amp input for Sallen-Key data filter	17
DFFB	I/O	Data filter feedback node	18
DSP	I	Positive data slicer input	19
VDD5	P	5V supply voltage	20
DATA	O	Data output	21
PDOUT	O	Peak detector output	22
CE	I	Chip enable pin. Pull high (connect to VDD5) to power on the chip	23
XIN	I	Crystal oscillator input	24

Note: Pin 13 and Pin 14 are identical pins. Users can choose either pin as the limiting amplifier input and treat the other pin as the de-coupling input.

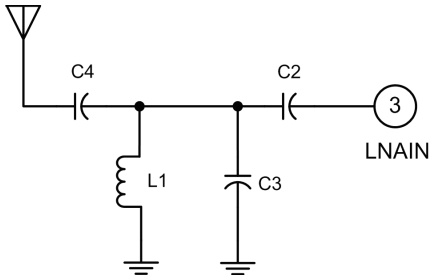
FUNCTION DESCRIPTION

The PT4301 CMOS superheterodyne receiver achieves both low power consumption and high sensitivity and functions as a complete receive chain from antenna input to digital data output. Depending upon the component selection, data rates as high as 50Kb/s may be achieved at both 315 and 434MHz frequency bands.

LOW NOISE AMPLIFIER (LNA)

The LNA is an on-chip cascade amplifier with a power gain of 16dB and a noise figure of approximately 3dB. The gain is determined by external matching networks in front of the LNA and between the LNA output and the mixer input.

Examples of the input matching network and the input impedance of the PT4301 for 315/434MHz bands are shown in Figure 1. The component values given in the table following the application circuit shown in page 2 are nominal values only. For a particular PCB layout, the user may be required to make component adjustments in order to achieve highest sensitivity.



Frequency(MHz)	LNA Input Impedance (Pin 3) Normalized to 50Ω
315	2.45-j138.4
433.92	3.05-j194.85

Figure 1. LNA Input Matching Circuit and Input Impedance of PT4301

The LNA output of PT4301 externally connects to the mixer stage. For the interface between the LNA and mixer, the coupling capacitor should be as close to the PT4301 pins as possible, with the bias inductor being further away. The value of the inductor may be changed to compensate for trace inductance. For obtaining better LNA gain, it is recommended to add a capacitor in parallel with this inductor to implement a resonant tank at the desired frequency as shown in Figure 2. Note that the LNA might self-oscillate and degrade the receiver sensitivity if a large output inductor value is chosen. An alternative matching method is to replace the parallel capacitor with a 330Ω to 1KΩ resistor, which would reduce the resonant tank Q (quality factor) to avoid the self-oscillation.

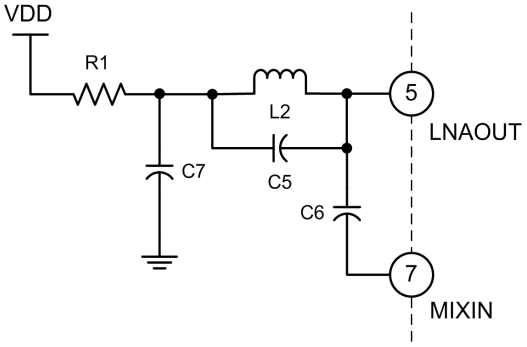


Figure 2. LNA Output Matching Circuit

The LNA incorporates gain control circuitry. When the RSSI voltage exceeds a threshold reference value corresponding to an RF input level of approximately -47dBm, the AGC switches on the LNA gain reduction resistor. The loading resistor reduces the LNA gain by 20dB, thereby reducing the RSSI output by approximately 260mV. The threshold reference voltage which is compared with the RSSI voltage to determine the gain state of the LNA is also reduced. The LNA resumes high-gain mode when the RSSI voltage drops below this lower threshold voltage corresponding to approximately -63dBm RF input. The AGC incorporates an additional protection mechanism (delay timer of $2^{20} \times T_{REF}$ seconds) to prevent immediate resetting of the LNA back to the high-gain state during reception of a “space” for OOK/ASK modulation.

MIXER

A special feature of the PT4301 is its integrated double-balanced image-rejection mixer, which eliminates the need for a costly front-end SAW filter for many applications. The advantages of not using a SAW filter include simplified antenna matching, less board space, and lower BOM cost. The mixer cell is a pair of double-balanced mixers that perform an IQ down-conversion of the RF input to the 10.7MHz IF with low-side injection (i.e. $f_{LO}=f_{RF}-f_{IF}$). The image-rejection circuit then combines these signals to achieve a typical 35dB of image-rejection ratio. Low-side injection is required since high-side injection is not possible due to the on-chip image rejection. The IF output is driven by a source follower biased to create a driving impedance of 330Ω to interface with an off-chip 330Ω ceramic IF filter. The voltage-conversion gain of the image-rejection mixer is approximately 18dB at 315MHz and 15dB at 433.92MHz with a 330Ω load.

PHASE-LOCKED LOOP (PLL)

The PT4301 utilizes a fixed divided-by-32 PLL to generate the receiver LO. The PLL consists of the voltage-controlled oscillator (VCO), crystal oscillator, asynchronous÷32 divider, charge pump, loop filter and phase-frequency detector (PFD). All these components are integrated on-chip. The PFD compares two signals and produces an error signal which is proportional to the difference between the input phases. The error signal passes through a loop filter with an approximately 400KHz bandwidth, and is used to control the VCO which generates an LO frequency. The VCO frequency is also fed through a frequency divider back to one input of the PFD, producing a feedback loop. Thus, the output is locked to the reference frequency at the other input, which is derived from a crystal oscillator (i.e. $f_{REF}=(f_{RF}-f_{IF})/32$). The block diagram below shows the basic elements of the PLL.

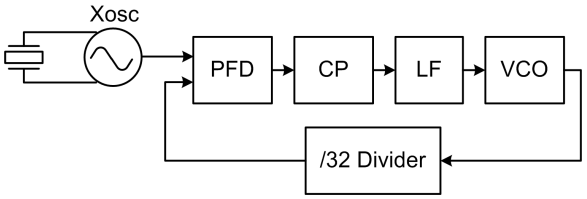


Figure 3. Phase-locked Loop in PT4301

To achieve an accurate frequency for the crystal oscillator, it is recommended to specify the suitable load capacitors, C14 and C15. Specifying the value of 27pF is acceptable. Choosing a lower value of crystal parallel equivalent capacitance, C_0=1.5pF is also a suitable, but this may increase the price of the crystal itself. Typically the value of C_0_max is 7.0pF.

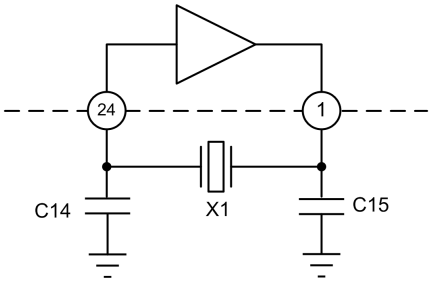


Figure 4. Crystal Oscillator Circuit

The reference oscillator frequency is close to 10.7 MHz intermediate frequency. It is necessary to avoid signal trace coupling between the reference oscillator and intermediate frequency. Otherwise, it would degrade receiver performance.

LIMITER/RSSI

The limiter is an AC coupled multi-stage amplifier with a cumulative gain of approximately 72dB that possesses a band-pass characteristic. The -3dB bandwidth of the limiter is around 12MHz. The limiter circuit also produces an RSSI voltage that is directly proportional to the input signal level with a slope of approximately 13mV/dB. The RSSI signal is used to demodulate ASK-modulated receive signals in the subsequent baseband circuitry. The RSSI output level has the dynamic range of approximately 80dB.

AUTOMATIC GAIN CONTROL (AGC)

The AGC circuitry monitors the RSSI voltage level. As described previously, when the RSSI voltage reaches a first value corresponding to an RF input level of approximately -47dBm, the AGC reduces the LNA gain by 20dB, thereby reducing the RSSI output by approximately 260mV. When the RSSI voltage drops below a level corresponding to an RF input of approximately -63dBm, the AGC sets the LNA back to high-gain mode.

Figure 5 shows the change of RSSI voltage versus RF input power. When the RSSI level increases and then exceeds 1.77V (RF input power rising), the AGC switches the LNA from high-gain mode to low-gain mode. As RSSI level decreases back to 1.16V (RF input power falling), the AGC switches the LNA from low-gain mode back to high-gain mode. The AGC has an additional protection mechanism (delay timer of $2^{20} \times T_{REF}$ seconds) when the LNA is reset back to the high-gain state.

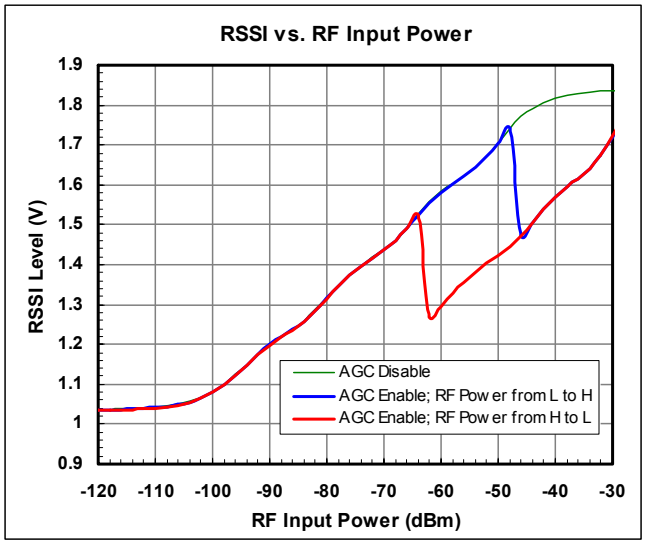


Figure 5. RSSI vs. RF Input Power

DATA FILTER

The data filter is implemented as a 2nd-order low-pass Sallen-Key filter as shown in Figure 6. The pole locations are set by the combination of two on-chip resistors and two external capacitors. Adjusting the value of the external capacitors changes the corner frequency to optimize for different data rates. The corner frequency should be set to approximately 1.5 times the highest expected data rate from the transmitter.

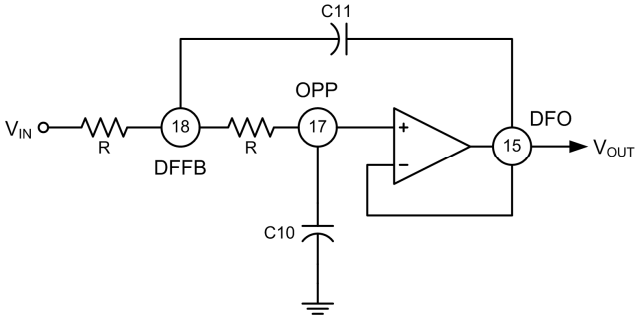


Figure 6. Ideal Sallen-Key Filter

Utilizing the on-board voltage follower and the two 100KΩ on-chip resistors, a 2nd-order Sallen-Key low pass data filter may be constructed by adding 2 external capacitors between pins 15 (DFO) and 18 (DFFB) and to pin 17 (OPP) as depicted in the Page 2. The following table shows the recommended values of the capacitors for different data rates.

Data Rate	C11 (pF)	C10 (pF)
<2Kb/s	1000	270
2Kb/s - 10Kb/s	470	100
10Kb/s - 20Kb/s	150	56
20Kb/s - 40Kb/s	56	15
>40Kb/s[Note]	15	4.7

Notes:
1. The maximum data rate of PT4301 is 50Kb/s
2. The component values may be different, which depend upon the data duty and codec pattern.

PEAK DETECTOR

The peak detector generates a DC voltage which is proportional to the peak value of the received data signal. An external R-C network is necessary. The peak detector input is connected to the data filter internally, and its output is connected to pin 16 (DSN) through the R-C network. This output may be used as an indicator of the received signal strength in wake-up circuits or used as a reference for data slicing. The time constant is calculated using the driving current of the op-amp in data filter, 100μA.

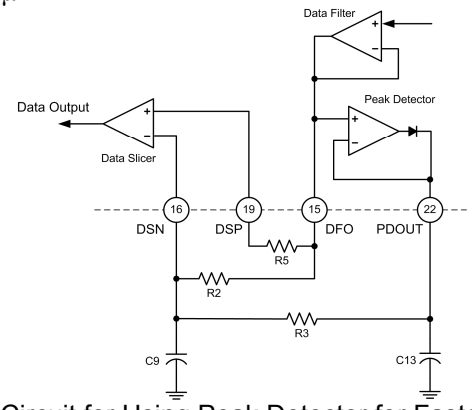


Figure 7. Circuit for Using Peak Detector for Faster Start-Up

DATA SLICER

The data slicer consists chiefly of a fast comparator, which allows for a maximum receive data rate of up to 50Kb/s. The maximum achievable data rate also depends upon the IF filter bandwidth. Both data slicer inputs are accessible off-chip to allow for easy adjustment of the slicing threshold. The output delivers a digital data signal (CMOS level) for subsequent circuits. The self-adjusting threshold on pin 16 (DSN) is generated by an R-C network or peak detector, depending upon the baseband coding scheme.
The suggested data slicer configuration is shown in Figure 8. The cut-off frequency of the R-C integrator must be set lower than the lowest frequency appearing in the data signal to minimize distortion in the output signal.

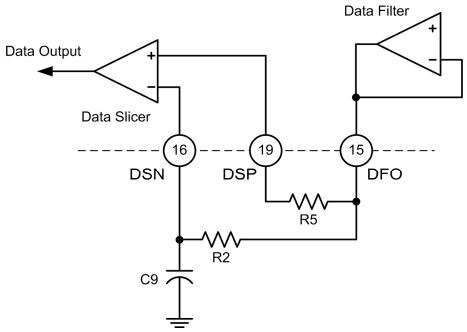


Figure 8. Circuit for Generating Data Slicer Threshold

DEMODULATION

With different circuit combinations, the PT4301 may utilize two demodulation modes, called “peak mode” and “average mode.”

PEAK MODE

In conjunction with an external RC filter (R3 and C13), the threshold voltage may be set at the peak detector output for comparison as shown in Figure 7. The demodulated data enters into a quasi-mute state as the RF input signal becomes very small (when there is no RF signal received or the RF signal is too small) and the DATA output remains mostly at a logic “HIGH” level. If the environment is very noisy, the R3 value may be enlarged to achieve better immunity against noise, but at the cost of less sensitivity.

AVERAGE MODE

When the “average mode” has been set as shown in Figure 8, the DATA output will exhibit a toggling behavior similar to random noise. In this mode, better sensitivity may be achieved, but noise immunity is worse than in “peak mode.”

SENSITIVITY AND SELECTIVITY

In digital radio systems, sensitivity is often defined as the lowest signal level at the receiver input that will achieve a specified bit error ratio (BER) at the output. The sensitivity of the PT4301 receiver, when used in the 434MHz application shown in Figure 9, is typically -106dBm (OOK modulated with 2Kb/s, 50% duty cycle square wave in average mode) to achieve a 0.1% BER. The input was matched for a 50Ω signal source. At 315MHz, -108dBm sensitivity is typically achievable.

The selectivity is governed by the response of the receiver front-end circuitry, the channel filter (off-chip 10.7MHz IF filter), and the data filter. Note the IF filter provides not only channel selectivity but also the interference rejection. Within the pass band of the receiver, no rejection for interfering signals is provided.

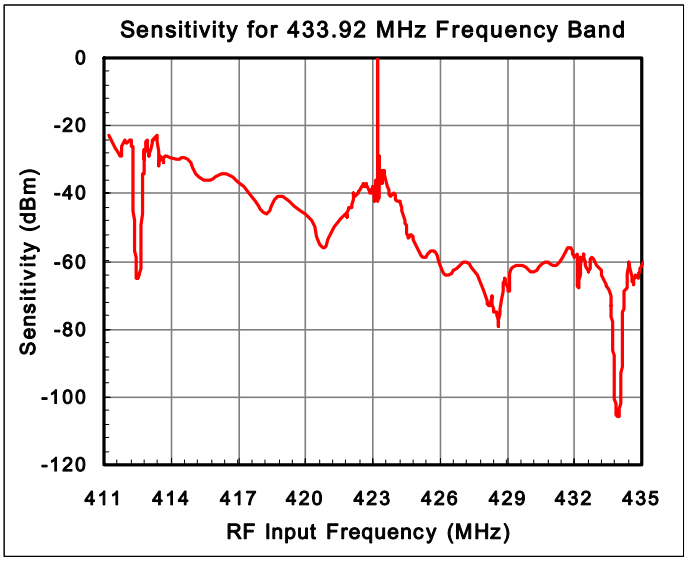


Figure 9. Sensitivity of PT4301

POWER-DOWN CONTROL

The chip enable (CE) pin controls the power on/off behavior of the PT4301. Connecting CE to "HIGH" sets the PT4301 to its normal operation mode; connecting CE to "LOW" sets the PT4301 to standby mode. The chip consumption current will be lower than 1μA in standby mode. Once enabled, the PT4301 requires <10ms to recover received data.

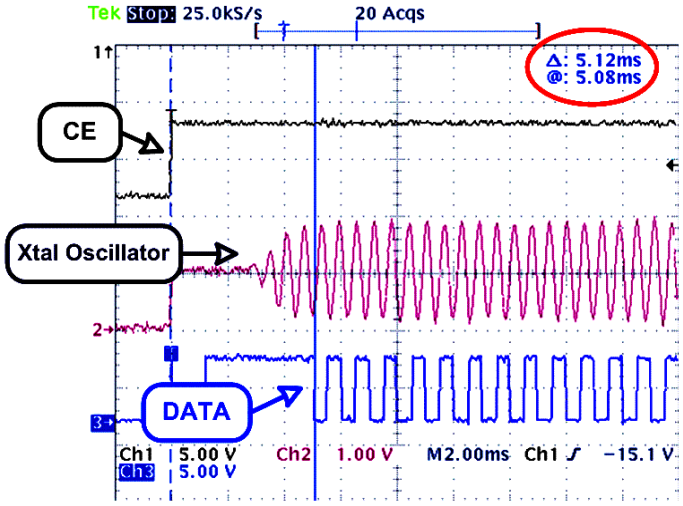


Figure 10. Timing plot of PT4301 Chip Enable under 27°C & -80dBm Input Power Test Condition.

ANTENNA DESIGN

For a $\lambda/4$ dipole antenna and operating frequency, f (in MHz), the required antenna length, L (in cm), may be calculated by using the formula

$$L = \frac{7132}{f}$$

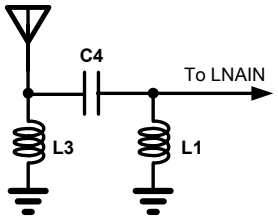
For example, if the frequency is 315MHz, then the length of a $\lambda/4$ antenna is 22.6cm. If the calculated antenna length is too long for the application, then it may be reduced to $\lambda/8$, $\lambda/16$, etc. without degrading the input return loss. However, the RF input matching circuit may need to be re-optimized. Note that in general, the shorter the antenna, the worse the receiver sensitivity and the shorter the detection distance. Usually, when designing a $\lambda/4$ dipole antenna, it is better to use a single conductive wire (diameter about 0.8mm to 1.6mm) rather than a multiple core wire.

If the antenna is printed on the PCB, ensure there is neither any component nor ground plane underneath the antenna on the backside of PCB. For an FR4 PCB (ε_r=4.7) and a strip-width of 30mil, the length of the antenna, L (in cm), is calculated by

$$L = \frac{c}{4 \times f \times \sqrt{\varepsilon_r}}$$ where "c" is the speed of light (3 x10^{10}cm/s)

ANTENNA PART ESD PROTECTION

PT4301 IC provides the ESD level (Human Body Mode) better than 3KV at LNAIN pin. However, the higher ESD protection level would be required in system level for some applications. The extra ESD protection level could rely on the external components. Changing L1 from SMD type to coil type could enhance ESD protection level of around 1KV, and adding a shunt coil inductor L3 in the front of C4 to gain more ESD protection enhancements.



RF Frequency f_{RF}	Suggestion Value of L3
315MHz	39nH
340MHz	39nH
390MHz	33nH
433.92MHz	27nH

Figure 11. Antenna ESD Protection Inductor of PT4301

PCB LAYOUT CONSIDERATION

Proper PCB layout is extremely critical in achieving good RF performance. At the very least, using a two-layer PCB is strongly recommended, so that one layer may incorporate a continuous ground plane. A large number of via holes should connect the ground plane areas between the top and bottom layers. Note that if the PCB design incorporates a printed loop antenna, there should be no ground plane beneath the antenna.

Within the PT4301, the power supply rails of the LNA and others blocks should be separated for improving the isolation and minimizing the noise coupling effects. Careful consideration must also be paid to the supply power and ground at the board level. The larger ground area plane should be placed as close as possible to all the VSS pins. To reduce supply bus noise coupling, the power supply trace should be incorporate series-R, shunt-C filtering as shown in Figure 12.

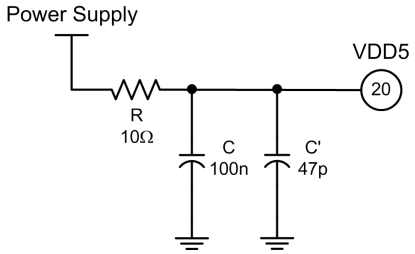


Figure 12. Noise Rejection Filter for Power Bus

ABSOLUTE MAXIMUM RATINGS

(V_{SS}=0V)

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD5}	V_{SS}-0.3 to V_{SS}+6.0	V
Operating temperature range	Topr	-40 to +85	℃
Storage temperature range	Tstg	-55 to +125	℃
Soldering temperature	T_{SLD}	255	℃
Soldering time	t_{SLD}	10	s

RECOMMENDED OPERATING CONDITIONS

(V_{SS}=0V)

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Supply voltage range	V_{DD5}	2.4	5.0	5.5	V
Operating temperature	T_A	-40	27	85	℃

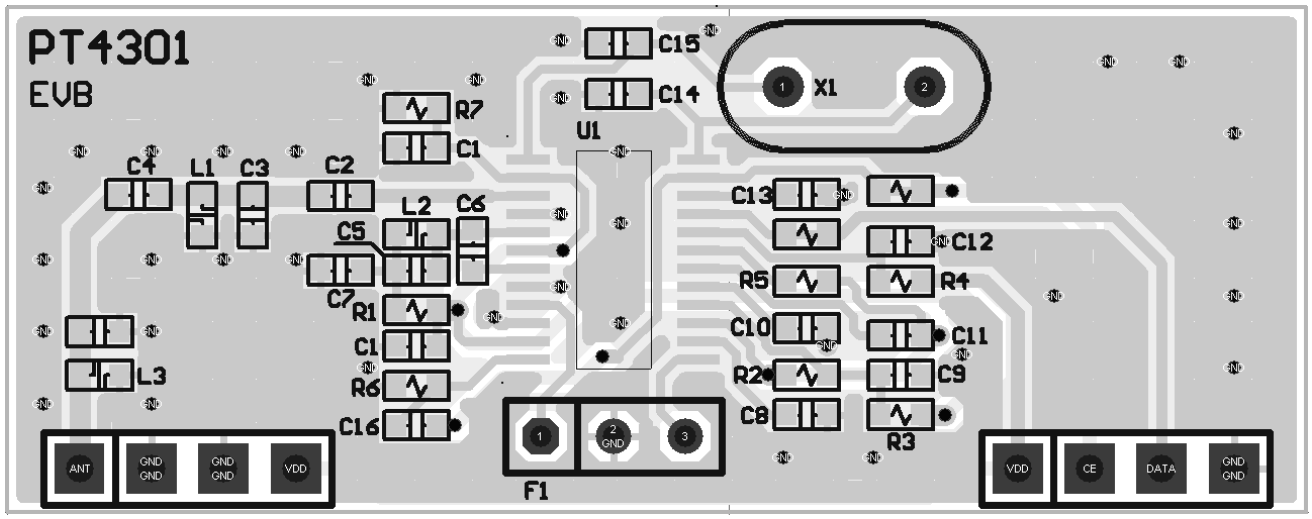
ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, V_{DD5}=5.0V, V_{SS}=0V, CE="HIGH", Temp=27℃)

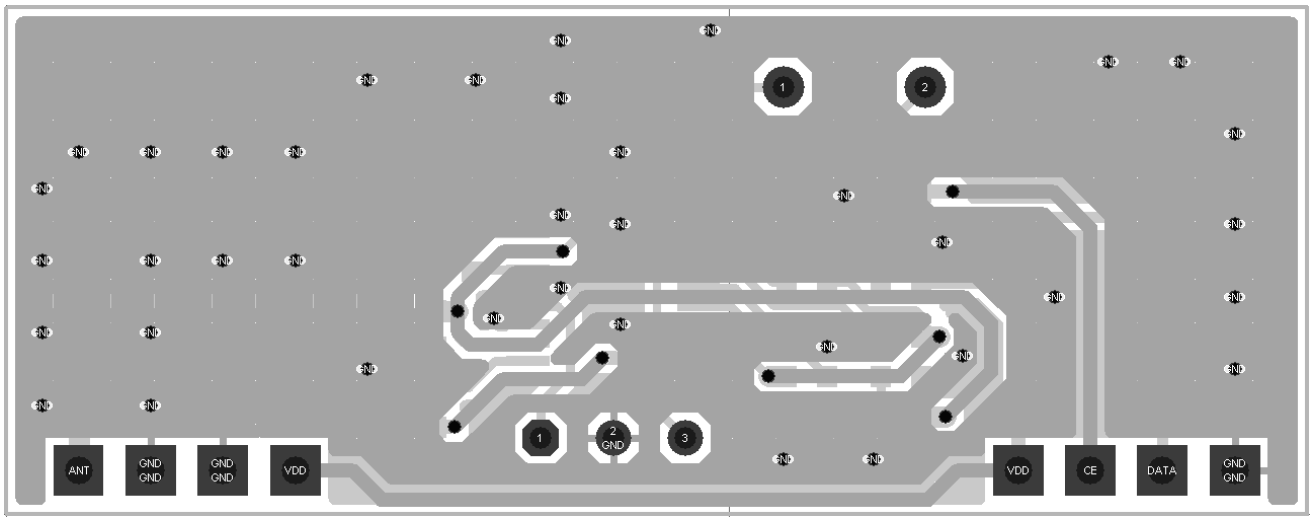
Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
General Characteristics						
Frequency range	f_{RF}		250		500	MHz
Maximum receiver input level	$P_{RF,MAX}$		-25	-20		dBm
Sensitivity[Note1]	S_{IN}	ASK[Note2], peak power level @315MHz		-114	-112	dBm
		OOK, peak power level @315MHz		-108	-106	dBm
		ASK, peak power level @434MHz		-112	-110	dBm
		OOK, peak power level @434MHz		-106	-104	dBm
Data rate[Note3]	D_{Rate}			2	50	Kb/s
Image rejection ratio	IMR		25	35		dB
LO leakage	L_{LO}	Measured at RF input			-80	dBm
System start-up time	$T_{start-up}$	RF input power=-60dBm Temp=27℃			10	ms
Power Supply						
Supply voltage	V_{DD5}	Connect the supply voltage to VDD5 pin only	2.4	5.0	5.5	V
Consumption DC current	I_{DD5}	CE="HIGH"@315MHz		5.0	5.5	mA
		CE="HIGH"@434MHz		5.3	5.9	mA
Standby DC current	$I_{stand-by}$	CE="LOW"			1.0	μA
LNA						
Power gain	G_{LNA}	Matched to 50Ω@315MHz	13	16	20	dB
		Matched to 50Ω@434MHz	12	15	18	dB
Noise figure	NF_{LNA}	Matched to 50Ω		3	3.6	dB
Input third-order intermodulation intercept point	$IIP3_{LNA}$	Matched to 50Ω	-20			dBm
Auto Gain Control (AGC)[Note4]						
AGC hysteresis	H_{AGC}			16		dB
LNA voltage gain reduction	G_{Red}			20	30	dB
AGC delay time	DY_{AGC}	$T_{REF}=1/f_{REF}$		$2^{20}\times T_{REF}$		s
Down-conversion Mixer						
Conversion voltage gain	G_{MIX}	@315MHz	15	18	22	dB
		@434MHz	12	15	18	dB
Input third-order intermodulation intercept point	$IIP3_{MIX}$		-18			dBm
Output impedance	$Z_{OUT,MIX}$			330		Ω
PLL						
Reference frequency	f_{REF}		6		16	MHz
VCO frequency range	f_{VCO}		220		550	MHz
Limiter Amplifier and RSSI						
IF frequency	f_{IF}			10.7		MHz
Input impedance	$Z_{IN,LIM}$			330		Ω
RSSI dynamic range	DR_{RSSI}			80		dB
RSSI gain	SL_{RSSI}			13		mV/dB

Notes:
1. BER=1^{e-3}, data rate=2Kb/s.
2. AM 99% square-wave modulation.
3. The selection of data rate depends upon the component values use for the data filter, peak detector, and slicer.
4. AGC hysteresis and LNA gain reduction depend upon the gain setting and matching circuits of the LNA. The AGC delay time depends upon the PLL reference frequency.

TEST BOARD LAYOUT



<Top Side>

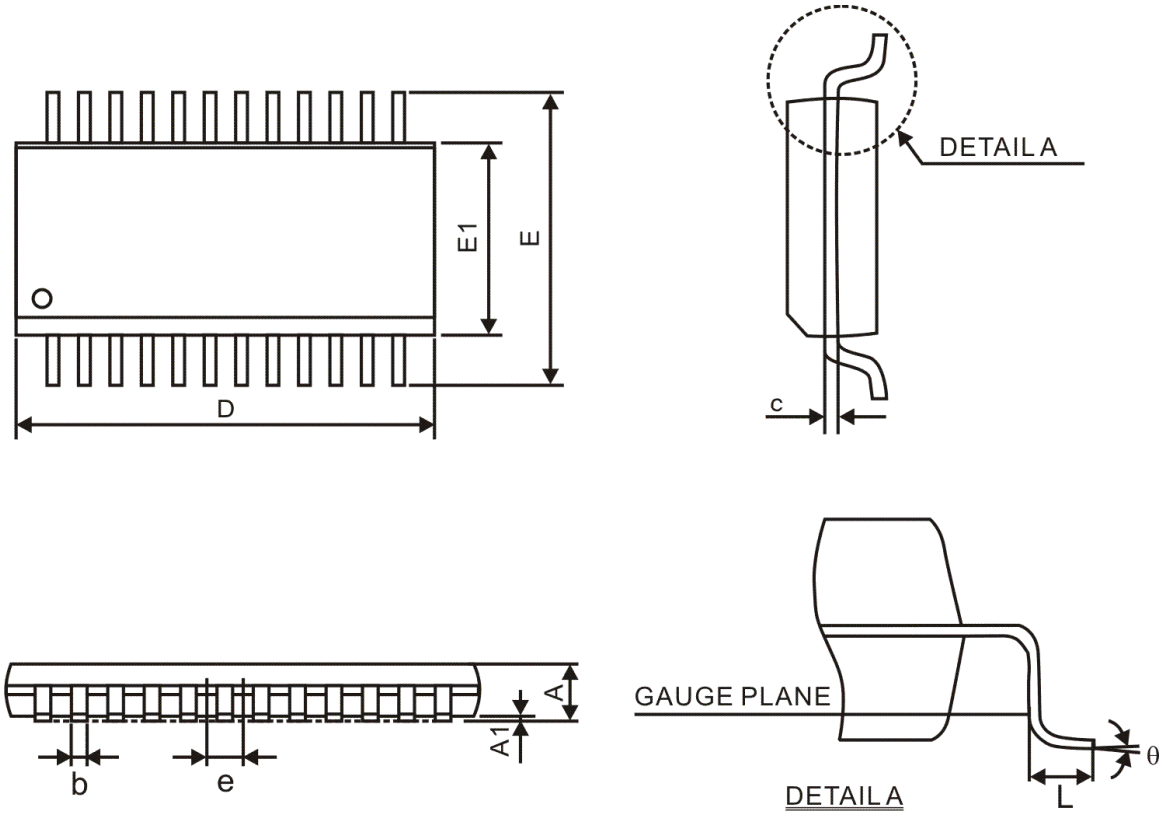


<Bottom Side>

Figure 12. Example of Test Board Layout

PACKAGE INFORMATION

24 PINS, SSOP, 150MIL



Symbol	Min.	Nom.	Max.
A	-	-	1.75
A1	0.10	-	0.25
b	0.20	-	0.30
c	0.10	-	0.25
D	8.66 BSC		
E	5.99 BSC		
E1	3.91 BSC		
e	0.635 BSC		
L	0.41	-	1.27
θ	0°	-	8°

Notes:
1. Refer to JEDEC MO-137AE.
2. All dimensions are in millimeter.

IMPORTANT NOTICE

Princeton Technology Corporation (PTC) reserves the right to make corrections, modifications, enhancements, improvements, and other changes to its products and to discontinue any product without notice at any time.
PTC cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a PTC product. No circuit patent licenses are implied.

Princeton Technology Corp.
2F, 233-1, Baociao Road,
Sindian, Taipei 23145, Taiwan
Tel: 886-2-66296288
Fax: 886-2-29174598
http://www.princeton.com.tw