32-bit ARM® Cortex™-M3 Microcontroller,
up to 32 KB flash and 8 KB SRAM with 1 MSPS ADC, USART, SPI, I^2C.

HT32F1251/51B/52/53 Series
User Manual

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1 Introduction

Overview

This user manual provides detailed information including how to use the HT32F125x series of devices, system and bus architecture, memory organization and peripheral instructions. The target audiences for this document are software developers, application developers and hardware developers. For more information regarding pin assignment, package and electrical characteristics, please refer to the HT32F125x series datasheet.

The Holtek HT32F125x series of devices are high performance, low power consumption 32-bit microcontrollers based on the ARM® Cortex™-M3 processor core. The Cortex™-M3 is a next-generation processor core which is tightly coupled with a Nested Vectored Interrupt Controller (NVIC), SysTick timer and advanced debug support.

The HT32F125x device operates at a frequency of up to 72 MHz with a Flash accelerator to obtain maximum efficiency. It provides up to 32 KB of embedded Flash memory for code/data storage and up to 8 KB of embedded SRAM memory for system operation and application program usage. A variety of peripherals, such as ADC, I^2C, USART, SPI, SW-DP (Serial Wire Debug Port), etc., are also implemented in this device series. Several power saving modes provide the flexibility for maximum optimisation between wakeup latency and power consumption, an especially important consideration in low power applications.

The above features make the HT32F125x device suitable for a wide range of applications, especially in areas such as white goods and application control, power monitor and alarm systems, consumer and handheld equipment, data logging applications and so on.

Features

- Core
  - 32-bit ARM® Cortex™-M3 processor core
  - Up to 72 MHz operation frequency
  - 1.25 DMIPS/MHz (Dhrystone 2.1)
  - Single-cycle multiplication and hardware division
  - Integrated Nested Vectored Interrupt Controller (NVIC)
  - 24-bit SysTick timer
- On-chip memory
  - 9 to 32 KB on-chip Flash memory for instruction/data and option storage
  - 2 to 8 KB on-chip SRAM
  - Supports several boot modes
- Flash Memory Controller
  - Flash accelerator for maximum efficiency
  - 32-bit word programming (ISP and IAP)
  - Flash protection capability to prevent illegal access
- Reset and Clock Control Units
  - Supply supervisor: Power On Reset (POR), Brown Out Detector (BOD) and Programmable Low Voltage Detector (LVD)
  - External 4 to 16 MHz crystal oscillator
  - External 32,768 Hz crystal oscillator
  - Internal 8MHz RC oscillator trimmed to 1% accuracy at 3.3 V operating voltage and 25ºC operating temperature.
  - Internal 32 kHz RC oscillator
  - Integrated system clock PLL
  - Independent clock gating bits for peripheral clock sources
- Power management
  - Single 3.3 V power supply - 2.7 V to 3.6 V
  - Integrated 1.8 V LDO regulator for core and peripheral power supply
  - V_{BAT} battery power supply for RTC and backup registers
  - Three power domains: 3.3V, 1.8V and Backup
  - Four power saving modes: Sleep, Deep-Sleep1, Deep-Sleep2, Power-Down
- ADC
  - 12-bit SAR ADC engine
  - Up to 1 Msps conversion rate - 1 μs at 56 MHz, 1.17 μs at 72 MHz
  - 8 external analog input channels
  - Supply voltage range: 2.7 V ~ 3.6 V
  - Conversion range: V_{SSA} ~ V_{DDA}
- Analog Operational Amplifier/Comparator
  - 2 Operational Amplifiers or 2 Comparator functions which are software configurable
  - Supply voltage range: 2.7 V ~ 3.6 V

- I/O ports
  - Up to 32 GPIOs
  - Port A and Port B are mapped as 16 external interrupts (EXTI)
  - Almost all I/O pins are 5 V-tolerant except for pins shared with analog inputs
- PWM Generation and Capture Timers
  - Two 16-bit General-Purpose Timers (GPTM)
  - Up to 4CHs PWM compare output or input capture input for each GPTM
  - External trigger input
- Communication interfaces
  - I^2C interface which support both master and slave modes with a frequency of up to 400 kHz
  - SPI interface which support both master and slave modes with a frequency of up to 18 MHz
  - USART interface operates at a frequency of up to 4.5 MHz
- Debug support
  - Serial Wire Debug Port - SW-DP
  - 6 instruction comparators and 2 literal comparators for hardware breakpoint or code / literal patch
  - 4 comparators for hardware watchpoint
  - 1-bit asynchronous trace - TRACESWO
- 48-pin LQFP package
- Operation temperature range: -40ºC to +85ºC

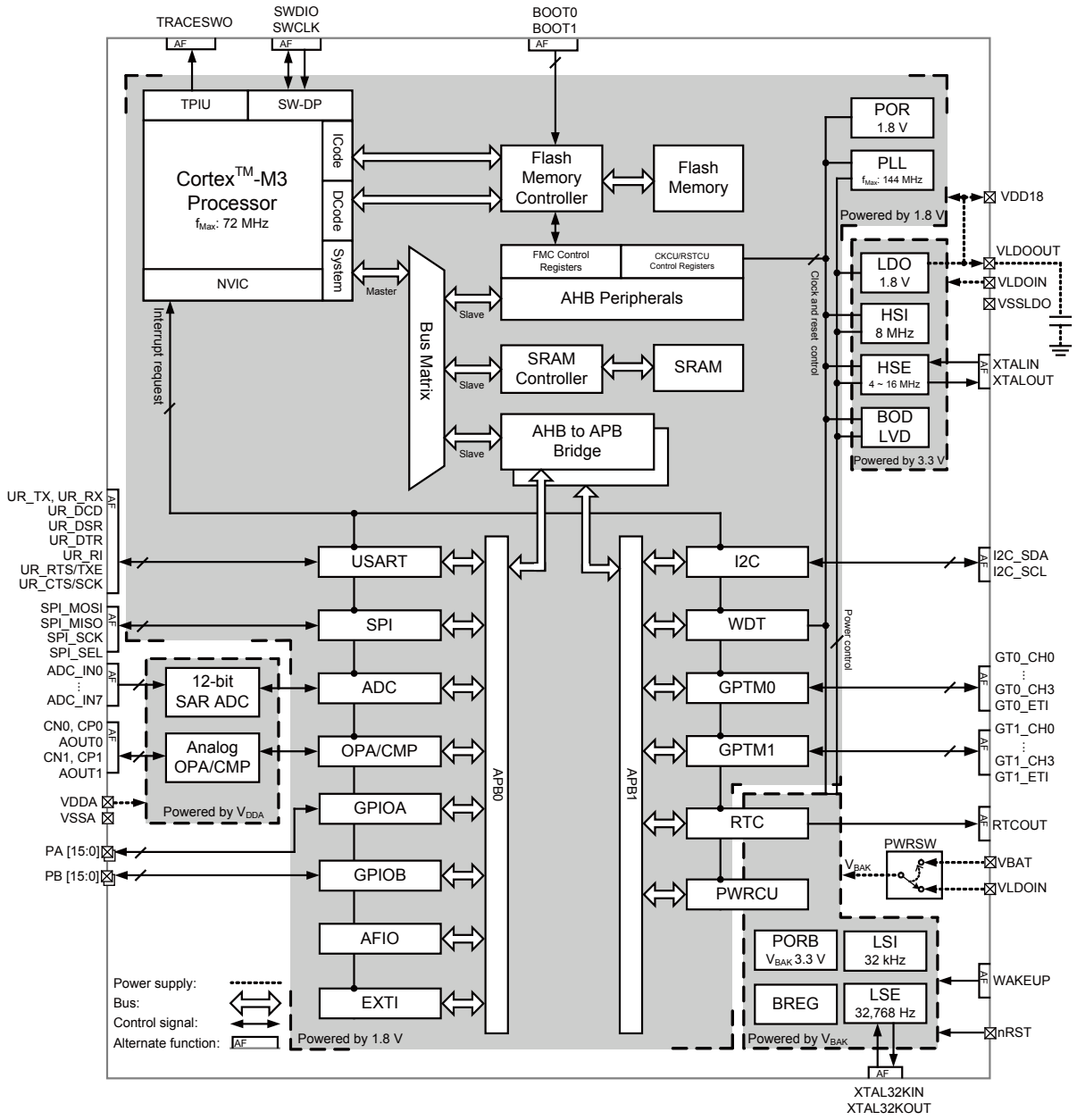
Device Information

Most features are common to all devices while the main features distinguishing them are Flash memory and SRAM memory capacities.

Table 1. HT32F125x Series Features and Peripheral List

Peripherals		HT32F1253	HT32F1252	HT32F1251	HT32F1251B
Main Flash (KB)		31	16	8	8
Option Bytes Flash (KB)		1	1	1	1
SRAM (KB)		8	4	2	2
Timers	GPTM	2			
	RTC	1			
	WDT	1			
Communication	USART	1			
	SPI	1			
	I^2C	1			
GPIO		32			30
EXTI		16			
12-bit ADC Number of channels		1 8 Channels			
OPA/Comparator		2			
CPU frequency		Up to 72 MHz			
Operating voltage		2.7 V ~ 3.6 V			
Operating temperature		-40 °C ~ +85 °C			
Package		LQFP48			

Block Diagram



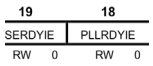
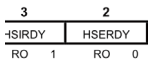
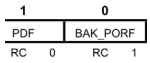
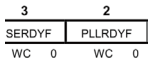
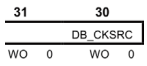
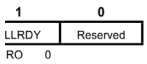
NOTE: HT32F1251B does not include the V_{BAT}, XTAL32KIN and XTAL32KOUT pins.

Figure 1. HT32F125x Block Diagram

2 Document Conventions

The conventions used in this document are shown in the following table.

Table 2. Document Conventions

Notation	Example	Description
0x	0x5a05	The number string with a 0x prefix indicates a hexadecimal number.
0xnnnn_nnnn	0x2000_0100	32-bit Hexadecimal address or data.
NAME [n]	ADDR [5]	Specific bit of NAME. NAME can be a register or field of register. For example, ADDR [5] means bit 5 of the ADDR register (field).
NAME [m:n]	ADDR [11:5]	Specific bits of NAME. NAME can be a register or field of register. For example, ADDR [11:5] means bit 11 to 5 of ADDR register (field).
X	'10X1'	Don't care notation which means any value is allowed.
RW		Software can read or write to this bit.
RO		Software can only read this bit. A write operation will have no effect.
RC		Software can only read this bit. Read operation will clear it to 0 automatically.
WC		Software can read this bit or clear it by writing 1. Writing 0 will have no effect.
WO		Software can only write to this bit. A read operation always returns 0.
Reserved		Reserved bit(s) for future use. Data read from these bits is not well defined and should be treated as random data. Normally these reserved bits should be to 0. Note that reserved bit must be kept at reset value.
Word		Data length of a word is 32-bit.
Half-word		Data length of a half-word is 16-bit.
Byte		Data length of a byte is 8-bit.

3 System Architecture

The system architecture of the HT32F125x series of devices that includes the ARM® Cortex™-M3 processor, bus architecture and memory organization will be described in the following sections. The Cortex™-M3 processor is a next generation processor core which offers many new features. Integrated and advanced features make the Cortex™-M3 processor suitable for market products that require microcontrollers with high performance and low power consumption. In brief, the Cortex™-M3 processor includes three AHB-Lite buses known as ICode, DCode and System buses. All memory accesses of the Cortex™-M3 processor are executed on the three buses according to the different purposes and the target memory spaces. The memory organisation uses a Harvard architecture, pre-defined memory map and up to 4 GB of memory space, making the system flexible and extendable.

ARM® Cortex-M3 Processor

The Cortex™-M3 processor is a general-purpose 32-bit processor core especially suitable for products requiring high performance and low power consumption microcontrollers. It offers many new features such as a Thumb-2 instruction sets, hardware divider, low latency interrupt respond time, atomic bit-band access and multiple buses for simultaneous accesses. The Cortex™-M3 processor is based on the ARMv7 architecture and supports both Thumb and Thumb-2 instruction sets. Some system peripherals listed below are also provided by Cortex™-M3:

- Internal Bus Matrix connected with ICode bus, DCode bus, System bus, Private Peripheral Bus (PPB) and debug accesses (AHB-AP)
- Nested Vectored Interrupt Controller (NVIC)
- Flash Patch and Breakpoint (FPB)
- Data Watchpoint and Trace (DWT)
- Instrument Trace Macrocell (ITM)
- Memory Protection Unit (MPU)
- Serial Wire debug Port (SW-DP)
- Serial Wire JTAG Debug Port (SWJ-DP)
- Embedded Trace Macrocell (ETM)
- Trace Port Interface Unit (TPIU)

The following figure shows the Cortex™-M3 processor block diagram. For more information, refer to the ARM® Cortex™-M3 Technical Reference Manual.

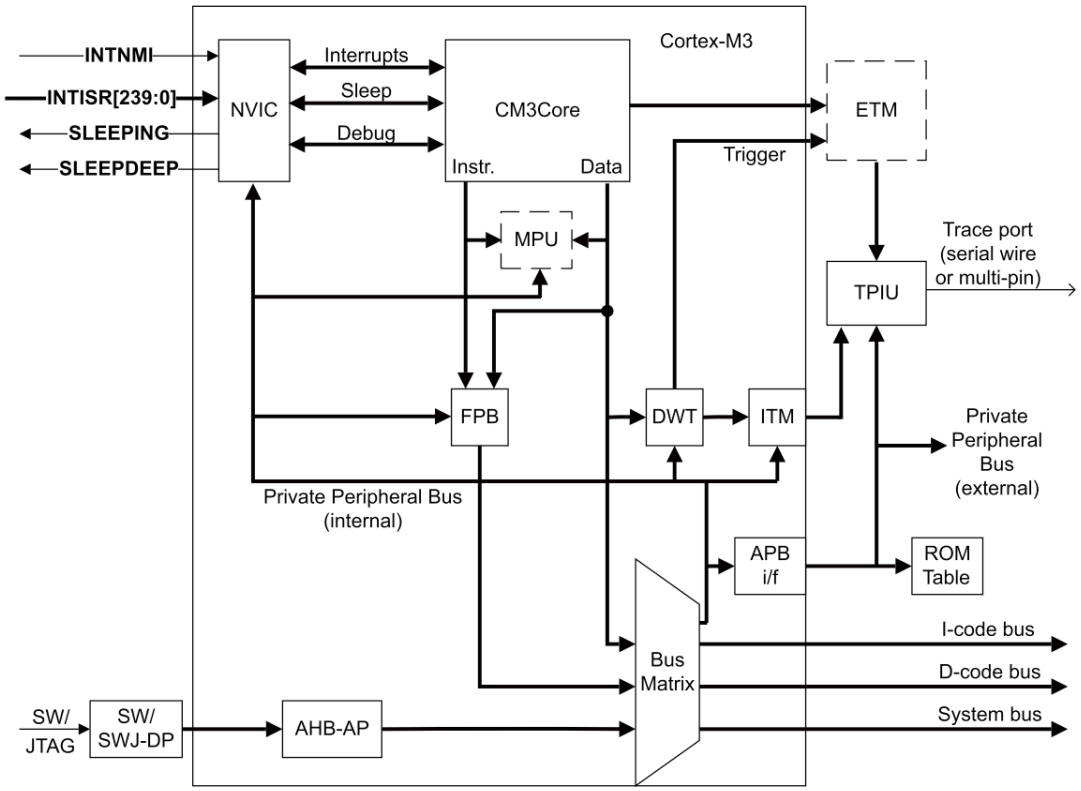


Figure 2. Cortex™-M3 Block Diagram

Bus Architecture

The HT32F125x series consists of three masters and four slaves in the bus architecture. The Cortex™-M3 ICode, DCode and System buses are the masters while the internal SRAM access bus, the internal Flash memory access bus, the AHB peripherals access bus and the AHB to APB bridge are the slaves. The ICode bus is used for instruction and vector fetches from the Code region (0x0000_0000 ~ 0x1FFF_FFFF) to the Cortex™-M3 core. The DCode bus is used for loading/storing data and also for debug access of the Code region. Similarly, the System bus is used for instruction/vector fetches, data loading/storing and debugging access of the system regions. The System regions include the internal SRAM region and the Peripheral region. All of the three master buses are based on 32-bit Advanced High-performance Bus-Lite (AHB-Lite) protocol. The following figure shows the bus architecture of the HT32F125x series.

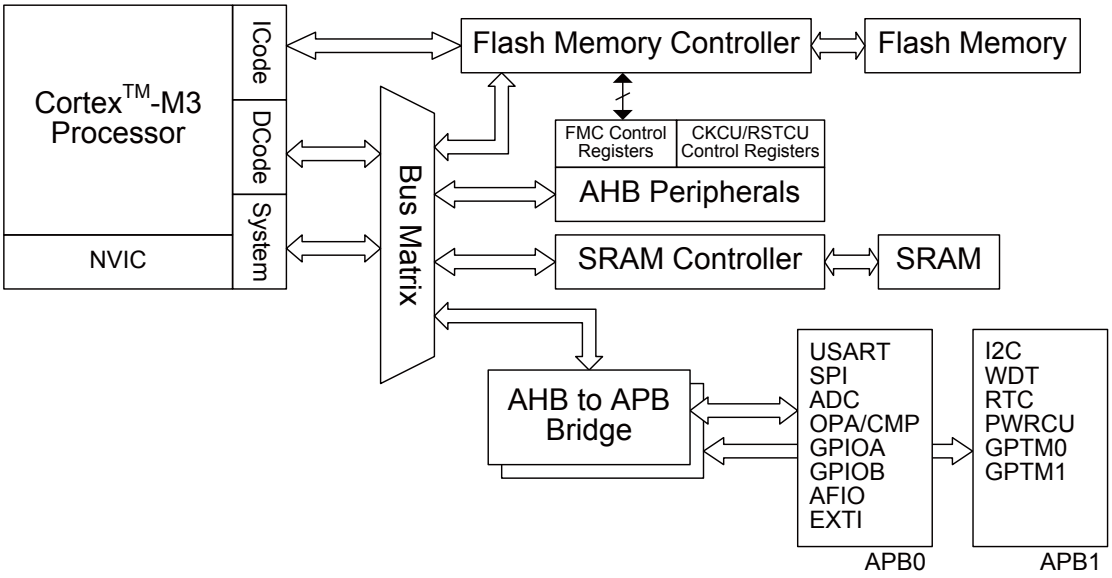
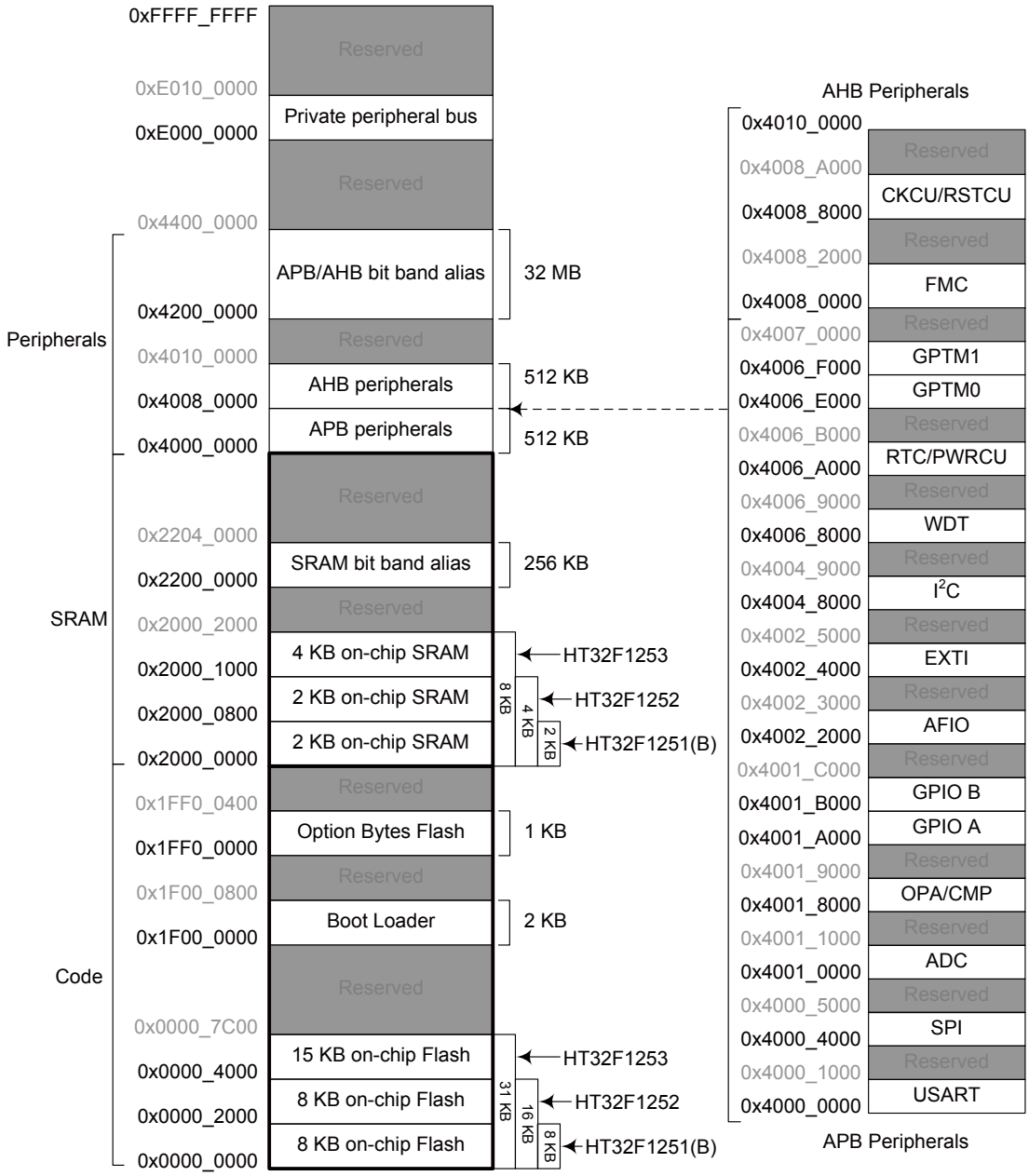


Figure 3. HT32F125x Series Bus Architecture

Memory Organization

The ARM® Cortex™-M3 processor is structured in Harvard architecture which can use separate buses to fetch instructions and load/store data. The instruction code and data are both located in the same memory address space but in different address ranges. The maximum address range of the Cortex™-M3 is 4 GB since it has a 32-bit bus address width. Additionally, a pre-defined memory map is provided by the Cortex™-M3 processor to reduce the software complexity of repeated implementation of different device vendors. However, some regions are used by the ARM® Cortex™-M3 system peripherals. Refer to the ARM® Cortex™-M3 Technical Reference Manual for more information. The following figure shows the memory map of the HT32F125x series of devices, including Code, SRAM, peripheral, and other pre-defined regions.

Memory Map



NOTES: 1. For HT32F1251(B), the Flash memory space at 0x0000_2000 to 0x0000_7BFF and the SRAM memory space at 0x2000_0800 to 0x2000_1FFF are reserved.

2. For HT32F1252, the Flash memory space at 0x0000_4000 to 0x0000_7BFF and the SRAM memory space at 0x2000_1000 to 0x2000_1FFF are reserved.

Figure 4. HT32F125x Memory Map

Table 3. HT32F125x Series Register Map

Start Address	End Address	Peripheral	Bus	Register map
0x4000_0000	0x4000_0FFF	USART	APB	
0x4000_1000	0x4000_3FFF	Reserved		
0x4000_4000	0x4000_4FFF	SPI		
0x4000_5000	0x4000_FFFF	Reserved		
0x4001_0000	0x4001_0FFF	ADC		
0x4001_1000	0x4001_7FFF	Reserved		
0x4001_8000	0x4001_8FFF	OPA/Comparator		
0x4001_9000	0x4001_9FFF	Reserved		
0x4001_A000	0x4001_AFFF	GPIOA		
0x4001_B000	0x4001_BFFF	GPIOB		
0x4001_C000	0x4001_CFFF	Reserved		
0x4001_D000	0x4002_1FFF	Reserved		
0x4002_2000	0x4002_2FFF	AFIO		
0x4002_3000	0x4002_3FFF	Reserved		
0x4002_4000	0x4002_4FFF	EXTI		
0x4002_5000	0x4004_7FFF	Reserved		
0x4004_8000	0x4004_8FFF	I^2C		
0x4004_9000	0x4006_7FFF	Reserved		
0x4006_8000	0x4006_8FFF	WDT		
0x4006_9000	0x4006_9FFF	Reserved		
0x4006_A000	0x4006_AFFF	RTC/PWRCU		
0x4006_B000	0x4006_DFFF	Reserved		
0x4006_E000	0x4006_EFFF	GPTM0		
0x4006_F000	0x4006_FFFF	GPTM1		
0x4007_0000	0x4007_FFFF	Reserved		
0x4008_0000	0x4008_1FFF	FMC	AHB	
0x4008_2000	0x4008_7FFF	Reserved		
0x4008_8000	0x4008_9FFF	CKCU/RSTCU		
0x4008_A000	0x400F_FFFF	Reserved		

Embedded Flash Memory

The HT32F125x series of devices provide up to 32 KB of on-chip Flash memory which is located at address 0x0000_0000. It supports bytes, half-word and word access. Note that the Flash memory only supports read operations for the Cortex™-M3 ICode or DCode bus access. Any write operations to the Flash memory (via DCode bus) will cause a bus fault exception. The Flash memory has a capacity of up to 32 pages. Each page has a memory capacity of 1 KB and can be erased independently. A 32-bit programming interface provides the capability of changing bits from 1 to 0. A data storage or firmware upgrade can be implemented using several methods such as In System Programming (ISP), In Application Programming (IAP) or In Circuit Programming (ICP). For more information refer to the Flash Memory Controller section.

Embedded SRAM Memory

The HT32F125x series of devices contain up to 8 KB of on-chip SRAM which is located at address 0x2000_0000. They support byte, half-word, and word access operations. In order to reduce the time of read-modify-write operations, the Cortex™-M3 processor provides a bit-band function to perform a single atomic bit operation. Users can modify a single bit in the SRAM bit-band region by accessing the corresponding bit-band alias. For more information about bit-bind, refer to the ARM® Cortex™-M3 Technical Reference Manual. The following formulas and examples show how to access a bit in the bit-band region by calculating the bit-band alias.

```
Bit-band alias = Bit-band base + (byte offset * 32) + (bit number * 4)
```

For example, to access bit 7 of address 0x2000_0200, the bit-band alias is:

```
Bit-band alias = 0x2200_0000 + (0x200 * 32) + (7 * 4) = 0x2200_401C
```

Writing to address 0x2200_401C will cause bit 7 of address 0x2000_0200 change while a read to address 0x2200_401C will return 0x01 or 0x00 according to the value of bit 7 at the SRAM address 0x2000_0200.

AHB Peripherals

The address of the AHB peripherals ranges from 0x4008_0000 to 0x400F_FFFF. Some peripherals such as the Clock Control Unit, Reset Control Unit and Flash Memory Controller are connected to the AHB bus directly. The AHB peripheral clocks are always enabled after a system reset. Access to the registers for these peripherals can be achieved directly via the AHB bus. Note that all the peripheral registers in the AHB bus support only word access.

APB Peripherals

The address of the APB peripherals ranges from 0x4000_0000 to 0x4007_FFFF. An APB to AHB bridge provides access capability between the Cortex™-M3 processor and the APB peripherals. Additionally, the APB peripheral clocks are disabled after a system reset. Software must enable the peripheral clock by setting up the APBCCRn register in the Clock Control Unit before accessing the corresponding peripheral register. Note that the APB to AHB bridge will duplicate the half-word or byte data to word width when a half-word or byte access is performed on the APB peripheral registers. In other words, the access result of a half-word or byte access on the APB peripheral registers will vary depending on the width of access data.

4 Flash Memory Controller (FMC)

Introduction

The Flash Memory Controller, FMC, provides all the necessary functions and pre-fetch buffer for the embedded on-chip Flash Memory. Since the access speed of the Flash Memory is slower than the CPU, a wide access interface with a pre-fetch buffer is provided for the Flash Memory in order to reduce the CPU waiting time which will cause CPU instruction execution delays. Flash Memory word program/page erase functions are also provided.

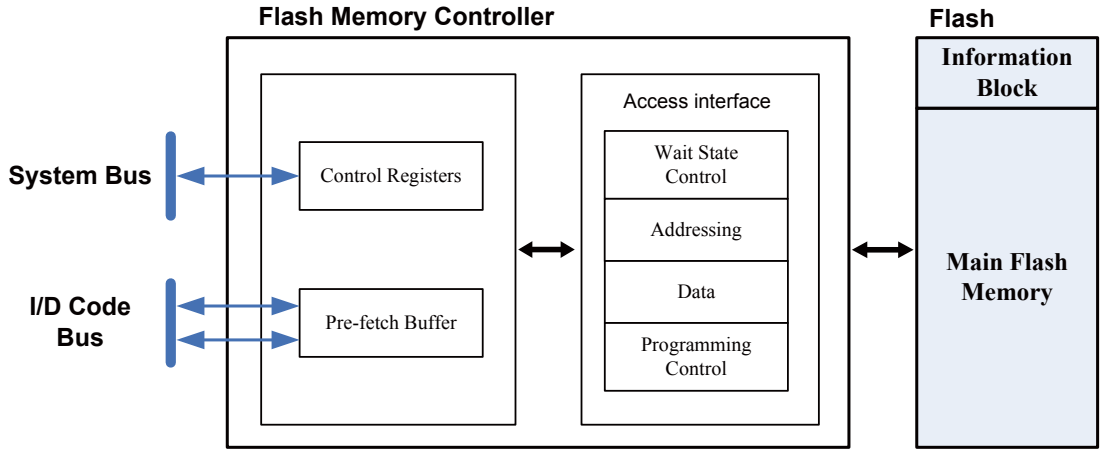


Figure 5. Block Diagram of Flash Memory Controller

Features

- Up to 32 KB of on-chip Flash memory for storing instruction/data and options
  - HT32F1253: 31 KB + 1 KB (instruction/data + option bytes)
  - HT32F1252: 16 KB + 1 KB (instruction/data + option bytes)
  - HT32F1251(B): 8 KB + 1 KB (instruction/data + option bytes)
- Page size of 1 KB - total of up to 32 pages
- Wide access interface with pre-fetch buffer to reduce instruction gaps
- Page erase and mass erase capability
- 32-bit word programming
- Interrupt function to indicate end of flash memory operations or an error occurs
- Flash read protection to prevent illegal code/data access
- Page erase/program protection to prevent unexpected operation

Functional Descriptions

Flash Memory Map

The following figure is the Flash Memory map of the HT32F125x series of devices in which the address ranges from 0x0000_0000 to 0x1FFF_FFFF (0.5 GB). The address from 0x1F00_0000 to 0x1F00_07FF is mapped to the Boot Loader Block with a capacity of 2 KB. Additionally, the region addressed from 0x1FF0_0000 to 0x1FF0_03FF is the Option Byte Block with a capacity of 1 KB. The memory mapping on system view is shown as below.

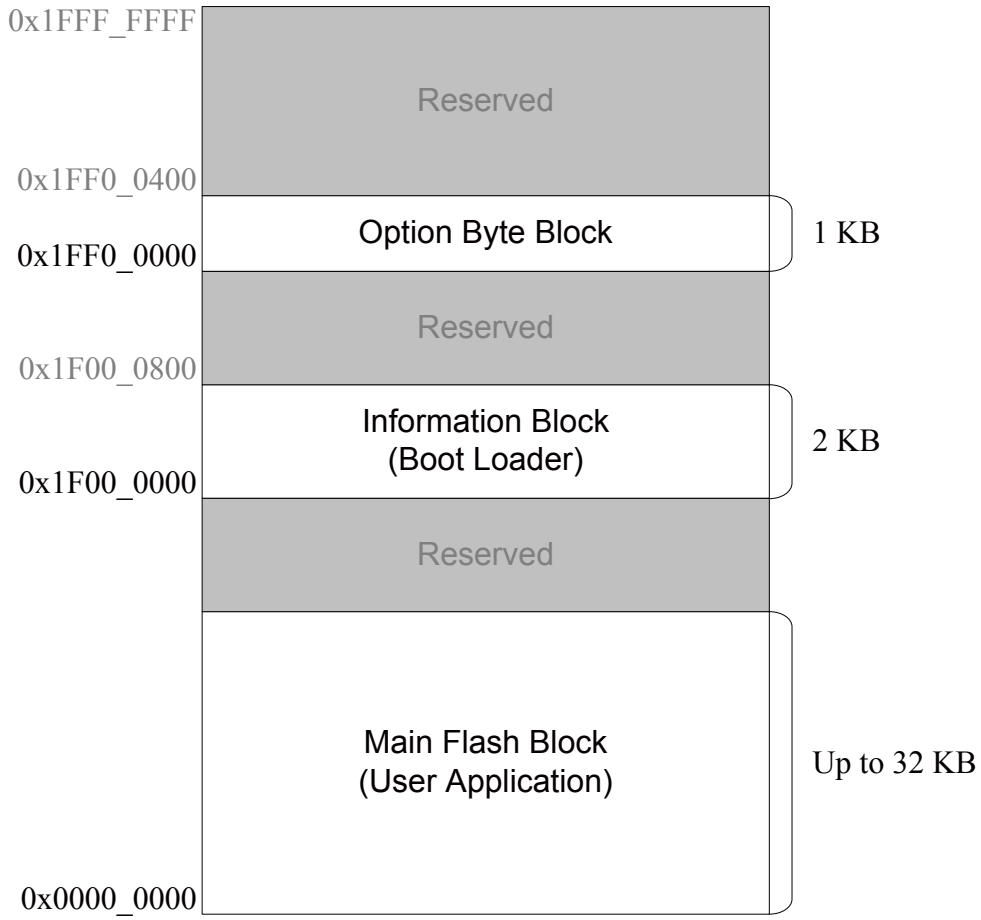


Figure 6. Memory Map of Flash Memory

Flash Memory Architecture

The Flash memory consists of up to 32 KB main Flash organized into 32 pages with 1 KB capacity per page and a 2 KB Information Block for the Boot Loader. The main Flash memory contains a total of up to 32 pages which can be erased individually. The following table shows the base address, size, and protection setting bit of each page.

Table 4. Flash Memory and Option Byte

Block	Name	Address	Page Protection Bit	Size
Main Flash Block	Page 0	0x0000_0000 ~ 0x0000_03FF	OB_PP [0]	1 KB
	Page 1	0x0000_0400 ~ 0x0000_07FF	OB_PP [1]	1 KB
	Page 2	0x0000_0800 ~ 0x0000_0BFF	OB_PP [2]	1 KB
	• • •	• • •	• • •	• • •
	Page 30	0x0000_7800 ~ 0x0000_7BFF	OB_PP [30]	1 KB
	Option Byte	0x1FF0_0000 ~ 0x1FF0_03FF	OB_CP [1]	1 KB
Information Block	Boot Loader	0x1F00_0000 ~ 0x1FF0_07FF	NA	2 KB

NOTE: The Information Block stores the bootloader - this block can not be programmed or erased by user.

Wait State Setting

When the CPU clock, HCLK, is greater than the access speed of the Flash memory, then wait state cycles must be inserted during the CPU fetch instructions or load data from Flash memory. The wait state can be changed by setting the WAIT [2:0] bits of the Flash Cache and Pre-fetch Control Register CFCR. In order to match the wait state requirement, the following two rules should be considered.

- HCLK clock is switched from low to high frequency:
  Change the wait state setting first and then switch the HCLK clock.
- HCLK clock is switched from high to low frequency:
  Switch the HCLK clock first and then change the wait state setting.

The following table shows the relationship between the wait state cycle and the CPU clock HCLK. The default wait state is 0 since the High Speed Internal oscillator HSI which operates at a frequency of 8 MHz is selected as the HCLK clock source after a reset.

Table 5. Relationship Between Wait State Cycle and HCLK

Wait State Cycle	HCLK
0	0 MHz < HCLK ≦ 24 MHz
1	24 MHz < HCLK ≦ 48 MHz
2	48 MHz < HCLK ≦ 72 MHz

Booting Configuration

The HT32F125x series of devices provides three kinds of boot modes which can be selected using the BOOT0 and BOOT1 pins. The BOOT0 and BOOT1 pins are sampled during a power-on reset or a system reset. Once the logic value on these pins has been determined, the first 4 words of the vector will be remapped to the corresponding source according to the boot mode. The boot modes are shown in the following table.

Table 6. Booting Modes

Boot mode selection pins		Mode	Description
BOOT1	BOOT0		
0	0	Boot Loader	Vector Source is the Boot Loader
0	1	SRAM	Vector source is SBVT0 ~ SBVT3
1	X	Main Flash	Vector source is the main Flash Memory

The Vector Mapping Control Register (VMCR) is provided to change the vector remapping setting temporarily after a device reset. The initial reset value of the VMCR register is determined by the BOOT0 and BOOT1 pins which will be sampled during the reset duration.

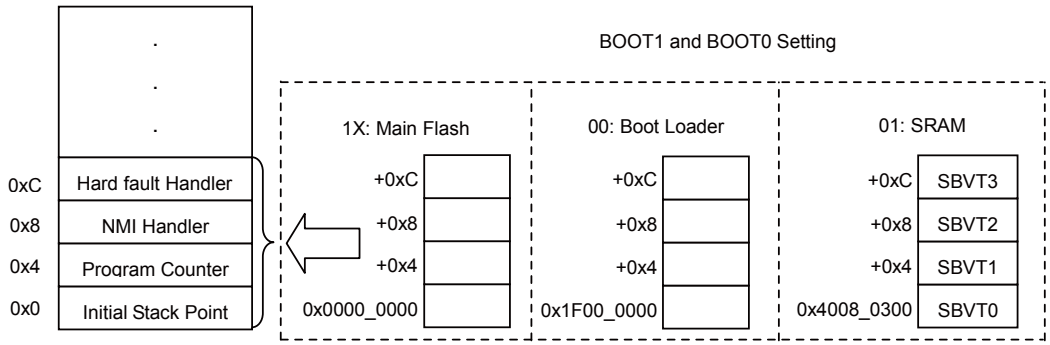


Figure 7. Vector Remapping

Page Erase

The FMC provides a page erase function which is used to initialise the contents of a Flash memory page to a high state. Each page can be erased independently without affecting the contents of other pages. The following steps show the access sequence of the register for a page erase operation.

- Check the OPCR register to confirm that no Flash memory operation is in progress (OPM [3:0] equal to 0xE or 0x6). Otherwise, wait until the operation has finished.
- Write the page address into the TADR register
- Write the page erase command into the OCMR register (CMD [3:0] = 0x8).
- Send the page erase command to the FMC by setting the OPCR register (set OPM [3:0] = 0xA).
- Wait until all the operations have been completed by checking the value of the OPCR register (OPM [3:0] equal to 0xE).
- Read and verify the page if required using a DCODE access.

Note that a correct target page address must be confirmed. The software may run out of control if the target erase page is being used to fetch codes or to access data. The FMC will not provide any notification when this occurs. Additionally, the page erase operation will be ignored on protected pages. A Flash Operation Error interrupt will be triggered by the FMC if the OREIEN bit in the OIER register is set. The software can check the PPEF bit in the OISR register to detect this condition in the interrupt handler. The following figure shows the page erase operation flow.

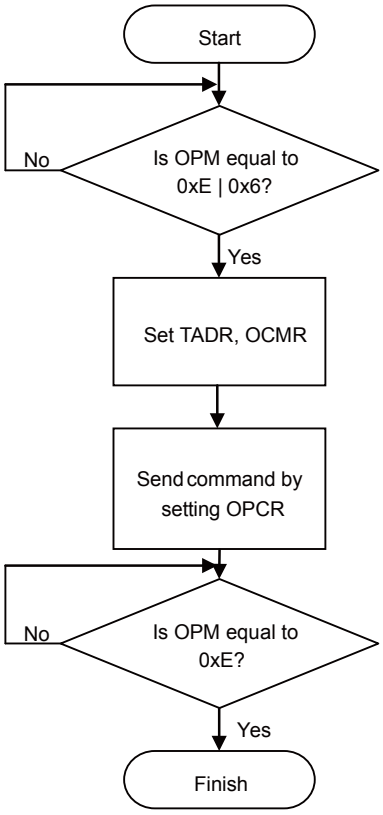


Figure 8. Flash Page Erase Operation Flowchart

Mass Erase

The FMC provides a complete erase function which is used to initialise the complete Flash Memory contents. The following steps show the mass erase register access sequence.

- Check the OPCR register to confirm that there is no Flash memory operations in progress (OPM [3:0] equal to 0xE or 0x6). Otherwise, wait until the previous operation has finished.
- Write the mass erase command into the OCMR register (CMD [3:0] = 0xA).
- Send the mass erase command to the FMC by setting the OPCR register (set OPM [3:0] = 0xA).
- Wait until all operations have finished by checking that the value of the OPCR register (OPM [3:0] is equal to 0xE).
- Read and verify the Flash memory if required using a DCODE access.

Since all Flash data will be reset to a value of 0xFFFF_FFFF, the mass erase operation can be implemented using a program that runs in SRAM or by using the debugging tool that accesses the FMC registers directly. Software functions that are executed on the Flash memory will not trigger a mass erase operation. The following figure indicates the mass erase operation flow.

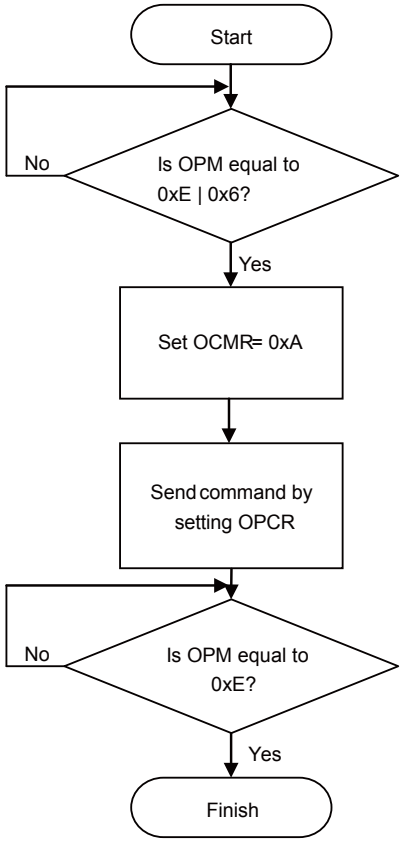


Figure 9. Mass Erase Operation Flowchart

Word Programming

The FMC provides a 32-bit word programming function which is used to modify the Flash memory contents. The following steps show the word programming operation register access sequence.

- Check the OPCR register to confirm that no Flash memory operations are in progress (OPM [3:0] equal to 0xE, or 0x6). Otherwise, wait until the previous operation has finished.
- Write the word address into the TADR register. Write the word data into the WRDR register.
- Write the word program command into the OCMR register (CMD [3:0] = 0x4).
- Send the word program command to the FMC by setting the OPCR register (set OPM [3:0] = 0xA).
- Wait until all operations have finished by checking the value of the OPCR register (OPM [3:0] equal to 0xE).
- Read and verify the Flash memory if required using a DCODE access.

Note that the word programming operation can not be applied to the same address twice. Successive word programming operations to the same address must be separated by a page erase operation. Additionally, the word program operation will be ignored on protected pages. A Flash operation error interrupt will be triggered by the FMC if the OREIEN bit in the OIER register is set. The software can check the PPEF bit in the OISR register to detect this condition in the interrupt handler. The following figure displays the word programming operation flow.

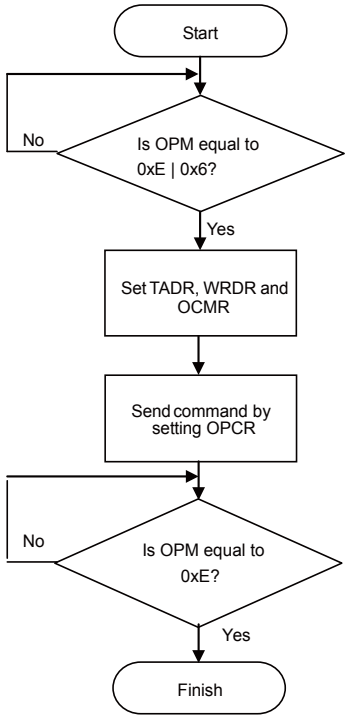


Figure 10. Word Programming Operation Flowchart

Option Byte Description

The Option Byte region can be treated as an independent Flash Memory in which the base address is 0x1FF0_0000. The following table shows the functional descriptions and the memory map of the Option Byte.

Table 7. Memory Map of Option Byte

Option Byte	Offset	Description	Reset Value
Option Byte Base Address = 0x1FF0_0000			
OB_PP	0x000 0x004 0x008 0x00C	OB_PP [n]: Flash Memory Page Erase/Program Protection (n = 0 ~ 30 for page 0 ~ page 30) 0: Flash Memory Page n Erase/Program Protection is enabled 1: Flash Memory Page n Erase/Program Protection is disabled OB_PP [127:31] is reserved for future usage.	0xFFFF_FFFF 0xFFFF_FFFF 0xFFFF_FFFF 0xFFFF_FFFF
OB_CP	0x010	OB_CP [0]: Flash Security Protection 0: Flash Security protection is enabled 1: Flash Security protection is disabled OB_CP [1]: Option Byte Protection 0: Option Byte protection is enabled 1: Option Byte protection is disabled OB_CP [31:2]: Reserved	0xFFFF_FFFF
OB_CK	0x020	OB_CK [31:0]: Flash Option Byte Checksum OB_CK should be set as the sum of the 5 words Option Byte content, of which the address offset ranges form 0x000 to 0x010 (0x000 + 0x004 + 0x008 + 0x00C + 0x010), when the content of the OB_PP or OB_CP register is not equal to 0xFFFF_FFFF.	0xFFFF_FFFF

Page Erase/Program Protection

The FMC provides page erase/program protection functions to prevent inadvertent operations on the Flash memory. The page erase (CMD [3:0] = 0x8 in the OCMR register) or word program (CMD [3:0] = 0x4) command will not be accepted by the FMC on protected pages. If the page erase or word program command is sent to the FMC on a protected page, the PPEF bit in the OISR register will then be set by the FMC. If the PPEF bit is set and the OREIE bit is also set to 1 to enable the corresponding interrupt, then the Flash operation error interrupt will be triggered by the FMC to get the attention of the CPU. The page protection function can be individually enabled for each page by configuring the OB_PP [30:0] bits field in the option byte. If a page erase operation is executed on the Option Byte region, all the Flash Memory page protection functions will be disabled. The page protection function of the Option Byte region is enabled by clearing the OB_CP [1] bit to 0. Once the Option Byte has been protected, the only way to disable its protection function is to execute a mass erase operation. The following table shows the access permission of the main Flash page when the page protection is enabled.

Table 8. Access Permission of Protected Flash Page

Mode / Operation	ISP/IAP	ICP/Debug mode	Boot from SRAM
DCODE Read	O	O	O
Program	X	X	X
Page Erase	X	X	X
Mass Erase	O	O	O

NOTES: **1.** Note that the write protection setup is based on specific pages. The above access permission only affects the pages that the protection function has been enabled. Other pages are not affected.

2. The Main Flash page protection is configured by OB_PP [30:0] bits. The Option Byte page protection is configured by the OB_CP [1] bit.

The following steps show the page erase/program protection procedure register access sequence:

- Check the OPCR register to confirm that no Flash memory operation is in progress (OPM [3:0] equal to 0xE or 0x6). Otherwise, wait until the previous operation has been finished.
- Write the OB_PP address into the TADR register (TADR = 0x1FF0_0000).
- Write the data which indicates the protection function of the corresponding page is enabled or disabled into the WRDR register (0: Enabled, 1: Disabled).
- Write the word program command into the OCMR register (CMD [3:0] = 0x4).
- Send the word program command to the FMC by setting the OPCR register (set OPM [3:0] = 0xA).
- Wait until all operations have been finished by checking the value of the OPCR register (OPM [3:0] is equal to 0xE).
- Read and verify the Option Byte if required using a DCODE access.
- Obtain the OB_CK option byte by summing the 5 option words addressed from 0x000 to 0x010 according to the option byte checksum rule.
- Apply a system reset to activate the new OB_PP setting.

Security Protection

The FMC provides a Security protection function to prevent illegal code/data access on the Flash memory. This function is useful for protecting the software/firmware from illegal users. The function is activated by setting the option byte OB_CP [0]. Once the function has been enabled, all the main Flash DCODE access, programming and page erase operations will not be allowed except for the user's application. However, the mass erase operation will still be accepted by the FMC in order to disable this security protection function. The following table shows the access permission of Flash memory when the security protection is enabled.

Table 9. Access Permission When The Security Protection Is Enabled

Mode / Operation	User application (Note 1)	ICP/Debug mode	Boot from SRAM
DCODE Read	O	X (read as 0)	X (read as 0)
Program	O (Note 1)	X	X
Page Erase	O (Note 1)	X	X
Mass Erase	O	O	O

NOTES: 1. User application means the software that is executed or booted from the main Flash memory with the JTAG/SW debugger disconnected. However the Option Byte block and page 0 are still protected in which Program/Page Erase operations can not be executed.

2. A mass erase operation can erase the Option Byte Block and disable its security protection.

The following steps show the security protection procedure register access sequence.

- Check the OPCR register to confirm that no Flash memory operation is in progress (OPM [3:0] equal to 0xE or 0x6). Otherwise, wait until the pervious operation has been finished.
- Write the OB_CP address into the TADR register (TADR = 0x1FF0_0010).
- Write the data into the WRDR register to clear the OB_CP [0] bit to 0.
- Write the word program command into the OCMR register (CMD [3:0] = 0x4).
- Send the word program command to the FMC by setting the OPCR register (set OPM = 0xA).
- Wait until all operations have been finished by checking the value of the OPCR register (OPM [3:0] equals to 0xE).
- Read and verify the option byte if required using a DCODE access.
- Program the OB_CK option byte by summing the 5 option words addressed from 0x000 to 0x010 according to the option byte checksum rule.
- Apply a system reset to activate the new OB_CP setting.

Register Map

The following table shows the FMC registers and reset values.

Table 10. Register Map of FMC

Register	Offset	Description	Reset Value
FMC Base Address = 0x4008_0000			
TADR	0x000	Flash Target Address Register	0x0000_0000
WRDR	0x004	Flash Write Data Register	0x0000_0000
OCMR	0x00C	Flash Operation Command Register	0x0000_0000
OPCR	0x010	Flash Operation Control Register	0x0000_000C
OIER	0x014	Flash Operation Interrupt Enable Register	0x0000_0000
OISR	0x018	Flash Operation Interrupt Status Register	0x0001_0000
PPSR	0x020 0x024 0x028 0x02C	Flash Page Erase/Program Protection Status Register	0xXXXX_XXXX 0xXXXX_XXXX 0xXXXX_XXXX 0xXXXX_XXXX
CPSR	0x030	Flash Security Protection Status Register	0xXXXX_XXXX
VMCR	0x100	Flash Vector Mapping Control Register	0x0000_000X
CFCR	0x200	Flash Cache and Pre-fetch Control Register	0x0000_0051
SBVT0	0x300	SRAM Booting Vector 0 (Stack Pointer)	0x2000_XX00
SBVT1	0x304	SRAM Booting Vector 1 (Program Counter)	0x2000_0101
SBVT2	0x308	SRAM Booting Vector 2 (NMI Handler)	0x0000_0000
SBVT3	0x30C	SRAM Booting Vector 3 (Hard Fault Handler)	0x0000_0000

NOTE: "X" means various reset values which depend on the Device, Flash value, option byte value or power on reset setting.

Register Descriptions

Flash Target Address Register (TADR)

This register specifies the target address of the page erase and word programming operations.

Offset: 0x000

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	TADB							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	TADB							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	TADB							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	TADB							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[31:0]	TADB	Flash Target Address Bits For programming operations, the TADR register specifies the address where the data is written. Since the programming length is 32 bits, TADR shall be set as word-aligned (4 bytes). TADB [1:0] will be ignored during programming operations. For page erase operations, the TADR register contains the page address which is going to be erased. Since the page size is 1 KB, TADB [9:0] will be ignored in order to limit the target address to 1 KB-aligned. For 32 KB main Flash addressing, TADB [31:16] should be zero (TADB [31:15] should be zero for 16 KB, TADB [31:14] should be zero for 8 KB). The Option Byte which has a I KB capacity ranges from 0x1FF0_0000 to 0x1FF0_03FF. This field is used to specify the Flash Memory address which must be within the range from 0x0000_0000 to 0x1FFF_FFFF. Otherwise, an Invalid Target Address interrupt will be generated if the corresponding interrupt enable bit is set.

Flash Write Data Register (WRDR)

This register stores the data to be written into the TADR register for programming operations.

Offset: 0x004

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	WRDB							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	23	22	21	20	19	18	17	16
	WRDB							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
	WRDB							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	WRDB							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[31:0]	WRDB	Flash Write Data Bits The data value for programming operation.

Flash Operation Command Register (OCMR)

This register is used to specify the Flash operation commands that include read, read ID, word program, page erase and mass erase.

Offset: 0x00C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved				CMD			
Type/Reset					RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[3:0]	CMD	Flash Operation Command The following table shows the definitions of the operation command bits CMD [3:0] which determine the Flash Memory operation. If an invalid command is set and the IOCMIEN bit is equal to 1, an Invalid Operation Command interrupt will occur.

CMD [3:0]	Description
0x0	Idle - default
0x4	Word program
0x8	Page erase
0xA	Mass erase
Others	Reserved

Flash Operation Control Register (OPCR)

This register is used for controlling the command commitment and checking the status of the FMC operations.

Offset: 0x010

Reset value: 0x0000_000C

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved			OPM				Reserved
Type/Reset				RW 0	RW 0	RW 0	RW 0	

Bits	Field	Descriptions
[4:1]	OPM	Operation Mode The following table shows the operation modes of the FMC. User can commit the command which is set by the OCMR register for the FMC according to the address alias setting in the TADR register. The contents of the TADR, WRDR and OCMR registers should be prepared before setting this register. After all the operations have finished, the OPM field will be set as 0xE by the FMC hardware. The Idle mode can be set when all the operations have finished for power saving purposes. Note that the operation status should be checked before the next operation is executed on the FMC. The contents of the TADR, WRDR, OCMR and OPCR registers should not be changed until the previous operation has finished.

OPM [4:1]	Description
0x6	Idle (default)
0xA	Commit command to main Flash
0xE	All operation finished on main Flash
Others	Reserved

Flash Operation Interrupt Enable Register (OIER)

This register is used to enable or disable the FMC interrupt function. The FMC generates interrupts to the controller when the corresponding interrupt enable bits are set.

Offset: 0x014

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved			OREIEN	IOCMIEN	OBEIEN	ITADIEN	ORFIEN
Type/Reset				RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[4]	OREIEN	Operation Error Interrupt Enable 0: Operation Error interrupt is disabled 1: Operation Error interrupt is enabled
[3]	IOCMIEN	Invalid Operation Command Interrupt Enable 0: Invalid Operation Command interrupt is disabled 1: Invalid Operation Command interrupt is enabled
[2]	OBEIEN	Option Byte Check Sum Error Interrupt Enable 0: Option Byte Check Sum Error interrupt is disabled 1: Option Byte Check Sum Error interrupt is enabled
[1]	ITADIEN	Invalid Target Address Interrupt Enable 0: Invalid Target Address interrupt is disabled 1: Invalid Target Address interrupt is enabled
[0]	ORFIEN	Operation Finished Interrupt Enable 0: Operation Finish interrupt is disabled 1: Operation Finish interrupt is enabled

Flash Operation Interrupt and Status Register (OISR)

This register indicates the FMC interrupt status which is used to check if a Flash operation has finished otherwise an error occurs. The status bits are available when the corresponding interrupt enable bits in the OIER register are set.

Offset: 0x018

Reset value: 0x0001_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved						PPEF	RORFF
Type/Reset							RO 0	RO 1
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved			OREF	IOCMF	OBEF	ITADF	ORFF
Type/Reset				WC 0	WC 0	WC 0	WC 0	WC 0

Bits	Field	Descriptions
[17]	PPEF	Page Erase/Program Protected Error Flag 0: Page Erase/Program Protected Error does not occur 1: Operation error occurs due to an invalid Page erase/program operation being applied to a protected page This bit is reset by hardware once a new flash operation command is committed.
[16]	RORFF	Raw Operation Finished Flag 0: The last flash operation command has not yet finished 1: The last flash operation command has finished The RORFF bit is directly connected to the Flash memory for debugging purpose.
[4]	OREF	Operation Error Flag 0: No flash operation error has occurred 1: The last flash operation has failed This bit will be set when any flash operation error occurs such as an invalid command, program error and erase error, etc. The ORE interrupt occurs if the OREIEN bit in the OIER register is set. Reset this bit by writing 1
[3]	IOCMF	Invalid Operation Command Flag 0: No invalid flash operation command was set 1: An invalid flash operation command has been written to the OCMR register. The IOCM interrupt will occur if the IOCMIEN bit in the OIER register is set. Reset this bit by writing 1.
[2]	OBEF	Option Byte Checksum Error Flag 0: Option byte Checksum is correct 1: Option byte Checksum is incorrect The OBE interrupt will occur if the OBEIEN bit in the OIER register is set. Reset this bit by writing 1.

Bits	Field	Descriptions
[1]	ITADF	Invalid Target Address Flag 0: The target address TADR is valid 1: The target address TADR is invalid The data in the TADR field must have a range from 0x0000_0000 to 0x1FFF_FFFF. An ITAD interrupt will occur if the ITADIEN bit in the OIER register is set. Reset this bit by writing 1.
[0]	ORFF	Operation Finished Flag 0: Flash operation unfinished. 1: Last flash operation command has finished The ORF interrupt will occur if the ORFIEN bit in the OIER register is set. Reset this bit by writing 1.

Flash Page Erase/Program Protection Status Register (PPSR)

This register indicates the page protection status of the Flash Memory.

Offset: 0x020 ~ 0x02C

Reset value: 0xXXXX_XXXX

	31		30		29		28		27		26		25		24	
	PPSBn															
Type/Reset	RO	X	RO	X	RO	X	RO	X	RO	X	RO	X	RO	X	RO	X
	23		22		21		20		19		18		17		16	
	PPSBn															
Type/Reset	RO	X	RO	X	RO	X	RO	X	RO	X	RO	X	RO	X	RO	X
	15		14		13		12		11		10		9		8	
	PPSBn															
Type/Reset	RO	X	RO	X	RO	X	RO	X	RO	X	RO	X	RO	X	RO	X
	7		6		5		4		3		2		1		0	
	PPSBn															
Type/Reset	RO	X	RO	X	RO	X	RO	X	RO	X	RO	X	RO	X	RO	X

Bits	Field	Descriptions
[127:0]	PPSBn	Page n Erase/Program Protection Status Bits (n = 0 ~ 127) PPSB[n] = OB_PP[n] 0: The corresponding page n is protected 1: The corresponding page n is not protected The content of this register is not dynamically updated and will only be reloaded by the option byte loader which is activated when any kind of reset occurs. The erase or program function of the specific pages is not allowed when the corresponding bits of the PPSR registers are reset. The reset value of the bits PPSR [127:0] is determined by the option byte, OB_PP [127:0]. The total pages of the main flash memory for the HT32F125x series will be different because of the different device specifications. Therefore, only the OB_PP [n:0] and PPSR [n:0] bits are valid (where n = chip flash page number - 1). The other bits of the OB_PP and PPSR registers are reserved for future usage.

Flash Security Protection Status Register (CPSR)

This register indicates the Flash Memory Security protection status. The content of this register is not dynamically updated and will only be reloaded by the option byte loader which is activated when any kind of reset occurs.

Offset: 0x030

Reset value: 0xXXXX_XXXX

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved						OBPSB	CPSB
Type/Reset							RO X	RO X

Bits	Field	Descriptions
[1]	OBPSB	Option Byte Page Erase/Program Protection Status Bit 0: The Option Bytes page is protected. 1: The Option Bytes page is not protected. The reset value of the OPBSB bit is determined by the OB_CP [1] bit in the option byte.
[0]	CPSB	Flash Memory Security Protection Status Bit 0: Flash Memory Security protection is enabled 1: Flash Memory Security protection is not enabled The reset value of the CPSB bit is determined by the OB_CP [0] bit in the option byte,.

Flash Vector Mapping Control Register (VMCR)

This register is used to control the vector mapping. The reset value of the VMCR register is determined by the status of the external booting pins, BOOT0 and BOOT1 during the power on reset period.

Offset: 0x100

Reset value: 0x0000_000X

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved						VMCB	
Type/Reset							RW X	RW X

Bits	Field	Descriptions
[1:0]	VMCB	Vector Mapping Control Bit The VMCB bits are used to control the mapping source of the first 4-word vectors addressed from 0x0 to 0xC. The following table shows the vector mapping setup.

BOOT1	BOOT0	VMCB [1:0]	Descriptions
Low	Low	00	Boot Loader mode The vector mapping source is the boot loader area.
Low	High	01	SRAM booting mode The vector mapping source is SBVT0~3.
High	Low	10	Main Flash mode The vector mapping source is the main Flash Memory area.
High	High	11	

The reset value of the VMCB register is determined by the pin status of the external booting pins BOOT1 and BOOT0 during a power on reset and a system reset. However, when the application program is executed, the vector mapping settings can be temporarily changed by configuring the VMCB bits to correctly access the first 4-word vectors in the flash memory, especially when the CPU is booted from the Boot Loader or the SRAM region.

Flash Pre-fetch Control Register (CFCR)

This register is used for controlling the FMC pre-fetch module.

Offset: 0x200

Reset value: 0x0000_0051

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								

	7	6	5	4	3	2	1	0
	Reserved	IPSE	Reserved	PFBE	Reserved	WAIT		
Type/Reset		RW 1		RW 1		RW 0	RW 0	RW 1

Bits	Field	Descriptions
[6]	IPSE	Flash Idle Power Saving Enable Bit 0: Flash Idle Power Saving is disabled 1: Flash Idle Power Saving is enabled
[4]	PFBE	Pre-fetch Buffer Enable Bit 0: Pre-fetch buffer is disabled. The instruction/Data is provided directly by theFlash memory. 1: Pre-fetch buffer is enabled
[2:0]	WAIT	Flash Wait State Setting These bits are used to set the HCLK wait clock count during a non-sequential Flash access. The actual value of the wait clocks is given by (WAIT [2:0] - 1). Since a wide access interface with a pre-fetch buffer is provided, the wait state of sequential Flash access is very close to zero.

WAIT [2:0]	Wait Status	Allowed HCLK Range
001	0	0 MHz < HCLK ≦ 24 MHz
010	1	24 MHz < HCLK ≦ 48 MHz
011	2	48 MHz < HCLK ≦ 72 MHz
Others	Reserved	Reserved

SRAM Booting Vector Register n (SBVTn, n = 0 ~3)

These registers specify the initial values of the Stack Point, Program Counter, NMI Handler address, and Hard Fault Handler address for the SRAM Booting mode.

Offset: 0x300 ~ 0x30C

Reset value: Various depending on the address offset

	31		30		29		28		27		26		25		24	
	SBVTn															
Type/Reset	RW	X	RW	X	RW	X	RW	X	RW	X	RW	X	RW	X	RW	X
	23		22		21		20		19		18		17		16	
	SBVTn															
Type/Reset	RW	X	RW	X	RW	X	RW	X	RW	X	RW	X	RW	X	RW	X
	15		14		13		12		11		10		9		8	
	SBVTn															
Type/Reset	RW	X	RW	X	RW	X	RW	X	RW	X	RW	X	RW	X	RW	X
	7		6		5		4		3		2		1		0	
	SBVTn															
Type/Reset	RW	X	RW	X	RW	X	RW	X	RW	X	RW	X	RW	X	RW	X

Bits	Field	Descriptions
[31:0]	SBVT	SRAM Booting Vector n (n = 0 ~ 3) The SRAM Booting Vector 0 ~ 3 provides a SRAM booting capability for application debugging. The contents of the SBVTn registers are re-mapped into the addresses 0x0 to 0xC of the Flash Memory CODE area under the SRAM booting mode. Refer to the description of the VMCR register and BOOT1/BOOT0 boot pins. The following table shows the purpose and reset value of the SBVTn register. The reset value provides a fixed setting for program execution during the SRAM booting mode. These registers can be modified by the debugging tool in order to change the program execution setting. The reset values of the SBVTn register will be reloaded only by a power-on reset. Other reset sources will have no effect.

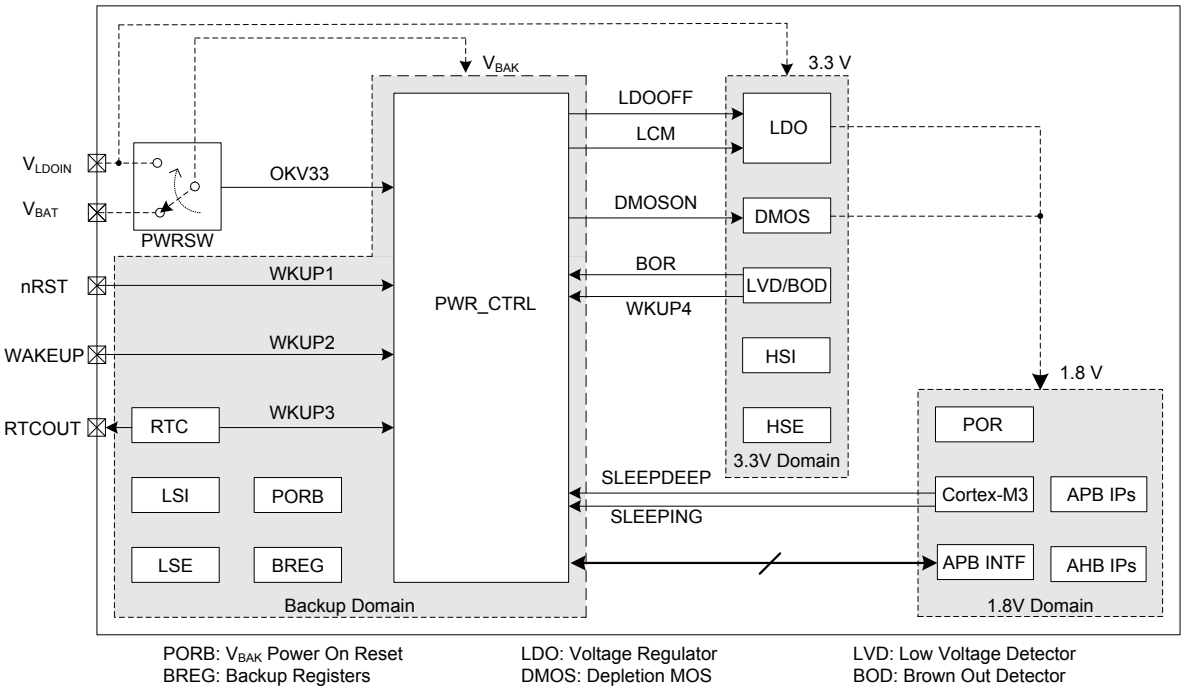
Name	Address Offset	Purpose Descriptions	Reset Value
SBVT0	0x300	Stack point	8 KB SRAM: 0x2000_2000 4 KB SRAM: 0x2000_1000 2 KB SRAM: 0x2000_0800
SBVT1	0x304	Program counter	0x2000_0101
SBVT2	0x308	NMI handler address	0x0000_0000
SBVT3	0x30C	Hard fault handler address	0x0000_0000

This access width of the registers SBVT0 ~SBVT3 must be a 32-bit access (Word access). 8 or 16 bits (Byte or Half-Word) access is not allowed.

5 Power Control Unit (PWRCU)

Introduction

The power consumption can be regarded as one of the most important issues for many embedded system applications. Accordingly the Power Control Unit, PWRCU, provides many types of power saving modes such as Sleep, Deep-Sleep1, Deep-Sleep2 and Power-Down modes. These modes reduce the power consumption and allow the application to achieve the best trade-off between the conflicting demands of CPU operating time, speed and power consumption. The dashed line in Figure 11 indicates the power supply source of three digital power domains but the backup domain power supply (V_{BAK}) of HT32F1251B does not support battery power (V_{BAT}).



NOTE: The backup domain power supply (V_{BAK}) of HT32F1251B does not support battery power (V_{BAT}).

Figure 11. PWRCU Block Diagram

Features

- Three power domains: Backup, 3.3V and 1.8V power domains
- Four power saving modes: Sleep, Deep-Sleep1, Deep-Sleep2 and Power-Down modes
- Internal Voltage regulator supplies 1.8 V voltage source
- Additional Depletion MOS supplies 1.8 V voltage source with low leakage and low operating current
- Brown Out Detector can issue a system reset or an interrupt when 3.3 V power source (V_{LDOIN}) is lower than 2.5 V.
- Low Voltage Detector can issue an interrupt or wakeup event when V_{LDOIN} is lower than a programmable threshold voltage ranging from 2.7 V to 3.0 V.
- Battery power (V_{BAT}) for backup domain when V_{LDOIN} is shut down. (Unavailable for HT32F1251B)
- 40 bytes of backup registers powered by V_{BAK} for data storage of user application data when in the Power-Down mode.

Functional Descriptions

Backup Domain

Power Switch

The Backup Domain is powered by the 3.3V power source (V_{LDOIN}) or the battery power source (V_{BAT}) selected by the power switch PWRSW. The operating voltage of the power switch ranges from 2.7V to 3.6V. If V_{LDOIN} is lower than V_{BAT}, then the power source will be switched from V_{LDOIN} to V_{BAT}. Therefore, even if V_{LDOIN} is powered down, all the circuitry in the backup domain can operate normally. This means that the backup register contents will be retained, the RTC circuitry will operate normally and the low speed oscillators can keep running.

Backup Domain Reset

The Backup Domain reset sources include the Backup Domain power-on-reset (PORB), and the Backup Domain software reset which is activated by setting the BAKRST bit in the BAKCR register. The PORB signal forces the device to stay in the reset mode until V_{BAK} is greater than 1.36 V. The slew rate of the PORB signal is approximately V_{BAK}/100ms. Also the application software can trigger the Backup Domain software reset by setting the BAKRST bit in the BAKCR register to reset the Backup domain. All registers of the PWRCU and the RTC will be reset only by the Backup Domain reset.

LSE, LSI, and RTC

The Real Time Clock circuitry clock source can be derived from either the Low Speed Internal RC oscillator, LSI, or the Low Speed External Crystal oscillator, LSE. Before entering the power saving mode by executing the WFI/WFE instruction, the Cortex™-M3 needs to setup the compare register with an expected wakeup time and enable the wakeup function to achieve the RTC timer wakeup event. After entering the power saving mode for a certain amount of time, the Compare Match flag, CMFLAG, will be asserted to wakeup the device when the compare match event occurs. The details of the RTC configuration for wakeup timer will be described in the RTC chapter.

Backup Registers and Isolation Cells

Ten 32-bit registers, up to 40 bytes, are located in the Backup Domain for user application data storage. These registers are powered by V_{BAK} which constantly supplies power when the 1.8 V power is switched off. The Backup Registers are only reset by the Backup Domain power-on-reset, PORB, or the Backup Domain software reset, BAKRST. When the device resumes operation from the 1.8 V power, either by Hardware or Software, access to the Backup registers and the RTC registers are disabled by the isolation cells which protect these registers against possible parasitic write accesses. To resume access operations, users can disable these isolated cells by setting the BAKISO bit in the LPCR register of the Clock Control Unit to 1.

LDO Power Control

The LDO will be automatically switched off when one of the following conditions occurs:

- The Power-Down or Deep-Sleep2 mode is entered
- The control bits BODEN = 1, BODRIS=0 and the supply power $V_{LDOIN} \leq 2.5$ V

The LDO will be automatically switched on by hardware if any of the following conditions occurs:

- Resume operation from the power saving mode - RTC wakeup, LVD wakeup, or WAKEUP pin rising edge.
- Detect a falling edge on the external reset pin (nRST)
- The control bit BODEN = 1 and the supply power $V_{LDOIN} > 2.5$ V

To enter the Deep-Sleep1 mode, the PWRCU will request the LDO to operate in a low current mode, LCM. To enter the Deep-Sleep2 mode, the PWRCU will turn off the LDO and then turn on the DMOS to supply an alternative 1.8 V power.

3.3 V Power Domain

Voltage Regulator

The voltage regulator, LDO, Depletion MOS, DMOS, Low voltage Detector, LVD, the Brown out Detector, BOD and High Speed Internal oscillator, HSI, all operate under the 3.3 V power domain. The LDO can be configured to operate in either normal mode (LDOOFF=0, SLEEPDEEP=0, I=200mA) or low current mode (LDOOFF=0, SLEEPDEEP=1, I= 100 mA) to supply the 1.8 V power. An alternative 1.8 V power source is the output of the DMOS which has low leakage and drive current characteristics. It is controlled using the DMOSON bit in the BAKCR register. The DMOS output has weak drive current capability, and can operate only in the Deep-Sleep2 mode for data retention purposes in the V_{DD18} power domain.

Low Voltage Detector/Brown Out Detector

The Brown Out Detector, BOD, is used to detect if the 3.3 V supply voltage is equal to or lower than 2.5V. When the BODEN bit in the LVDCSR register is set to 1 and the 3.3 V supply voltage is lower than 2.5V then the BODF flag will be active. The PWRCU will regard this as a power down reset situation and then immediately disable the internal LDO regulator (when BODRIS=0) or issue an interrupt to notify the Cortex™-M3 to execute a user power down procedure (when BODRIS=1). The Low Voltage Detector, LVD, can also detect whether the 3.3 V supply voltage is lower than a programmable threshold voltage ranging from 2.7V to 3.0V. It is selected by the LVDS bits in the LVDCSR register. When a low voltage on the V_{LDOIN} power pin is detected, the LVDF flag will be active and an interrupt will be generated and sent to the Cortex™-M3 if the LVDEN and LVDIWEN bits in the LVDCSR register are set.

High Speed Internal Oscillator

The High Speed Internal Oscillator, HSI, is located in the 3.3V power domain. When exiting from the Deep-Sleep mode, the HSI clock can be configured as the system clock for a certain period by setting the PSRCEN bit to 1. This bit is located in the Global Clock Control Register, GCCR, in the Clock Control Unit, CKCU. The system clock will not be switched to the original clock source used before entering the Deep-Sleep mode until the original clock source, which may be either sourced from the PLL or HSE, stabilises. Also the system will force the HSI oscillator to be the system clock after a wake up from the Power-Down mode since a 1.8V power on reset will occur.

1.8V Power Domain

The main functions that include the APB interface for the backup domain, 1.8V power on reset (POR), Cortex™-M3 logic, AHB/APB peripherals, etc., are located in this power domain. Once the 1.8V is powered up, the POR will generate a reset sequence (Refer to PORB) on the 1.8V power domain. Subsequently, to enter the expected power saving mode, the associated control bits including the LDOOFF, DMOSON and SLEEPDEEP bits must be configured. Then, once a WFI or WFE instruction is executed, the device will enter an expected power saving mode which will be discussed in the following section.

Operation Modes

Run Mode

In the Run mode, the system operates with full functions and all power domains are active. There are two ways to reduce the power consumption in this mode. The first is to slow down the system clock by setting the AHBPRE field in the CKCU AHBCFGR register, and the second is to turn off the unused peripheral clock by setting the APBCCR0 and APBCCR1 registers. Reducing the system clock speed before entering the sleep mode will also help to minimize power consumption.

Additionally, there are several power saving modes to provide maximum optimisation between device performance and power consumption.

Table 11. Operation Mode Definitions

Type	Mode name	Hardware Action
Operating	Run	After system reset, Cortex™-M3 fetches instructions to execute.
Power Saving	Sleep	1. Cortex™-M3 core clock will be stopped. 2. Peripherals, Flash and SRAM clocks can be stopped.
	Deep-Sleep	1. Stop all clocks in the 1.8 V power domain. 2. Disable HSI, HSE, and PLL. 3. Reduce the 1.8 V power domain current by turning on the LDO low current mode or DMOS.
	Power-Down	Shut down the 1.8 V power domain

Sleep Mode

By default, only the Cortex™-M3 clock will be stopped in the Sleep mode. Clearing the FMCEN or SRAMEN bit in the CKCU AHBCCR register to 0 will have the effect of stopping the Flash clock or SRAM clock after the system enters the Sleep mode. If it is not necessary for the CPU to access the Flash memory and SRAM in the Sleep mode, it is recommended to clear the FMCEN and SRAMEN bits in the AHBCCR register to minimize power consumption. To enter the Sleep mode, it only needs to clear the SLEEPDEEP bit to 0 and execute a WFI or WFE instruction. The system will exit from the Sleep mode via any interrupt or event trigger. Table 12 provides more information regarding the power saving modes.

Table 12. Enter / Exit Power Saving Modes

Mode	Mode Entry				Mode Exit
	Cortex™-M3 Instruction	Cortex™-M3 SLEEPDEEP	LDOOFF	DMOSON	
Sleep	WFI or WFE (Takes effect)	0	X	X	WFI: Any interrupt WFE: Any wakeup event(NOTE 1) or … Any interrupt (NVIC on) or … Any interrupt with SEVONPEND = 1 (NVIC off)
Deep-Sleep1		1	0	0	Any EXTI in event mode or RTC wakeup or LVD wakeup or WAKEUP pin rising edge
Deep-Sleep2		1	X	1	RTC wakeup or LVD wakeup(NOTE 2) or WAKEUP pin rising edge
Power-Down		1	1	0	RTC wakeup or LVD wakeup(NOTE 2) or WAKEUP pin rising edge or External reset (nRST)

NOTES: 1. Wakeup event means the EXTI line in the event mode, RTC, LVD, and WAKEUP pin rising edge.

2. If the system allows LVD activity to wake it up after the system has entered the power saving mode. The LVDIWEN and LVDEN bits in the LVDCSR register have to be enabled to make sure the LDO regulator can be turn-on when system is woken up from the Deep-Sleep2 and Power-Down mode.

Deep-Sleep Mode

To enter the Deep-Sleep mode, configure the registers as shown in Table 12 and execute the WFI or WFE instruction. In the Deep-Sleep mode, all clocks including PLL and high speed oscillator, known as HSI and HSE, will be stopped. In addition, Deep-Sleep1 turns the LDO into low current mode while Deep-Sleep2 turns off the LDO and uses a DMOS to keep 1.8V power. Once the PWRCU receives a wakeup event or an interrupt as shown in Mode Exit of Table 12, the LDO will then operate in the normal mode and the high speed oscillator will be enabled. Finally, the Cortex™-M3 will return to the Run mode to handle the wakeup interrupt if required. A Low Voltage Detection also can be regarded as a wakeup event if the corresponding wakeup control bit LVDIWEN in the LVDCSR register is enabled. The last wakeup event is a transition from low to high on the external WAKEUP pin sent to the PWRCU to resume from the Deep-Sleep mode. During the Deep-Sleep mode, retaining the register and memory contents will shorten the wakeup latency.

Power-Down Mode

The Power-Down mode is derived from the Deep-Sleep mode of the Cortex™-M3 together with the additional control bits LDOOFF and DMOSON. To enter the Power-Down mode, users can configure the registers as shown in Table 12 and execute the WFI or WFE instruction. A RTC wakeup trigger event, a LVD wakeup, a low to high transition on the external WAKEUP pin or an external reset (nRST) signal will force the micro controller out of the Power-Down mode. In the Power-Down mode, the 1.8V power supply will be turned off. The remaining active power supplies are the 3.3V I/O power (V_{DD33}) and the Backup Domain power (V_{BAK}).

After a system reset, the PDF and BAKPORF bits in the BAKSR register should be checked by software to confirm if the device is being resumed from the Power-Down mode, a backup domain power on reset or an unexpected loss of the 1.8V power or other reset (nRST, WDT,...). If the device has entered the Power-Down mode under the correct firmware procedure, then the PDF bit will be set. The system information could be saved in the Backup Registers and be retrieved when the 1.8V power domain is powered on again. More information regarding the PDF and BAKPORF bits in the BAKSR register is shown in Table 13.

Table 13. Power Status After System Reset

PDF	BAK_PORF	Description
0	1	Power-up for the first time after the backup domain is reset: Power on reset when V_{BAK} is applied for the first time or executing a software reset command on the backup domain.
0	0	Restart from an unexpected loss of the 1.8 V power or other reset (nRST, WDT,...)
1	0	Restart from the Power-Down mode.
1	1	Reserved

Register Map

The following table shows the PWRCU registers and reset values. Note all the registers in this unit are located in the V_{BAK} backup power domain.

Table 14. Register Map of PWRCU

Register	Offset	Description	Reset Value
PWRCU Base Address = 0x4006_A000			
BAKSR	0x100	Backup Domain Status Register	0x0000_0001
BAKCR	0x104	Backup Domain Control Register	0x0000_0000
BAKTEST	0x108	Backup Domain Test Register	0x0000_0027
HSIRCR	0x10C	HSI Ready Counter Control Register	0x0000_0003
LVDCSR	0x110	Low Voltage/Brown Out Detect Control and Status Register	0x0000_0000
BAKREG0	0x200	Backup Register 0	0x0000_0000
BAKREG1	0x204	Backup Register 1	0x0000_0000
BAKREG2	0x208	Backup Register 2	0x0000_0000
BAKREG3	0x20C	Backup Register 3	0x0000_0000
BAKREG4	0x210	Backup Register 4	0x0000_0000
BAKREG5	0x214	Backup Register 5	0x0000_0000
BAKREG6	0x218	Backup Register 6	0x0000_0000
BAKREG7	0x21C	Backup Register 7	0x0000_0000
BAKREG8	0x220	Backup Register 8	0x0000_0000
BAKREG9	0x224	Backup Register 9	0x0000_0000

Register Descriptions

Backup Domain Status Register (BAKSR)

This register indicates the backup domain status.

Offset: 0x100

Reset value: 0x0000_0001 (Reset only by Backup Domain reset)

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							WUPF
Type/Reset								RC 0
	7	6	5	4	3	2	1	0
	Reserved						PDF	BAKPORF
Type/Reset							RC 0	RC 1

Bits	Field	Descriptions
[8]	WUPF	External WAKEUP Pin Flag 0: the WAKEUP pin is not asserted 1: the WAKEUP pin is asserted This bit is set by hardware when the WAKEUP pin asserts and is cleared by a software read. Software should read this bit to clear it after a system wake up from the power saving mode.
[1]	PDF	Power Down Flag 0: Wakeup from abnormal V_{DD18} shutdown (Loss of V_{DD18} is unexpected) 1: Wakeup from the Power-Down mode. The loss of V_{DD18} is under expectation. This bit is set by hardware when the system has successfully entered the Power-Down mode.
[0]	BAKPORF	Backup Domain Reset Flag 0: Backup Domain reset does not occur 1: Backup Domain reset occurs This bit is set by hardware when a Backup Domain reset occurs, either a Backup Domain power on reset or Backup Domain software reset. The bit is cleared by a software read. This bit must be cleared after the system is first powered up, otherwise it will be impossible to detect when a Backup Domain reset has been triggered. When this bit is read as 1, a read software loop must be implemented until the bit returns again to 0. This software loop is necessary to confirm that the Backup Domain is ready for access. It must be implemented after the Backup Domain is first powered up.

Backup Domain Control Register (BAKCR)

This register provides the power control bits for the Deep-Sleep and Power-Down mode.

Offset: 0x104

Reset value: 0x0000_0000 (Reset only by Backup Domain reset)

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	DMOSSTS	Reserved		V18RDYSC	Reserved		WUPIEN	WUPEN
Type/Reset	RO 0			RW 0			RW 0	RW 0
	7	6	5	4	3	2	1	0
	DMOSON	Reserved			LDOOFF	Reserved		BAKRST
Type/Reset	RW 0				RW 0			WO 0

Bits	Field	Description
[15]	DMOSSTS	DMOS Status This bit is set to 1 if the DMOSON bit in this register has been set to 1. This bit is cleared to 0 if the DMOSON bit has been set to 0 or if a BOD reset occurred.
[12]	V18RDYSC	V_{DD18} Ready Source Selection. Setting this bit to determine what control signal of isolation cells is used to disable the isolation function of the V18 to V33 domain level shifter. 0: BKISO bit in the LPCR register located in the CKCU 1: V_{DD18} POR
[9]	WUPIEN	External WAKEUP Pin Interrupt Enable 0: Disable WAKEUP pin interrupt function 1: Enable WAKEUP pin interrupt function The software can set the WUPIEN bit to 1 to assert the LPWUP interrupt in the NVIC unit when the WUPEN and WUPF bits are both set to 1.
[8]	WUPEN	External WAKEUP Pin Enable 0: Disable WAKEUP pin function. 1: Enable WAKEUP pin function. The software can set WUPEN as 1 to enable the WAKEUP pin function before entering the power saving mode. When WUPEN = 1, a rising edge on the WAKEUP pin wakes up the system from the power saving mode. For the WAKEUP pin is active high, the pin should be set as input pull down mode. The corresponding registers which should be properly set are PBPD[10] to 1 in the PBPDR register, PBPU[10] to 0 in the PBPUR register and the PBCFG10 field to 0x01 in the GPBCFGR register. **NOTE:** This bit is reset by a system reset or by a Backup Domain reset. Because this bit is located in the Backup Domain, after reset activity there will be a delay until the bit is active. The bit will not be active until the system reset finished and the Backup Domain ISO signal has been disabled. This means that the bit can not be immediately set by software after a system reset finished and the Backup domain ISO signal disabled. The delay time needed is a minimum of three 32KHz clock periods until the bit reset activity has finished.

Bits	Field	Description
[7]	DMOSON	DMOS Control 0: DMOS is OFF 1: DMOS is ON. A DMOS is implemented to provide an alternative voltage source for the 1.8 V power domain when the Cortex™-M3 enters the Deep-Sleep mode (SLEEPDEEP = 1). The control bit DMOSON is set by software and cleared by software or PORB. If the DMOSON bit is set to 1, the LDO will automatically be turned off when the Cortex™-M3 enters the Deep-Sleep mode.
[3]	LDOOFF	LDO Operating Mode Control 0: The LDO operates in a low current mode when the Cortex™-M3 enters the Deep-Sleep mode (SLEEPDEEP = 1). The V_{DD18} power is available. 1: The LDO is turned off when the Cortex™-M3 enters the Deep-Sleep mode (SLEEPDEEP = 1). The V_{DD18} power is not available. **NOTE:** This bit is only available when the DMOSON bit is cleared to 0.
[0]	BAKRST	Backup Domain Software Reset 0: No action 1: Backup Domain Software Reset is activated - includes all the related RTC and PWRCU registers.

Backup Domain Test Register (BAKTEST)

This register specifies a read-only value for the software to recognize whether the backup domain is ready for access.

Offset: 0x108

Reset value: 0x0000_0027

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	BAKTEST							
Type/Reset	RO 0	RO 0	RO 1	RO 0	RO 0	RO 1	RO 1	RO 1

Bits	Field	Descriptions
[7:0]	BAKTEST	Backup Domain Test Bits A constant value of 0x27 will be read when the Backup Domain is ready for Cortex™-M3 access.

HSI Ready Counter Control Register (HSIRCR)

This register specifies the counter bit length of HSI ready counter.

Offset: 0x10C

Reset value: 0x0000_0003

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved						HSIRCBL	
Type/Reset							RW 1	RW 1

Bits	Field	Descriptions
[1:0]	HSIRCBL	HSI Ready Counter Bit Length 00: 7 bits 01: 8 bits 10: 9 bits 11: 10 bits HSIRCBL specifies the bit length of HSI ready counter. Software can set HSIRCBL to shorten the startup waiting time of HSI before entering Deep-Sleep mode or Power-Down mode. (HSICRBL is reset only by Backup Domain reset)

Low Voltage/Brown Out Detect Control and Status Register (LVDCSR)

This register specifies the flags, enable bits and option bits for the Low Voltage Detector and Brown Out Detector.

Offset: 0x110

Reset value: 0x0000_0000 (Reset only by Backup Domain reset)

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved			LVDIWEN	LVDF		LVDS	LVDEN
Type/Reset				RW 0	RO 0	RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved				BODF	Reserved	BODRIS	BODEN
Type/Reset					RO 0		RW 0	RW 0

Bits	Field	Descriptions
[20]	LVDIWEN	LVD Interrupt or Wakeup LDO Enable 0: LVD interrupt or wakeup is disabled 1: LVD interrupt or wakeup is enabled Set this bit to 1 to enable the LVD interrupt in the CPU run mode or to enable a wakeup LDO from Deep-Sleep1, Deep-Sleep2, or Power-Down mode when the LVDF bit is asserted.
[19]	LVDF	Low Voltage Detect Status Flag 0: Low Voltage event has not occurred (V_{DD33} is higher than the specific voltage level) 1: Low Voltage event occured (V_{DD33} is equal to or lower than the specific voltage level) When the LVDF flag is asserted, an interrupt will be generated and sent to the Cortex™-M3 if the LVDIWEN bit is set to 1.
[18:17]	LVDS	Low Voltage Detect Level Selection 00: 2.7 V nominal - default value 01: 2.8 V nominal 10: 2.9 V nominal 11: 3.0 V nominal
[16]	LVDEN	Low Voltage Detect Enable 0: Disable Low Voltage Detect 1: Enable Low Voltage Detect Set this bit to 1 to wakeup the CPU from power saving mode when 3.3 V power is lower than the voltage set by LVDS bits. Therefore when the bit is enabled before the system is into the Deep-Sleep2 (DMOS is turn on and LDO is power down) or Power-Down mode (DMOS and LDO are power down). Then LVDIWEN bit has to be enabled to avoid the LDO is not active in the meantime when the CPU is woken up by the low voltage detection activity.
[3]	BODF	Brow Out Detection Flag If V_{DD33} < 2.5 V, BODF = 1. Otherwise, BODF = 0.

Bits	Field	Descriptions
[1]	BODRIS	BOD Reset or Interrupt Selection 0: Reset the whole device 1: Generate Interrupt
[0]	BODEN	Brown Out Detect Enable 0: Disable Brown Out Detect 1: Enable Brown Out Detect

Backup Register n (BAKREGn, n = 0 ~ 9)

This register specifies the backup register n for storing data during the V_{DD18} power-off period.

Offset: 0x200 ~ 0x224

Reset value: 0x0000_0000 (Reset only by Backup Domain reset)

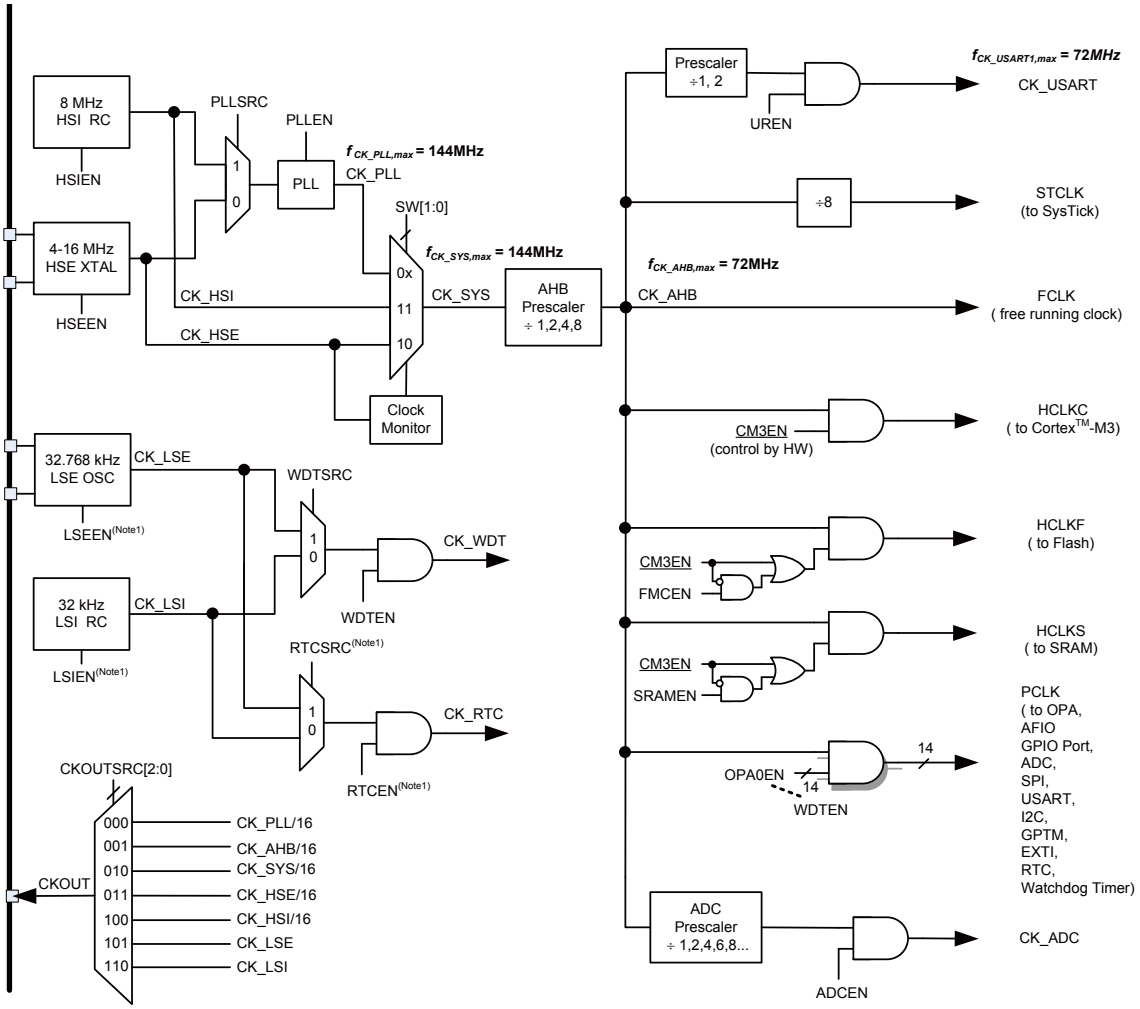
	31	30	29	28	27	26	25	24
	BAKREGn							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	BAKREGn							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	BAKREGn							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	BAKREGn							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[31:0]	BAKREGn	Backup Register n (n = 0 ~ 9) These registers are used for general purpose data storage. The contents of the BAKREGn register will remain even if the V_{DD18} power is lost.

6 Clock Control Unit (CKCU)

Introduction

The Clock Control unit, CKCU, provides a range of frequencies and clock functions. These include a High Speed Internal RC oscillator (HSI), a High Speed External crystal oscillator (HSE), a Low Speed Internal RC oscillator (LSI), a Low Speed External crystal oscillator (LSE), a Phase Lock Loop (PLL), a HSE clock monitor, clock prescalers, clock multiplexers and clock gating circuitry. The clocks of the AHB, APB and Cortex™-M3 are derived from the system clock (CK_SYS) which can source from the HSI, HSE or PLL. The Watchdog Timer and Real Time Clock (RTC) use either the LSI or LSE as their clock source. The maximum operating frequency of the system core clock (CK_AHB) can be up to 72 MHz. (**NOTE:** LSE is not supported by HT32F1251B).



Legend: HSE = High Speed External clock
HSI = High Speed Internal clock
LSE = Low Speed External clock
LSI = Low Speed Internal clock

NOTES: 1. Control bits LSIEN, LSEEN, RTCEN and RTCSRC are located at RTC Control Register (RTCCR).
2. HT32F1251B does not include the VBAT, XTAL32KIN and XTAL32KOUT pins.

Figure 12. CKCU Block Diagram

Some of the internal clocks can also be wired out via the CKOUT pin for debugging purposes. The clock monitor circuit can be used to detect an HSE clock failure. Once the HSE clock has ceased to operate, for whatever reason, the CKCU will force the system clock source to switch to the HSI clock to prevent a system halt from occurring.

Features

- 4 to 16 MHz High Speed External crystal oscillator (HSE)
- 8 MHz High Speed Internal RC oscillator (HSI)
- 32,768 Hz Low Speed External crystal oscillator (LSE)
- 32 kHz Low Speed Internal RC oscillator (LSI)
- PLL clock source can be HSE or HSI
- HSE clock monitor

Functional Descriptions

High Speed External Crystal Oscillator (HSE)

The high speed external crystal oscillator (HSE), which has a frequency from 4 to 16 MHz, produces a highly accurate clock source for use as the system clock. A crystal with a specific frequency must be connected and located close to the two HSE pins, XTALIN / XTALOUT. The external resistor and capacitor components connected to the crystal are necessary for proper oscillation.

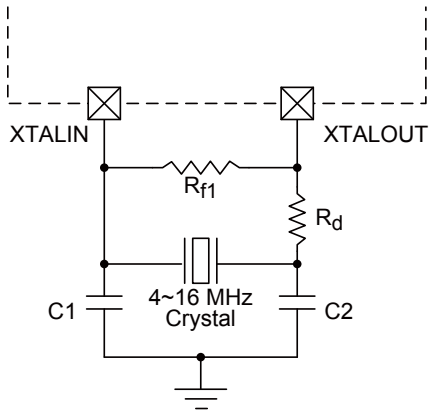


Figure 13. External HSE Crystal, Ceramic, and Resonator

The HSE crystal oscillator can be switched on or off using the HSEEN bit in the Global Clock Control Register GCCR. The HSERDY flag in the Global Clock Status Register GCSR indicates if the high-speed external crystal oscillator is stable. When the HSE is powered up, it will not be released for use until this HSERDY bit is set by the hardware. This specific delay period is known as the oscillator “Start-up time”. As the HSE becomes stable, an interrupt will be generated if the related interrupt enable bit HSERDYIE in the Global Clock Interrupt Register GCIR is set. At this point the HSE clock can be used directly as the system clock source or the PLL input clock.

High Speed Internal RC Oscillator (HSI)

The high speed internal RC oscillator, HSI, has a fixed frequency of 8 MHz and is the default clock source selection for the CPU when the device is powered up. The HSI oscillator provides a lower cost type clock source as no external components are required. The HSI RC oscillator can be switched on or off using the HSIEN bit in the Global Clock Control Register GCCR. The HSIRDY flag in the Global Clock Status Register GCSR is used to indicate if the internal RC oscillator is stable. The start-up time of the HSI oscillator is shorter than the HSE crystal oscillator. An interrupt can be generated if the related interrupt enable bit, HSIRDYIE, in the Global Clock Interrupt Register, GCIR, is set when the HSI becomes stable. The HSI clock can also be used as the PLL input clock.

The frequency accuracy of the HSI can be calibrated by the manufacturer, but its operating frequency is still less accurate than HSE. The application requirements, environment and cost will determine which oscillator type is selected.

If the HSE or PLL is the system clock source, to minimise the time required for the system to recover from the Deep-Sleep Mode, the software can set the PSRCEN bit (Power Saving Wakeup RC Clock Enable) to 1 to force the HSI clock to be the system clock when the system initially wakes-up. Subsequently, the system clock will automatically be switched back to the original clock source, HSE or PLL, when the original clock source ready flag is asserted. This function will reduce the wakeup time when using the HSE or PLL as the system clock.

Phase Locked Loop (PLL)

The internal Phase Locked Loop, PLL, can provide 8~144 MHz clock output which is 2 ~36 multiples of a fundamental reference frequency of 4 ~ 16 MHz. The PLL includes a reference divider, feedback dividers, a digital phase frequency detector (PD), a current-controlled charge pump (CP), an internal loop filter and a voltage-controlled oscillator (VCO) to achieve a stable phase-locked state.

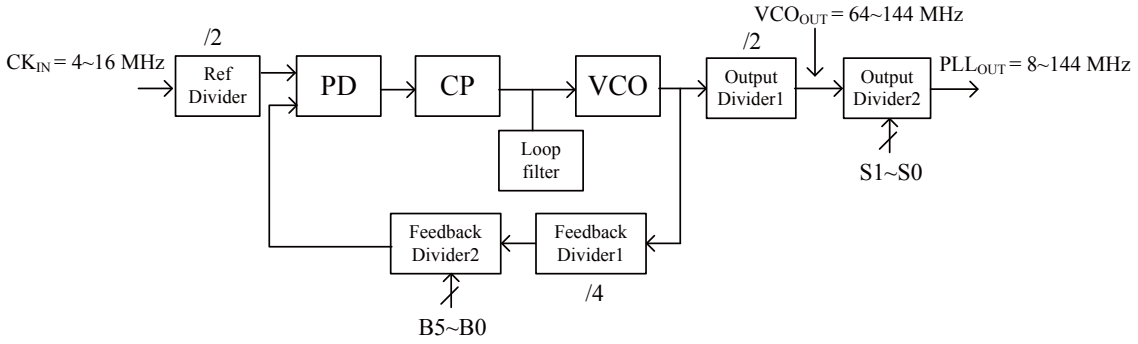


Figure 14. PLL Block Diagram

The PLL output clock frequency can be determined by the following formula:

$$PLL_{OUT} = CK_{IN} * \frac{NF1 * NF2}{NR * NO1 * NO2} = CK_{IN} * \frac{4 * NF2}{2 * 2 * NO2} = CK_{IN} * \frac{NF2}{NO2}$$

, where NR=Ref divider=2, NF1=Feedback divider1=4, NF2=Feedback divider2=1~64,

NO1 = Output divider1 = 2, NO2 = Output divider2 = 1, 2, 4, or 8

Consider a duty cycle of 50% and where both input and output frequencies are divided by 2. If a given clock PLL input clock source frequency, CK_{in}, generates a specific PLL output frequency, then it is recommended to use a higher value for NF2 in order to increase PLL stability and reduce jitter at the expense of settling time. The setup bits of the output and feedback divider2 are described in Table 15 and Table 16. All the setup bits named S1~S0 and B5~B0 in Table 15 and Table 16 are defined in the PLL Configuration Register PLLCFGR and the PLL Control Register PLLCR in the Register Definition section. Note that the VCO_{OUT} frequency must have a range from 64 MHz to 144 MHz. If the selected configuration exceeds this range, the PLL output frequency cannot be guaranteed to match the above PLL_{OUT} formula.

The PLL can be switched on or off by using the PLLEN bit in the Global Clock Control Register GCCR. The PLLRDY flag in the Global Clock Status Register GCSR will indicate if the PLL clock is stable. An interrupt can be generated if the related interrupt enable bit, PLLRDYIE, in the Global Clock Interrupt Register, GCIR, is set as the PLL becomes stable.

Table 15. Output Divider 2 Setting

Output divider 2 setup bits S1~S0 (POTD bits in the PLLCFGR register)	NO2 (Output divider2 value)
00	1
01	2
10	4
11	8

Table 16. Feedback Divider 2 Setting

Feedback divider 2 setup bits B5~B0 (PFBD bits in the PLLCFGR register)	NF2 (Feedback divider2 value)
000000	64
000001	1
000010	2
000011	3
000100	4
000101	5
000110	6
000111	7
001000	8
001001	9
001010	10
001011	11
001100	12
001101	13
001110	14
• • •	• • •
111111	63

Low Speed External Crystal Oscillator (LSE)

The low speed external crystal or ceramic resonator oscillator, which has a frequency of 32,768 Hz, produces a low power but highly accurate clock source for the Real Time Clock circuit or the Watchdog Timer. The crystal or ceramic resonator must be located close to the two LSE pins, XTAL32KIN and XTAL32KOUT. Their external resistor and capacitor components are necessary for proper oscillation. The LSE oscillator can be switched on or off using the LSEEN bit in the RTC Control Register RTCCR. The LSERDY flag in the Global Clock Status Register GCSR will indicate if the LSE clock is stable. An interrupt can be generated if the related interrupt enable bit, LSERDYIE, in the Global Clock Interrupt Register GCIR is set when the LSE becomes stable.

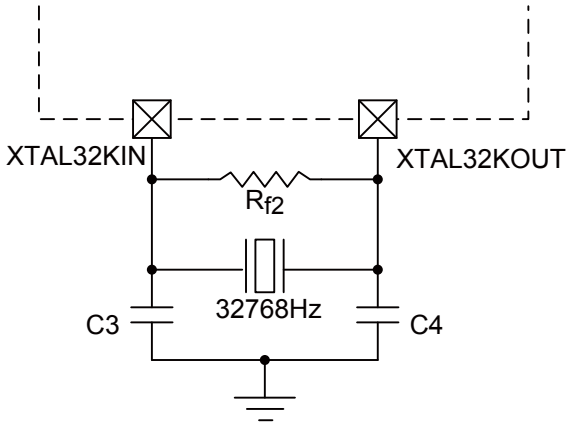


Figure 15. External Crystal, Ceramic, and Resonator for LSE

Low Speed Internal RC Oscillator (LSI)

The low speed internal RC oscillator has a frequency of about 32 kHz and is a low power clock source for the Real Time Clock circuit or the Watchdog Timer. The LSI offers a low cost clock source as no external components are required. The LSI RC oscillator can be switched on or off by using the LSIEN bit in the RTC Control Register, RTCCR. The frequency accuracy can be calibrated using the configuration options. The LSIRDY flag in the Global Clock Status Register GCSR will indicate if the LSI clock is stable. An interrupt can be generated if the related interrupt enable bit LSIRDYIE in the Global Clock Interrupt Register GCIR is set when the LSI becomes stable.

System Clock (CK_SYS) Selection

After the system reset, the default CK_SYS source will be HSI and can be switched to HSE or PLL by changing the System Clock Switch bits, SW, in the Global Clock Control Register, GCCR. When the SW value is changed, the CK_SYS will continue to operate using the original clock source until the target clock source is stable. The corresponding clock ready status is in the Global Clock Status Register, GCSR and the clock source usage can be found in the Clock Source Status Register, CKST. When a clock source is used directly by the CK_SYS or the PLL, it is not possible to stop it.

HSE Clock Monitor

The HSE clock monitor function is enabled by the HSE Clock Monitor Enable bit, CKMEN, in the Global Clock Control Register, GCCR. This function should be enabled after the HSE start-up delay and disabled when the HSE is stopped. Once the HSE failure is detected, the HSE will be automatically disabled. The HSE Clock Stuck Flag, CKSF, in the Global Clock Interrupt Register, GCIR, will be set and the HSE failure event will be generated if the Clock Stuck Interrupt Enable bit, CKSIE, in the GCIR register is set. This failure interrupt is connected to the Non-Maskable Interrupt, NMI, of the Cortex-M3. If the HSE is selected as the clock source of CK_SYS or PLL, the HSE failure will force the CK_SYS source to HSI and the PLL will be disabled automatically.

Clock Output Capability

The clock output capability of HT32 series MCU is ranging from 32 kHz to 9 MHz. There are several clock signals can be selected via the CKOUT Clock Source Selection bits, CKOUTSRC, in the Global Clock Configuration Register, GCFGR. The corresponding GPIO pin should be configured in the properly Alternate Function I/O (AFIO) mode to output the selected clock signal.

Table 17. CKOUT Clock Source

CKOUTSRC	Clock Source
000	CK_PLL / 16
001	HCLK / 16
010	CK_SYS / 16
011	CK_HSE / 16
100	CK_HSI / 16
101	CK_LSE
110	CK_LSI
111	Reserved

Register Map

The following table shows the CKCU registers and their reset value.

Table 18. Register Map of CKCU

Register	Offset	Description	Reset Value
CKCU Base Address = 0x4008_8000			
GCFGR	0x000	Global Clock Configuration Register	0x0000_0102
GCCR	0x004	Global Clock Control Register	0x0000_0803
GCSR	0x008	Global Clock Status Register	0x0000_0028
GCIR	0x00C	Global Clock Interrupt Register	0x0000_0000
PLLCFGR	0x018	PLL Configuration Register	0x0000_0000
PLLCR	0x01C	PLL Control Register	0x0000_0000
AHBCFGR	0x020	AHB Configuration Register	0x0000_0000
AHBCCR	0x024	AHB Clock Control Register	0x0000_0005
APBCFGR	0x028	APB Configuration Register	0x0000_0000
APBCCR0	0x02C	APB Clock Control Register 0	0x0000_0000
APBCCR1	0x030	APB Clock Control Register 1	0x0000_0000
CKST	0x034	Clock Source Status Register	0x0100_0000
LPCR	0x300	Low Power Control Register	0x0000_0000
MCUDBGCR	0x304	MCU Debug Control Register	0x0000_0000

Register Descriptions

Global Clock Configuration Register (GCFGR)

This register specifies the clock source for the PLL/USART/Watchdog Timer/CKOUT circuits.

Offset: 0x000

Reset value: 0x0000_0102

	31	30	29	28	27	26	25	24
	LPMOD			Reserved				
Type/Reset	RO 0	RO 0	RO 0					
	23	22	21	20	19	18	17	16
	Reserved		URPRE		Reserved			
Type/Reset		RW 0	RW 0					
	15	14	13	12	11	10	9	8
	Reserved							PLLSRC
Type/Reset								RW 1
	7	6	5	4	3	2	1	0
	Reserved				WDTSRC	CKOUTSRC		
Type/Reset					RW 0	RW 0	RW 1	RW 0

Bits	Field	Descriptions
[31:29]	LPMOD	Lower Power Mode Status Set and reset by hardware. 000: Device in run mode 001: Device wants to enter Sleep mode 010 :Device wants to enter Deep Sleep mode1 011: Device wants to enter Deep Sleep mode2 100: Device wants to enter Power Down mode Others: Reserved
[21:20]	URPRE	USART Clock Prescaler Selection Set and reset by software to control the USART clock prescaler value. 00:CK_USART = CK_UR 01: CK_USART = CK_UR / 2 Others: Reserved
[8]	PLLSRC	PLL Clock Source Selection Set and reset by software to control the PLL clock source. 0: External 4 ~ 16 MHz crystal oscillator clock is selected (HSE) 1: Internal 8 MHz RC oscillator clock is selected (HSI)
[3]	WDTSRC	Watchdog Timer Clock Source Selection Set and reset by software to control the Watchdog Timer clock source. 0: Internal LSI 32 kHz RC oscillator clock selected 1: External LSE 32,768 Hz crystal oscillator clock selected

Bits	Field	Descriptions
[2:0]	CKOUTSRC	CKOUT Clock Source Selection Set and reset by software. 000: (CK_PLL / 16) selected 001: (CK_AHB / 16) selected 010: (CK_SYS / 16) selected 011: (CK_HSE / 16) selected 100: (CK_HSI / 16) selected 101: CK_LSE selected 110: CK_LSI selected 111: Reserved

Global Clock Control Register (GCCR)

This register specifies the clock enable bits.

Offset: 0x004

Reset value: 0x0000_0803

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved						PSRCEN	CKMEN
Type/Reset							RW 0	RW 0
	15	14	13	12	11	10	9	8
	Reserved				HSIEN	HSEEN	PLLEN	Reserved
Type/Reset					RW 1	RW 0	RW 0	
	7	6	5	4	3	2	1	0
	Reserved							SW
Type/Reset							RW 1	RW 1

Bits	Field	Descriptions
[17]	PSRCEN	Power Saving Wakeup RC Clock Enable 0: No action. 1: Use HSI as the temporary CK_SYS source after waking up from Deep-Sleep1 or Deep-Sleep2. When the PSRCEN bit is set to 1, the HSI will be used as the clock source of CK_SYS after waking up from the Deep-Sleep1 or Deep-Sleep2 mode. This means that the instruction can be executed early before the original CK_SYS source such as HSE or PLL is stable.
[16]	CKMEN	HSE Clock Monitor Enable 0: Disable the External 4 ~ 16 MHz crystal oscillator (HSE) clock monitor 1: Enable the External 4 ~ 16 MHz crystal oscillator (HSE) clock monitor When the hardware detects that the HSE clock is stuck at a low or high state, the internal hardware will switch the system clock to be the internal high speed HSI RC clock. The way to recover the original system clock is by either an external reset, power on reset or clearing CKSF by software. **NOTE:** When the HSE clock monitor is enabled, the hardware will automatically enable the HSI internal RC oscillator regardless of the control bit, HSIEN, state.
[11]	HSIEN	Internal High Speed oscillator Enable Set and reset by software. This bit can not be reset if the HSI clock is used as the system clock. 0: Internal 8 MHz RC oscillator disabled 1: Internal 8 MHz RC oscillator enabled
[10]	HSEEN	External High Speed oscillator Enable Set and reset by software. This bit can not be reset if the HSE clock is used as the system clock or the PLL input clock. 0: External 4 ~ 16 MHz crystal oscillator disabled 1: External 4 ~ 16 MHz crystal oscillator enabled

Bits	Field	Descriptions
[9]	PLLEN	PLL Enable Set and reset by software. This bit cannot be reset if the PLL clock is used as the system clock. 0: PLL is switched off 1: PLL is switched on
[1:0]	SW	System Clock Switch 0X: Select CK_PLL as the CK_SYS source 10: Select CK_HSE as the CK_SYS source 11: Select CK_HSI as the CK_SYS source Set by software to select the CK_SYS source. Because the change of CK_SYS has inherent latency, software should read these bits to confirm whether the switching is complete or not. The switch will be forced to HSI by HSE clock monitor when the HSE failure is detected and the HSE is selected as the clock source of CK_SYS or PLL.

Global Clock Status Register (GCSR)

This register indicates the clock ready status.

Offset: 0x008

Reset value: 0x0000_0028

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
		Reserved	LSIRDY	LSERDY	HSIRDY	HSERDY	PLLRDY	Reserved
Type/Reset			RO 1	RO 0	RO 1	RO 0	RO 0	

Bits	Field	Descriptions
[5]	LSIRDY	LSI Internal Low Speed Oscillator Ready Flag Set by hardware to indicate if the LSI oscillator is stable and ready for use. 0: LSI oscillator not ready 1: LSI oscillator ready
[4]	LSERDY	LSE External Low Speed Oscillator Ready Flag Set by hardware to indicate if the LSE oscillator is stable and ready for use. 0: LSE oscillator not ready 1: LSE oscillator ready
[3]	HSIRDY	HSI High Speed Internal Oscillator Ready Flag Set by hardware to indicate if the HSI oscillator is stable and ready for use. 0: HSI oscillator not ready 1: HSI oscillator ready
[2]	HSERDY	HSE High Speed External Clock Ready Flag Set by hardware to indicate if the HSE oscillator is stable and ready for use. 0: HSE oscillator not ready 1: HSE oscillator ready
[1]	PLLRDY	PLL Clock Ready Flag Set by hardware to indicate if the PLL output clock is stable and ready for use. 0: PLL not ready 1: PLL ready

Global Clock Interrupt Register (GCIR)

This register specifies the interrupt enable and flag bits.

Offset: 0x00C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved	LSIRDYIE	LSERDYIE	HSIRDYIE	HSERDYIE	PLLRDYIE	Reserved	CKSIE
Type/Reset		RW 0	RW 0	RW 0	RW 0	RW 0		RW 0
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved	LSIRDYF	LSERDYF	HSIRDYF	HSERDYF	PLLRDYF	Reserved	CKSF
Type/Reset		WC 0	WC 0	WC 0	WC 0	WC 0		WC 0

Bits	Field	Descriptions
[22]	LSIRDYIE	LSI Ready Interrupt Enable LSI stabilization interrupt enable/disable control 0: Disable the LSI stabilization interrupt 1: Enable the LSI stabilization interrupt
[21]	LSERDYIE	LSE Ready Interrupt Enable LSE stabilization 0: Disable the LSE stabilization interrupt 1: Enable the LSE stabilization interrupt
[20]	HSIRDYIE	HSI Ready Interrupt Enable Set and reset by software to enable/disable the HSI stabilization interrupt 0: Disable the HSI stabilization interrupt 1: Enable the HSI stabilization interrupt
[19]	HSERDYIE	HSE Ready Interrupt Enable Set and reset by software to enable/disable the HSE stabilization interrupt 0: Disable the HSE stabilization interrupt 1: Enable the HSE stabilization interrupt
[18]	PLLRDYIE	PLL Ready Interrupt Enable Set and reset by software to enable/disable the PLL stabilization interrupt 0: Disable the PLL stabilization interrupt 1: Enable the PLL stabilization interrupt
[16]	CKSIE	Clock Stuck Interrupt Enable Set and reset by software to enable/disable the clock monitor interrupt 0: Disable the clock fail interrupt 1: Enable the clock fail interrupt

Bits	Field	Descriptions
[6]	LSIRDYF	LSI Ready Interrupt Flag Reset by software - write 1 to clear. Set by hardware when the Internal 32 kHz RC oscillator clock is stable and the LSIRDYIE bit is set. 0: No LSI stabilization clock ready interrupt generated 1: LSI stabilization interrupt generated
[5]	LSERDYF	LSE Ready Interrupt Flag Reset by software - write 1 to clear. Set by hardware when the External 32,768 Hz crystal oscillator clock is stable and the LSERDYIE bit is set. 0: No LSE stabilization interrupt generated 1: LSE stabilization interrupt generated
[4]	HSIRDYF	HSI Ready Interrupt Flag Reset by software - write 1 to clear. Set by hardware when the Internal 8 MHz RC oscillator clock is stable and the HSIRDYIE bit is set. 0: No HSI stabilization interrupt generated 1: HSI stabilization interrupt generated
[3]	HSERDYF	HSE Ready Interrupt Flag Reset by software - write 1 to clear. Set by hardware when the External 4 ~ 16 MHz crystal oscillator clock is stable and the HSERDYIE bit is set. 0: No HSE stabilization interrupt generated 1: HSE stabilization interrupt generated
[2]	PLLRDYF	PLL Ready Interrupt Flag Reset by software - write 1 to clear. Set by hardware when the PLL is stable and the PLLRDYIE bit is set. 0: No PLL stabilization interrupt generated 1: PLL stabilization interrupt generated
[0]	CKSF	HSE Clock Stuck Interrupt Flag Reset by software - write 1 to clear. Set by hardware when the HSE clock is stuck and the CKSIE bit is set. 0: Clock operating normally 1: HSE clock stuck

PLL Configuration Register (PLLCFGR)

This register specifies the PLL configuration.

Offset: 0x018

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved			PFBD [5:1]				
Type/Reset				RW 0	RW 0	RW 0	RW 0	RW 0
	23	22	21	20	19	18	17	16
	PFBD[0]		POTD	Reserved				
Type/Reset	RW 0	RW 0	RW 0					
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved							
Type/Reset								

Bits	Field	Descriptions
[28:23]	PFBD	PLL VCO Output Clock Feedback Divider (B5 ~ B0 in Figure 14) Feedback Divider divides the output clock from the PLL VCO.
[22:21]	POTD	PLL Output Clock Divider (S1 ~ S0 in Figure 14)

PLL Control Register (PLLCR)

This register specifies the PLL Bypass mode.

Offset: 0x01C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	PLLBPS	Reserved						
Type/Reset	RW 0							
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved							
Type/Reset								

Bits	Field	Descriptions
[31]	PLLBPS	PLL Bypass Mode Enable 0: Disable the PLL Bypass mode 1: Enable the PLL Bypass mode in which the PLL output clock PLLOUT is equal to the CK_{IN} clock (refer to Figure 14)

AHB Configuration Register (AHBCFGR)

This register specifies the system clock frequency.

Offset: 0x020

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved						AHBPRE	
Type/Reset							RW 0	RW 0

Bits	Field	Descriptions
[1:0]	AHBPRE	AHB Pre-Scaler Set and reset by software to control the AHB clock division ratio. 00: CK_AHB = CK_SYS 01: CK_AHB = CK_SYS / 2 10: CK_AHB = CK_SYS / 4 11: CK_AHB = CK_SYS / 8

AHB Clock Control Register (AHBCCR)

This register specifies the AHB clock enable bits.

Offset: 0x024

Reset value: 0x0000_0005

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved					SRAMEN	Reserved	FMCEN
Type/Reset						RW 1		RW 1

Bits	Field	Descriptions
[2]	SRAMEN	SRAM Clock Enable Set and reset by software. Clear the SRAMEN bit to 0 to reduce power consumption if the SRAM is unused in the Sleep mode. 0: SRAM clock disabled in Sleep mode 1: SRAM clock enabled in Sleep mode
[0]	FMCEN	Flash Memory Controller Clock Enable Set and reset by software. Clear the FMCEN bit to 0 to reduce power consumption if the Flash Memory is unused in the Sleep mode. 0: FMC clock disabled in Sleep mode 1: FMC clock enabled in Sleep mode

APB Configuration Register (APBCFGR)

This register specifies the ADC clock frequency.

Offset: 0x028

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved					ADCDIV		
Type/Reset						RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved							
Type/Reset								

Bits	Field	Descriptions
[18:16]	ADCDIV	ADC Clock Frequency Division Select Set and reset by software to control the ADC clock division ratio. 000: CK_ADC = CK_AHB 001: CK_ADC = (CK_AHB / 2) 010: CK_ADC = (CK_AHB / 4) 011: CK_ADC = (CK_AHB / 8) 100: CK_ADC = (CK_AHB / 16) 101: CK_ADC = (CK_AHB / 32) 110: CK_ADC = (CK_AHB / 64) 111: CK_ADC = (CK_AHB / 6)

APB Clock Control Register 0 (APBCCR0)

This register specifies the APB clock enable bits.

Offset: 0x02C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved						PBEN	PAEN
Type/Reset							RW 0	RW 0
	15	14	13	12	11	10	9	8
	EXTIEN	AFIOEN	Reserved					UREN
Type/Reset	RW 0	RW 0						RW 0
	7	6	5	4	3	2	1	0
	Reserved			SPIEN	Reserved			I2CEN
Type/Reset				RW 0				RW 0

Bits	Field	Descriptions
[17]	PBEN	GPIO Port B Clock Enable Set and reset by software. 0: Port B clock disabled 1: Port B clock enabled
[16]	PAEN	GPIO Port A Clock Enable Set and reset by software. 0: Port A clock disabled 1: Port A clock enabled
[15]	EXTIEN	External Interrupt Clock Enable Set and reset by software. 0: EXTI clock disabled 1: EXTI clock enabled
[14]	AFIOEN	Alternate Function I/O Clock Enable Set and reset by software. 0: AFIO clock disabled 1: AFIO clock enabled
[8]	UREN	USART Clock Enable Set and reset by software. 0: USART clock disabled 1: USART clock enabled
[4]	SPIEN	SPI Clock Enable Set and reset by software. 0: SPI clock disabled 1: SPI clock enabled
[0]	I2CEN	I^2C Clock Enable Set and reset by software. 0: I^2C clock disabled 1: I^2C clock enabled

APB Clock Control Register 1 (APBCCR1)

This register specifies the APB clock enable bits.

Offset: 0x030

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							ADCEN
Type/Reset								RW 0
	23	22	21	20	19	18	17	16
	OPA1EN	OPA0EN	Reserved					
Type/Reset	RW 0	RW 0						
	15	14	13	12	11	10	9	8
	Reserved						GPTM1EN	GPTM0EN
Type/Reset							RW 0	RW 0
	7	6	5	4	3	2	1	0
	Reserved	RTCEN	Reserved	WDTEN	Reserved			
Type/Reset		RW 0		RW 0				

Bits	Field	Descriptions
[24]	ADCEN	ADC Clock Enable Set and reset by software. 0: ADC clock disabled 1: ADC clock enabled
[23]	OPA1EN	OPA/CMP 1 Clock Enable Set and reset by software. 0: OPA/CMP 1 clock disabled 1: OPA/CMP 1 clock enabled
[22]	OPA0EN	OPA/CMP 0 Clock Enable Set and reset by software. 0: OPA /CMP 0 clock disabled 1: OPA /CMP 0 clock enabled
[9]	GPTM1EN	GPTM1 Clock Enable Set and reset by software. 0: GPTM1 clock disabled 1: GPTM1 clock enabled
[8]	GPTM0EN	GPTM0 Clock Enable Set and reset by software. 0: GPTM0 clock disabled 1: GPTM0 clock enabled
[6]	RTCEN	RTC Clock Enable Set and reset by software. 0: RTC clock disabled 1: RTC clock enabled
[4]	WDTEN	Watchdog Timer Clock Enable Set and reset by software. 0: Watchdog Timer clock disabled 1: Watchdog Timer clock enabled

Clock Source Status Register (CKST)

This register specifies the clock source status.

Offset: 0x034

Reset value: 0x0100_0000

	31	30	29	28	27	26	25	24
	Reserved					HSIST		
Type/Reset						RO 0	RO 0	RO 1
	23	22	21	20	19	18	17	16
	Reserved							HSEST
Type/Reset							RO 0	RO 0
	15	14	13	12	11	10	9	8
	Reserved							PLLST
Type/Reset								RO 0
	7	6	5	4	3	2	1	0
	Reserved							
Type/Reset								

Bits	Field	Descriptions
[26:24]	HSIST	High Speed Internal Clock Occupation Status (CK_HSI) xx1: HSI used by System Clock (CK_SYS) (SW = 0x03) x1x: HSI used by PLL 1xx: HSI used by Clock Monitor
[17:16]	HSEST	High Speed External Clock Occupation Status (CK_HSE) x1: HSE used by System Clock (CK_SYS) (SW = 0x02) 1x: HSE used by PLL
[8]	PLLST	PLL Clock Occupation Status 0: PLL not used by System Clock (CK_SYS) 1: PLL used by System Clock (CK_SYS)

Low Power Control Register (LPCR)

This register specifies the low power control bit.

Offset: 0x300

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved							BKISO
Type/Reset								RW 0

Bits	Field	Descriptions
[0]	BKISO	Backup Domain Isolation Control Set and reset by software. Refer to the Power Control Unit chapter for more information. 0: Backup domain isolated from other power domains 1: Backup domain accessible by other power domains

MCU Debug Control Register (MCUDBGCR)

This register specifies the MCU debug control.

Offset: 0x304

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved	DBDSLP2	Reserved			DBSPI	Reserved	DBUSART
Type/Reset		RW 0				RW 0		RW 0
	7	6	5	4	3	2	1	0
	DBGPTM1	DBGPTM0	Reserved		DBWDT	DBPD	DBDSLP1	DBSLP
Type/Reset	RW 0	RW 0			RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[14]	DBDSLP2	Debug Deep-Sleep mode 2 Set and reset by software. 0: LDO = Off, DMOS = On, FCLK = Off and HCLK = Off in Deep-Sleep2 1: LDO = On, FCLK = On and HCLK = On in Deep-Sleep mode 2
[10]	DBSPI	SPI Debug Mode Enable Set and reset by software. This bit is used to control whether the SPI timeout mode is stopped or not when the core is halted. 0: Same behavior as normal mode 1: SPI FIFO timeout is stopped
[8]	DBUSART	USART Debug Mode Enable Set and reset by software. This bit is used to control whether the USART timeout mode is stopped or not when the core is halted. 0: Same behavior as normal mode 1: USART RX FIFO timeout is stopped
[7]	DBGPTM1	GPTM1 Debug Mode Enable Set and reset by software. This bit is used to control whether the GPTM1 counter is stopped or not when the core is halted. 0: GPTM1 counter keeps counting even if the core is halted 1: GPTM1 counter is stopped when the core is halted
[6]	DBGPTM0	GPTM0 Debug Mode Enable Set and reset by software. This bit is used to control whether the GPTM0 counter is stopped or not when the core is halted. 0: GPTM0 counter keeps counting even if the core is halted 1: GPTM0 counter is stopped when the core is halted
[3]	DBWDT	Watchdog Timer Debug Mode Enable Set and reset by software. This bit is used to control whether the Watchdog Timer Counter is stopped or not when the core is halted. 0: Watchdog Timer counter keeps counting even if the core is halted 1: Watchdog Timer counter is stopped when the core is halted

Bits	Field	Descriptions
[2]	DBPD	Debug Power-Down Mode Set and reset by software. 0: LDO = Off, FCLK = Off and HCLK = Off in Power-Down mode 1: LDO = On, FCLK = On and HCLK = On in Power-Down mode
[1]	DBDSLP1	Debug Deep-Sleep mode 1 Set and reset by software. 0: LDO = Low power mode, FCLK = Off and HCLK = Off in Deep-Sleep1 1: LDO = On, FCLK = On and HCLK = On in Deep-Sleep mode 1
[0]	DBSLP	Debug Sleep Mode Set and reset by software. 0: LDO = On, FCLK = On and HCLK = Off in Sleep mode 1: LDO = On, FCLK = On and HCLK = On in Sleep mode

7 Reset Control Unit (RSTCU)

Introduction

The Reset Control Unit (RSTCU) has three kinds of reset, the power on reset, system reset and APB unit reset. The power on reset, known as a cold reset, resets the full system during a power up. A system reset resets the processor core and peripheral IP components with the exception of the SW-DP controller. The resets can be triggered by an external signal, internal events and the reset generators. More information about these resets will be described in the following section.

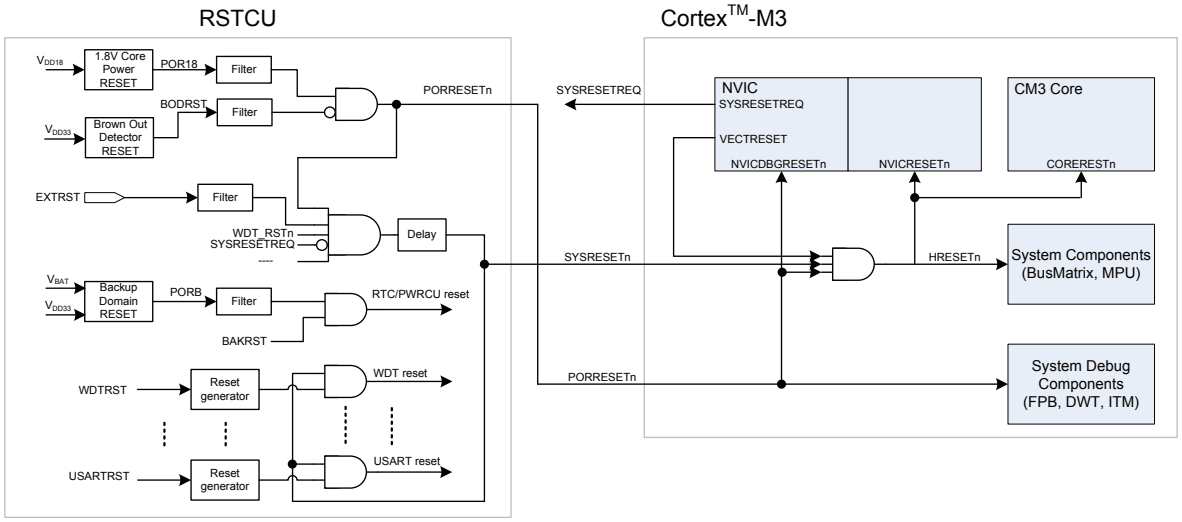
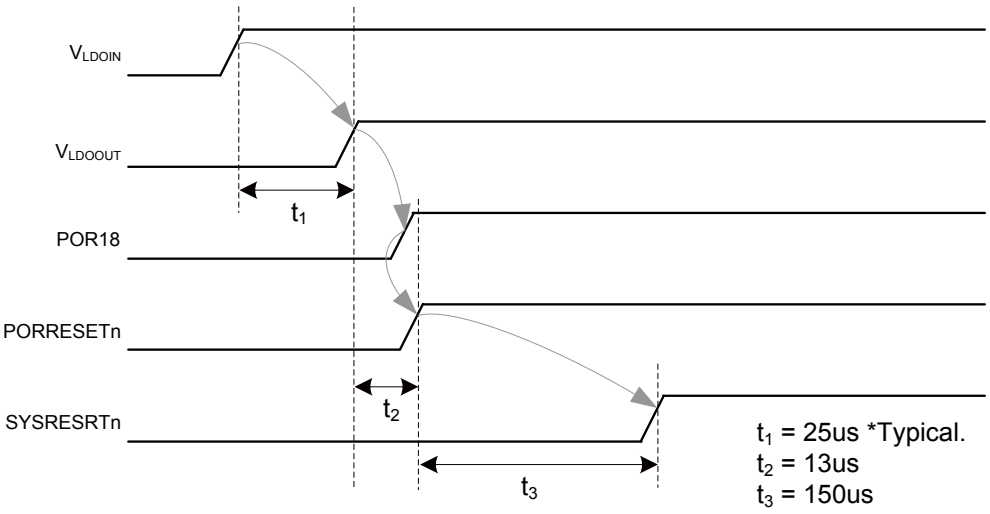


Figure 16. RSTCU Block Diagram

Functional Descriptions

Power On Reset

The Power on reset, POR, is generated by either an external reset or by the internal reset generator. Both types have an internal filter to prevent glitches from causing erroneous reset operations. By referring to Figure 16, the POR18 active low signal will be de-asserted when the internal LDO voltage regulator is ready to provide 1.8 V power. In addition to the POR18 signal, the Power Control Unit (PWRCU) will assert the BODRST signal as a Power Down Reset, PDR, when the BODEN bit in the LVDCSR register is set and the brown-out event occurs. For more details about the PWRCU function, refer to the PWRCU chapter.



* This timing is dependent on the internal LDO regulator output capacitor value.

Figure 17. Power On Reset Sequence

System Reset

A System reset is generated by a power on reset (PORRESETn), a Watchdog Timer reset (WDT_RSTn), an NVIC reset (NVICRESETn) or a software reset (VECTREST) event. For more information about the Watchdog Timer and NVIC reset events, refer to the related chapter in the Cortex™-M3 reference manual.

APB Unit Reset

An APB unit reset can be divided into hardware and software resets. A hardware reset can be generated by either a power on reset or a system reset for all APB units. Each functional IP connected to the APB can be reset individually through the associated software reset bits in the RSTCU. For example, the application software can generate a USART reset via the URRST bit in the APBPRSTR0 register to reset the USART circuits.

Register Map

The following table shows the RSTCU registers and reset values.

Table 19. Register Map of RSTCU

Register	Offset	Description	Reset Value
RSTCU Base Address = 0x4008_8000			
GRSR	0x100	Global Reset Status Register	0x0000_0008
APBPRSTR0	0x108	APB Peripheral Reset Register 0	0x0000_0000
APBPRSTR1	0x10C	APB Peripheral Reset Register 1	0x0000_0000

Register Descriptions

Global Reset Status Register (GRSR)

This register specifies a variety of reset status conditions.

Offset: 0x100

Reset value: 0x0000_0008

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved				PORSTF	WDTRSTF	EXTRSTF	SYSRSTF
Type/Reset					WC 0	WC 0	WC 0	WC 0

Bits	Field	Descriptions
[3]	PORSTF	Core 1.8V Power On Reset Flag Set by hardware when a power on reset occurs. Reset by software - write 1 to clear. 0: No POR occurred 1: POR occurred
[2]	WDTRSTF	Watchdog Timer Reset Flag Set by hardware when a watchdog timer reset occurs. Reset by software - write 1 to clear or by hardware when a power on reset occurs. 0: No Watchdog Timer reset occurred 1: Watchdog Timer reset occurred
[1]	EXTRSTF	External Pin Reset Flag Set by hardware when an external pin reset occurs. Reset by software - write 1 to clear or by hardware when a power on reset occurs. 0: No pin reset occurred 1 : nRST Pin reset occurred
[0]	SYSRSTF	System Reset Flag Set by hardware when a system reset occurs. Reset by software - write 1 to clear or by hardware when a power on reset occurs. 0: No NVIC asserting system reset occurred 1: NVIC asserting system reset occurred

APB Peripheral Reset Register 0 (APBPRSTR0)

This register specifies the APB peripheral software reset.

Offset: 0x108

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved						PBRST	PARST
Type/Reset							RW 0	RW 0
	15	14	13	12	11	10	9	8
	EXTIRST	AFIORST	Reserved					URRST
Type/Reset	RW 0	RW 0						RW 0
	7	6	5	4	3	2	1	0
	Reserved			SPIRST	Reserved			I2CRST
Type/Reset				RW 0				RW 0

Bits	Field	Descriptions
[17]	PBRST	GPIO Port B Reset This bit is set by software and cleared to 0 by hardware automatically. 0: No reset 1: Reset Port B
[16]	PARST	GPIO Port A Reset This bit is set by software and cleared to 0 by hardware automatically. 0: No reset 1: Reset Port A
[15]	EXTIRST	External Interrupt Controller Reset This bit is set by software and cleared to 0 by hardware automatically. 0: No reset 1: Reset EXTI
[14]	AFIORST	Alternate Function I/O Reset This bit is set by software and cleared to 0 by hardware automatically. 0: No reset 1: Reset Alternate Function I/O
[8]	URRST	USART Reset This bit is set by software and cleared to 0 by hardware automatically. 0: No reset 1: Reset USART
[4]	SPIRST	SPI Reset This bit is set by software and cleared to 0 by hardware automatically. 0: No reset 1: Reset SPI
[0]	I2CRST	I^2C Reset This bit is set by software and cleared to 0 by hardware automatically. 0: No reset 1: Reset I^2C

APB Peripheral Reset Register 1 (APBPRSTR1)

This register specifies the APB peripheral software reset

Offset: 0x10C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							ADCRST
Type/Reset								RW 0
	23	22	21	20	19	18	17	16
	OPA1RST	OPA0RST	Reserved					
Type/Reset	RW 0	RW 0						
	15	14	13	12	11	10	9	8
	Reserved						GPTM1RST	GPTM0RST
Type/Reset							RW 0	RW 0
	7	6	5	4	3	2	1	0
	Reserved			WDTRST	Reserved			
Type/Reset				RW 0				

Bits	Field	Descriptions
[24]	ADCRST	ADC Reset This bit is set by software and cleared to 0 by hardware automatically. 0: No reset 1: Reset ADC
[23]	OPA1RST	Comparator/OPA 1 Controller Reset This bit is set by software and cleared to 0 by hardware automatically. 0: No reset 1: Reset CMP/OPA 1
[22]	OPA0RST	Comparator/OPA 0 Controller Reset This bit is set by software and cleared to 0 by hardware automatically. 0: No reset 1: Reset CMP/OPA 0
[9]	GPTM1RST	GPTM1 Reset This bit is set by software and cleared to 0 by hardware automatically. 0: No reset 1: Reset GPTM1
[8]	GPTM0RST	GPTM0 Reset This bit is set by software and cleared to 0 by hardware automatically. 0: No reset 1: Reset GPTM0
[4]	WDTRST	Watchdog Timer Reset This bit is set by software and cleared to 0 by hardware automatically. 0: No reset 1: Reset Watchdog Timer

8 General Purpose I/O (GPIO)

Introduction

There are up to 32 General Purpose I/O pins, (GPIO), named PA0 ~ PA15 and PB0 ~ PB15 for the device to implement logic input/output functions. Each of the GPIO ports has related control and configuration registers to satisfy the requirements of specific applications.

The GPIO ports are pin-shared with other alternative functions (AFs) to obtain maximum flexibility on the package pins.. The GPIO pins can be used as alternative functional pins by configuring the corresponding registers regardless of the AF input or output pins.

The external interrupts on the GPIO pins of the device have related control and configuration registers in the External Interrupt Control Unit (EXTI).

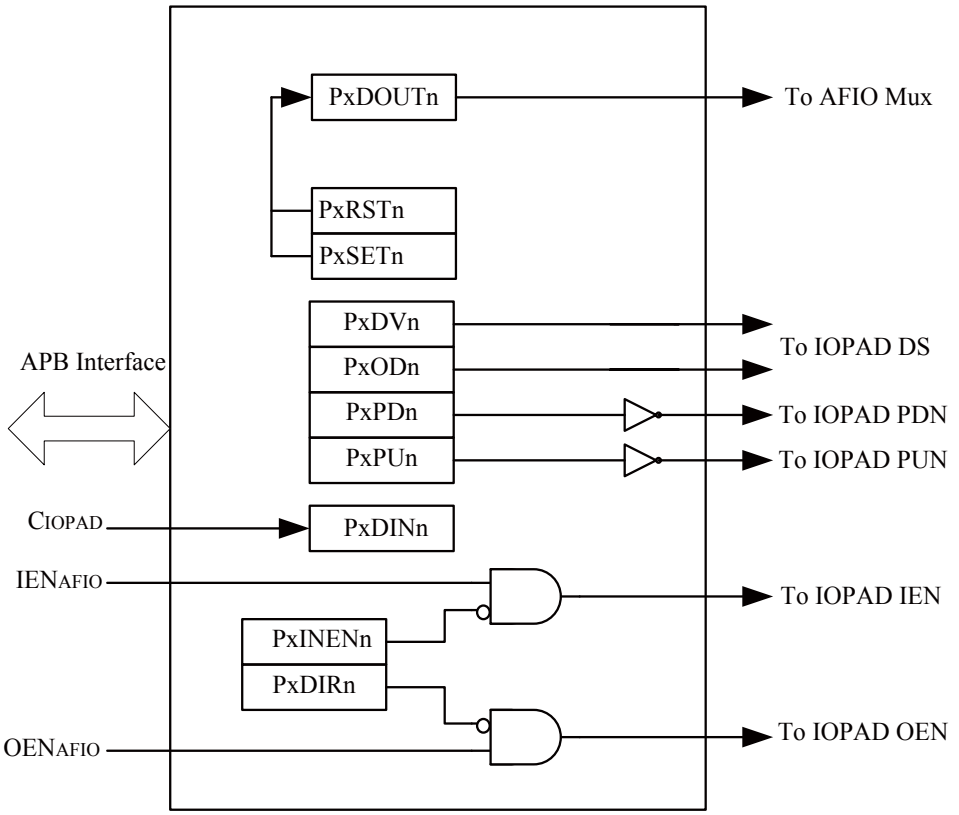


Figure 18. GPIO Block Diagram

Features

- Input/output direction control
- Schmitt Trigger Input function enable control
- Input pin weak pull-up/pull-down function
- Output push-pull/open drain enable control
- Output set/reset control
- Output drive current selection
- External interrupt with programmable trigger edge - using EXTI configuration registers
- Analog input/output configurations - using AFIO configuration registers
- Alternate function input/output configurations - using AFIO configuration registers
- Port configuration lock

Functional Descriptions

Default GPIO Pin Configuration

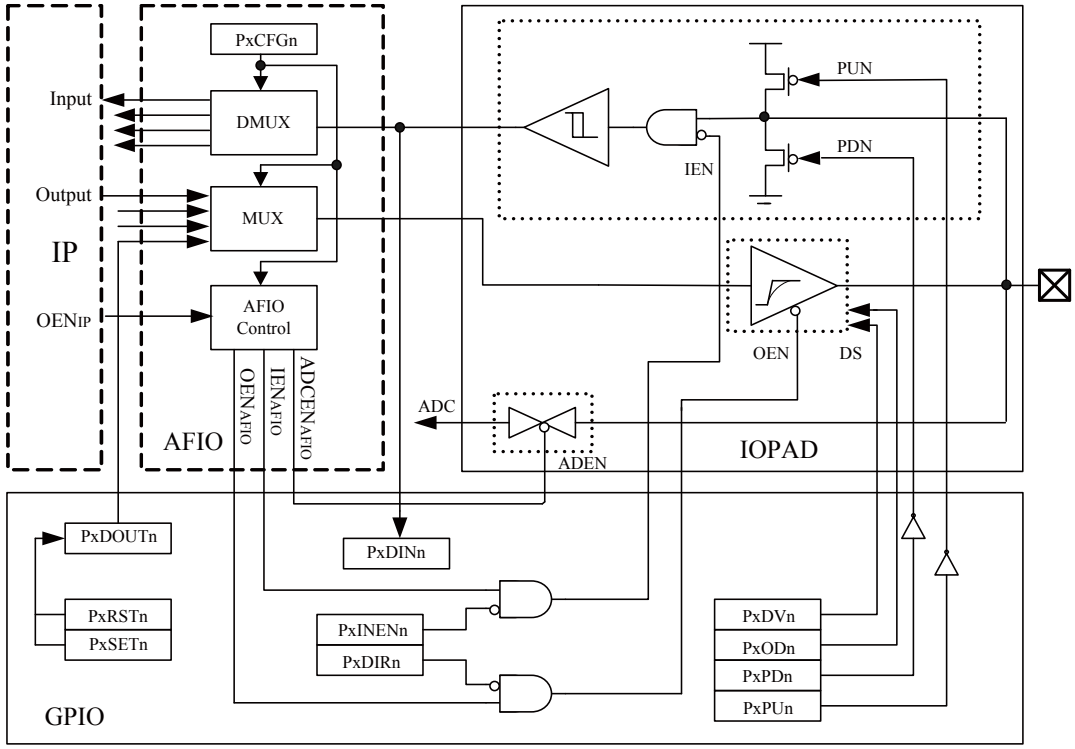
During or just after the reset period, the alternative functions are all inactive and the GPIO ports are configured into the input disable floating mode, i.e. input disabled without pull-up/pull-down resistors. Only the boot and Serial-Wired Debug pins which are pin-shared with the I/O pins PA9, PA10, PA13 and PA14 are active after a device reset.

- PA9/BOOT0: Input enable with internal pull-down
- PA10/BOOT1: Input enable with internal pull-up
- PA13/SWDIO: Input or output enable with internal pull-up
- PA14/SWCLK: Input enable with internal pull-up

General Purpose I/O (GPIO)

The GPIO pins can be configured as inputs or outputs via the data direction control registers PxDIRCR (where x is A or B). When the GPIO pins are configured as input pins, the data on the external pads can be read if the enable bits in the input enable function register PxINER are set. The GPIO pull-up/pull-down registers PxPUR/PxPDR can be configured to fit specific applications. When the pull-up and pull-down functions are both enabled, the pull-up function has the higher priority while the pull-down function will be blocked until the pull-up function is released.

The GPIO pins can be configured as output pins where the output data is latched into the data register PxDOUTR. The output type can be setup to be either push-pull or open-drain by the open drain selection register PxODR. Only one or several specific bits of the output data will be set or reset by configuring the port output set and reset control register PxSRR or the port output reset control register PxRR without affecting the unselected bits. As the port output set and reset functions are both enabled, the port output set function has the higher priority and the port output reset function will be blocked. The output driving current of the GPIO pins can be selected by configuring the drive current selection register PxDRVR.



PxDINn/PxDOUTn (x= A or B): Data Input/Data Output
PxRSTn/PxSETn (x= A or B): Reset/Set
PxDIRn (x= A or B): Direction
PxINENn (x= A or B): Input Enable
PxDVn (x= A or B): Output Drive
PxODn (x= A or B): Open Drain
PxPDn/PxPUn (x= A or B): Pull Down/Up
PxCFGn (x= A or B) AFIO Configuration

Figure 19. AFIO/GPIO Control Signal

Table 20. AFIO, GPIO, and IO Pad Control Signal Truth Table

Type	AFIO			GPIO		PAD		
	$ADCEN_{AFIO}$	OEN_{AFIO}	IEN_{AFIO}	PxDIRn	PxINENn	ADCEN	OEN	IEN
GPIO Input (Note)	1	1	1	0	1	1	1	0
GPIO Output (Note)	1	1	1	1	0 (1 if need)	1	0	1 (0)
AFIO Input	1	1	0	0	X	1	1	0
AFIO Output	1	0	1	X	0 (1 if need)	1	0	1 (0)
ADC Input	0	1	1	0	0 (1 if need)	0	1	1 (0)
OSC Output	0	1	1	0	0 (1 if need)	0	1	1 (0)

NOTE: The signals, IEN and OEN, for the I/O pads are derived from the GPIO register bits PxINENn and PxDIRn respectively when the associated pin is configured in the GPIO input/output mode.

GPIO Locking Mechanism

The GPIO also offers a lock function to lock the port until a reset event occurs. The PxLOCKR (x = A or B) registers are used to lock the port x and lock control options. The value 0x5FA0 is written into the PxLKEY field in the PxLOCKR register to freeze the PxDIRCR, PxINER, PxPUR, PxPDR, PxODR, PxDRVR control and AFIO mode configuration (GPxCFGR, where x = A or B). If the value in the PxLOCKR is 0x5FA0_0001, it means that the Port x Lock function is enabled and the Port x pin 0 is frozen.

Register Map

The following table shows the GPIO registers and reset values of Port A and Port B.

Table 21. Register Map of GPIO

Register	Offset	Description	Reset Value
GPIO A Base Address = 0x4001_A000			
PADIRCR	0x000	Port A Data Direction Control Register	0x0000_0000
PAINER	0x004	Port A Input Function Enable Control Register	0x0000_0600
PAPUR	0x008	Port A Pull-Up Selection Register	0x0000_6400
PAPDR	0x00C	Port A Pull-Down Selection Register	0x0000_0200
PAODR	0x010	Port A Open Drain Selection Register	0x0000_0000
PADRVR	0x014	Port A Drive Current Selection Register	0x0000_0000
PALOCKR	0x018	Port A Lock Register	0x0000_0000
PADINR	0x01C	Port A Data Input Register	0x0000_0000
PADOUTR	0x020	Port A Data Output Register	0x0000_0000
PASRR	0x024	Port A Output Set and Reset Control Register	0x0000_0000
PARR	0x028	Port A Output Reset Control Register	0x0000_0000
GPIO B Base Address = 0x4001_B000			
PBDIRCR	0x000	Port B Data Direction Control Register	0x0000_0000
PBINER	0x004	Port B Input Function Enable Control Register	0x0000_0000
PBPUR	0x008	Port B Pull-Up Selection Register	0x0000_0000
PBPDR	0x00C	Port B Pull-Down Selection Register	0x0000_0000
PBODR	0x010	Port B Open Drain Selection Register	0x0000_0000
PBDRVR	0x014	Port B Drive Current Selection Register	0x0000_0000
PBLOCKR	0x018	Port B Lock Register	0x0000_0000
PBDINR	0x01C	Port B Data Input Register	0x0000_0000
PBDOUTR	0x020	Port B Data Output Register	0x0000_0000
PBSRR	0x024	Port B Output Set and Reset Control Register	0x0000_0000
PBRR	0x028	Port B Output Reset Control Register	0x0000_0000

Register Descriptions

Port A Data Direction Control Register (PADIRCR)

This register is used to control the direction of the GPIO Port A pin as input or output.

Offset: 0x000

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	PADIR							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	PADIR							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	PADIRn	GPIO Port A pin n Direction Control Bits (n = 0 ~ 15) 0: Pin n in input mode 1: Pin n in output mode

Port A Input Function Enable Control Register (PAINER)

This register is used to enable or disable the GPIO Port A input function.

Offset: 0x004

Reset value: 0x0000_0600

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	PAINEN							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 1	RW 1	RW 0
	7	6	5	4	3	2	1	0
	PAINEN							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	PAINENn	GPIO Port A pin n Input Enable Control Bits (n = 0 ~ 15) 0: Pin n input function is disabled. 1: Pin n input function is enabled. When the pin n input function is disabled, the input Schmitt trigger will be turned off and the Schmitt trigger output will remain at a zero state.

Port A Pull-Up Selection Register (PAPUR)

This register is used to enable or disable the GPIO Port A pull-up function.

Offset: 0x008

Reset value: 0x0000_6400

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	Reserved							
Type/Reset								
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PAPU							
Type/Reset	RW 0	RW 1	RW 1	RW 0	RW 0	RW 1	RW 0	RW 0
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	PAPU							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	PAPUn	GPIO Port A pin n Pull-Up Selection Control Bits (n = 0 ~ 15) 0: Pin n pull-up function is disabled 1: Pin n pull-up function is enabled **NOTE:** When the pull-up and pull-down functions are both enabled, the pull-up function will have the higher priority and therefore the pull-down function will be blocked and disabled.

Port A Pull-Down Selection Register (PAPDR)

This register is used to enable or disable the GPIO Port A pull-down function.

Offset: 0x00C

Reset value: 0x0000_0200

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	Reserved							
Type/Reset								
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PAPD							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 1	RW 0
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	PAPD							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	PAPDn	GPIO Port A pin n Pull-Down Selection Control Bits (n = 0 ~ 15) 0: Pin n pull-down function is disabled 1: Pin n pull-down function is enabled **NOTE:** When the pull-up and pull-down functions are both enabled, the pull-up function will have the higher priority and thus the pull-down function will be blocked and disabled.

Port A Open Drain Selection Register (PAODR)

This register is used to enable or disable the GPIO Port A open drain function.

Offset: 0x010

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	Reserved							
Type/Reset								
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PAOD							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	PAOD							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	PAODn	GPIO Port A pin n Open Drain Selection Control Bits (n = 0 ~ 15) 0: Pin n Open Drain output is disabled. (The output type is CMOS output) 1: Pin n Open Drain output is enabled. (The output type is open-drain output)

Port A Output Current Drive Selection Register (PADRVR)

This register specifies the GPIO Port A output driving current.

Offset: 0x014

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	PADV							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[7:0]	PADVn	GPIO Port A pin n Output Current Drive Selection Control Bits (n = 0 ~ 7) 0: 4mA source/sink current 1: 8mA source/sink current

Port A Lock Register (PALOCKR)

This register specifies the GPIO Port A lock configuration.

Offset: 0x018

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	PALKEY							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	23	22	21	20	19	18	17	16
	PALKEY							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
	PALOCK							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	PALOCK							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[31:16]	PALKEY	GPIO Port A Lock Key 0x5FA0: Port A Lock function is enabled Others: Port A Lock function is disabled To lock the Port x function, a value 0x5FA0 should be written into the PxLKEY field in this register. To execute a successful write operation on this lock register, the value written into the PxLKEY field must be 0x5FA0. If the value written into this field is not equal to 0x5FA0, any write operations on the PxLOCKR register will be aborted. The result of a read operation on the PxLKEY field returns the GPIO Port x Lock Status which indicates whether the GPIO Port x is locked or not. If the read value of the PxLKEY field is 0, this indicates that the GPIO Port x Lock function is disabled. Otherwise, it indicates that the GPIO Port x Lock function is enabled as the read value is equal to 1.
[15:0]	PALOCKn	GPIO Port A Pin n Lock Control Bits (n = 0 ~ 15) 0: Port A Pin n is not locked 1: Port A Pin n is locked The PxLOCKn bits are used to lock the configurations of corresponding GPIO Pins when the correct Lock Key is applied to the PxLKEY field. The locked configurations include the PxDIRn, PxINENn, PxPUn, PxPDn, PxODn and PxDVn settings in the related GPIO registers. Additionally, the AFIO register GPxCFGR field which is used to configure the alternative function of the associated GPIO pin will also be locked. Note that the PxLOCKR register can only be written once which means that PxLKEY and PxLOCKn (lock control bit) should be written together and can not be changed until a system reset or a GPIO Port A reset occurs.

Port A Data Input Register (PADINR)

This register specifies the GPIO Port A input data.

Offset: 0x01C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	PADIN							
Type/Reset	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0
	7	6	5	4	3	2	1	0
	PADIN							
Type/Reset	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0

Bits	Field	Descriptions
[15:0]	PADINn	GPIO Port A Pin n Data Input Bits (n = 0 ~ 15) 0: The input data of pin n is 0 1: The input data of pin n is 1

Port A Output Data Register (PADOUTR)

This register specifies the GPIO Port A output data.

Offset: 0x020

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	PADOUT							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	PADOUT							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	PADOUTn	GPIO Port A Pin n Data Output Bits (n = 0 ~ 15) 0: Data to be output on pin n is 0 1: Data to be output on pin n is 1

Port A Output Set/Reset Control Register (PASRR)

This register is used to set or reset the corresponding bit of the GPIO Port A output data.

Offset: 0x024

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	PARST							
Type/Reset	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0
	23	22	21	20	19	18	17	16
	PARST							
Type/Reset	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0
	15	14	13	12	11	10	9	8
	PASET							
Type/Reset	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0
	7	6	5	4	3	2	1	0
	PASET							
Type/Reset	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0

Bits	Field	Descriptions
[31:16]	PARSTn	GPIO Port A Pin n Output Reset Control Bits (n = 0 ~ 15) 0: No effect on the PxDOUTn bit 1: Reset the PxDOUTn bit
[15:0]	PASETn	GPIO Port A Pin n Output Set Control Bits (n = 0 ~ 15) 0: No effect on the PxDOUTn bit 1: Set the PxDOUTn bit Note that the function enabled by the PxSETn bit has the higher priority if both the PxSETn and PxRSTn bits are set at the same time.

Port A Output Reset Register (PARR)

This register is used to reset the corresponding bit of the GPIO Port A output data.

Offset: 0x028

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	Reserved							
Type/Reset								
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PARST							
Type/Reset	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	PARST							
Type/Reset	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0

Bits	Field	Descriptions
[15:0]	PARSTn	GPIO Port A Pin n Output Reset Bits (n = 0 ~ 15) 0: No effect on the PxDOUTn bit 1: Reset the PxDOUTn bit

Port B Data Direction Control Register (PBDIRCR)

This register is used to control the direction of the GPIO Port B pin as input or output.

Offset: 0x000

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	PBDIR							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	PBDIR							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	PBDIRn	GPIO Port B pin n Direction Control Bits (n = 0 ~ 15) 0: Pin n is in input mode 1: Pin n is in output mode

Port B Input Function Enable Control Register (PBINER)

This register is used to enable or disable the GPIO Port B pin input function.

Offset: 0x004

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	Reserved							
Type/Reset								
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PBINEN							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	PBINEN							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	PBINENn	GPIO Port B pin n Input Enable Control Bits (n = 0 ~ 15) 0: Pin n input function is disabled. 1: Pin n input function is enabled. When the pin n input function is disabled, the input Schmitt trigger will be turned off and the Schmitt trigger output will remain at a zero state.

Port B Pull-Up Selection Register (PBPUR)

This register is used to enable or disable the GPIO Port B pull-up function.

Offset: 0x008

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	PBPU							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	PBPU							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	PBPUn	GPIO Port B pin n Pull-Up Selection Control Bits (n = 0 ~ 15) 0: Pin n pull-up function is disabled 1: Pin n pull-up function is enabled **NOTE:** When the pull-up and pull-down functions are both enabled, the pull-up function will have the higher priority and thus the pull-down function will be blocked and disabled.

Port B Pull-Down Selection Register (PBPDR)

This register is used to enable or disable the GPIO Port B pull-down function.

Offset: 0x00C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	Reserved							
Type/Reset								
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PBPD							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	PBPD							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	PBPDn	GPIO Port B pin n Pull-Down Selection Control Bits (n = 0 ~ 15) 0: Pin n pull-down function is disabled 1: Pin n pull-down function is enabled **NOTE:** When the pull-up and pull-down functions are both enabled, the pull-up function will have the higher priority and thus the pull-down function will be blocked and disabled.

Port B Open Drain Selection Register (PBODR)

This register is used to enable or disable the GPIO Port B open drain function.

Offset: 0x010

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	PBOD							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	PBOD							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	PBODn	GPIO Port B pin n Open Drain Selection Control Bits (n = 0 ~ 15) 0: Pin n Open Drain output is disabled - output type is CMOS 1: Pin n Open Drain output is enabled - output type is open-drain

Port B Output Current Drive Selection Register (PBDRVR)

This register specifies the GPIO Port B output driving current.

Offset: 0x014

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	PBDV							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[7:0]	PBDVn	GPIO Port B pin n Output Current Drive Selection Control Bits (n = 0 ~ 7) 0: 4mA source/sink current 1: 8mA source/sink current

Port B Lock Register (PBLOCKR)

This register specifies the GPIO Port B lock configuration.

Offset: 0x018

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	PBLKEY							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	PBLKEY							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PBLOCK							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	PBLOCK							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[31:16]	PBLKEY	GPIO Port B Lock Key 0x5FA0: Port B Lock function is enabled Others: Port B Lock function is disabled To lock the Port x function, a value 0x5FA0 should be written into the PxLKEY field in this register. To execute a successful write operation on this lock register, the value written into the PxLKEY field must be 0x5FA0. If the value written into this field is not equal to 0x5FA0, the write operation on the PxLOCKR register will be aborted. The result via a read operation on the PxLKEY field returns the GPIO Port x Lock Status which indicates whether the GPIO Port x is locked or not. If the read value of the PxLKEY field is 0, it indicates that the GPIO Port x Lock function is disabled. Otherwise, it indicates that the GPIO Port x Lock function is enabled as the read value is equal to 1.
[15:0]	PBLOCKn	GPIO Port B Pin n Lock Control Bits (n = 0 ~ 15) 0: Port B pin n is not locked 1: Port B pin n is locked The PxLOCKn bits are used to lock the configurations of corresponding GPIO Pins when the correct Lock Key is applied to the PxLKEY field. The locked configurations include the PxDIRn, PxINENn, PxPUn, PxPDn, PxODn and PxDVn settings in the related GPIO registers. Additionally, the AFIO register GPxCFGR field which is used to configure the alternative function of the associated GPIO pin will also be locked. Note that the PxLOCKR register can only be written once which means that PxLKEY and PxLOCKn (lock control bit) should be written together and can not be changed until a system reset or a GPIO Port B reset occurs.

Port B Data Input Register (PBDINR)

This register specifies the GPIO Port B input data.

Offset: 0x01C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	PBDIN							
Type/Reset	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0
	7	6	5	4	3	2	1	0
	PBDIN							
Type/Reset	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0

Bits	Field	Descriptions
[15:0]	PBDINn	GPIO Port B Pin n Data Input Bits (n = 0 ~ 15) 0: The input data of pin n is 0 1: The input data of pin n is 1

Port B Output Data Register (PBDOUTR)

This register specifies the GPIO Port B output data.

Offset: 0x020

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	PBDOUT							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	PBDOUT							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	PBDOUTn	GPIO Port B Pin n Data Output Bits (n = 0 ~ 15) 0: Data to be output on pin n is 0 1: Data to be output on pin n is 1

Port B Output Set/Reset Control Register (PBSRR)

This register is used to set or reset the corresponding bit of the GPIO Port B output data.

Offset: 0x024

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	PBRST							
Type/Reset	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0
	23	22	21	20	19	18	17	16
	PBRST							
Type/Reset	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0
	15	14	13	12	11	10	9	8
	PBSET							
Type/Reset	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0
	7	6	5	4	3	2	1	0
	PBSET							
Type/Reset	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0

Bits	Field	Descriptions
[31:16]	PBRSTn	GPIO Port B Pin n Output Reset Control Bits (n = 0 ~ 15) 0: No effect on the PxDOUTn bit 1: Reset the PxDOUTn bit
[15:0]	PBSETn	GPIO Port B Pin n Output Set Control Bits (n = 0 ~ 15) 0: No effect on the PxDOUTn bit 1: Set the PxDOUTn bit Note that the function enabled by the PxSETn bit has the higher priority if both the PxSETn and PxRSTn bits are set at the same time.

Port B Output Reset Register (PBRR)

This register is used to reset the corresponding bit of the GPIO Port B output data.

Offset: 0x028

Reset value: 0x0000_0000

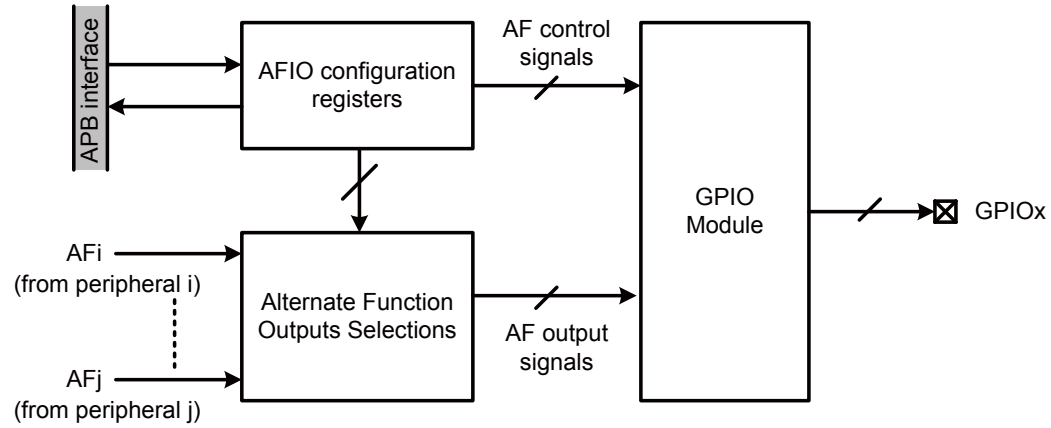
	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	PBRST							
Type/Reset	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0
	7	6	5	4	3	2	1	0
	PBRST							
Type/Reset	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0

Bits	Field	Descriptions
[15:0]	PBRSTn	GPIO Port B Pin n Output Reset Bits (n = 0 ~ 15) 0: No effect on the PxDOUTn bit 1: Reset the PxDOUTn bit

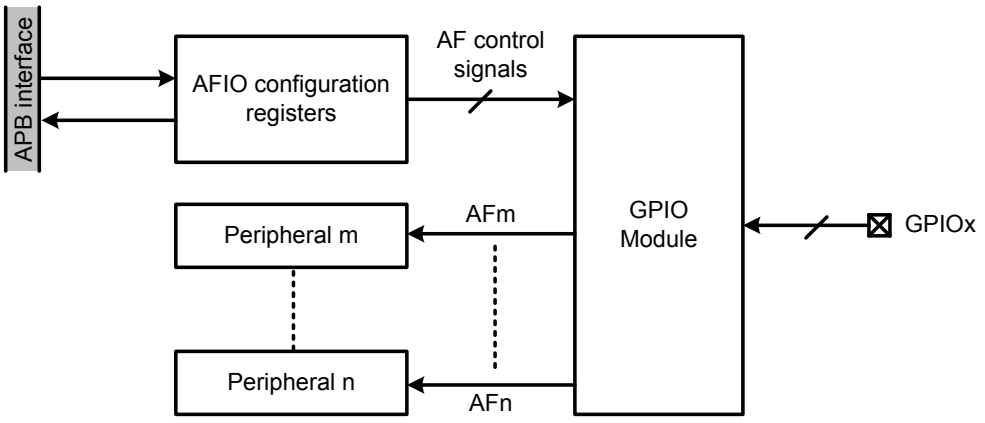
9 Alternative Function I/O (AFIO)

Introduction

In order to expand the flexibility of the GPIO or the usage of peripheral functions, each I/O pin can be configured to have up to four different functions (GPIO or IP functions) by setting the GPxCFGR register (Where x = A or B). According to the usage of the IP resource and application requirements, suitable pinout locations can be selected using the peripheral IO remapping mechanism. Additionally, various GPIO pins can be selected to be the EXTI interrupt line by setting the EXTInPIN [3:0] field in the ESSRn register to trigger an interrupt or event. Please refer to the EXTI section for more details.



Alternate function output through GPIO



Alternate function input through GPIO

Figure 20. AFIO Block Diagram

Features

- APB slave interface for register access
- EXTI source selection
- Configurable pin function for each GPIO, up to four alternative functions on each pin

Functional Descriptions

External Interrupt Pin Selection

The GPIO pins are connected to the 16 EXTI lines as shown in the accompanying figure. For example, the user can set the EXTI0PIN [3:0] field in the ESSR0 register to 00 to select the GPIO PA0 pin as the EXTI line 0 input. Since not all Port A ~ Port B pins are available in all package types, please refer to the pin assignment section for detailed pin information. The setting of the EXTInPIN [3:0] field is invalid when the corresponding pin is not available.

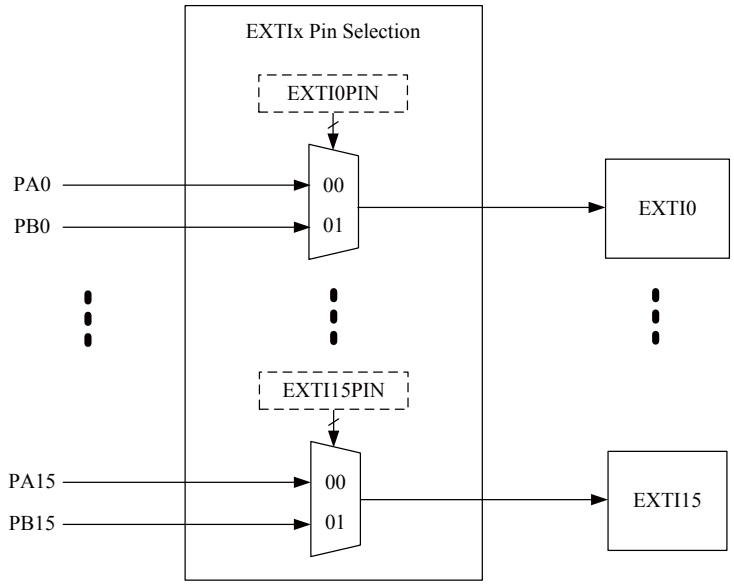


Figure 21. EXTI Channel Input Selection

Alternative Function

Up to four alternative functions can be chosen for each I/O pad by setting the PxCFGn [1:0] field in the GPxCFGR register. Refer to the register description section for the detailed AFIO assignments. The following description shows the setting of the PxCFGn [1:0] field. Note that if the Operational Amplifier/Comparator is active, then pins PB[4:2] or PB[7:5] can not be used as other AFIO functional pins simultaneously.

- PxCFGn [1:0] = 00: Default alternative function (after reset).
- PxCFGn [1:0] = 01: Alternative Function 1
- PxCFGn [1:0] = 10: Alternative Function 2
- PxCFGn [1:0] = 11: Alternative Function 3

Register Map

The following table shows the AFIO register and reset value.

Table 22. Register Map of AFIO

Register	Offset	Description	Reset Value
AFIO Base Address = 0x4002_2000			
ESSR0	0x000	EXTI Source Selection Register 0	0x0000_0000
ESSR1	0x004	EXTI Source Selection Register 1	0x0000_0000
GPACFGR	0x008	GPIO Port A Configuration Register	0x0000_0000
GPBCFGR	0x00C	GPIO Port B Configuration Register	0x0000_0000

Register Descriptions

EXTI Source Selection Register 0 (ESSR0)

This register specifies the selection of EXTI0 ~ EXTI7.

Offset: 0x000

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	EXTI7PIN				EXTI6PIN			
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	23	22	21	20	19	18	17	16
	EXTI5PIN				EXTI4PIN			
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
	EXTI3PIN				EXTI2PIN			
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	EXTI1PIN				EXTI0PIN			
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[31:0]	EXTInPIN[3:0]	EXTIn Pin Selection (n = 0 ~ 7) 0000: PA Bit n is selected as EXTIn source signal 0001: PB Bit n is selected as EXTIn source signal Others: Reserved **NOTE:** Since not all GPIO pins are available in all package types, refer to the pin assignment section for detailed pin information. The EXTInPIN [3:0] field setting is invalid when the corresponding pin is not available.

EXTI Source Selection Register 1 (ESSR1)

This register specifies the selection of EXTI8~EXTI15.

Offset: 0x004

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	EXTI15PIN				EXTI14PIN			
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	23	22	21	20	19	18	17	16
	EXTI13PIN				EXTI12PIN			
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
	EXTI11PIN				EXTI10PIN			
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	EXTI9PIN				EXTI8PIN			
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[31:0]	EXTInPIN[3:0]	EXTIn Pin Selection (n = 8 ~ 15) 0000: PA Bit n is selected as EXTIn signal out 0001: PB Bit n is selected as EXTIn signal out Others: Reserved **NOTE:** Since not all Port GPIO pins are available in all package types, refer to the pin assignment section for detailed pin information. The EXTInPIN [3:0] field setting is invalid when the corresponding pin is not available.

GPIO A Configuration Register (GPACFGR)

This register specifies the GPIO Port A alternative function.

Offset: 0x008

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	PACFG15		PACFG14		PACFG13		PACFG12	
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	PACFG11		PACFG10		PACFG9		PACFG8	
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PACFG7		PACFG6		PACFG5		PACFG4	
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	PACFG3		PACFG2		PACFG1		PACFG0	
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[31:30]	PACFG15	Port A bit 15 AFIO Configuration

PACFG15 [1:0]	Function
00	TRACESWO
01	PA15
10	Reserved
11	GT0_CH0

[29:28] PACFG14 Port A bit 14 AFIO Configuration

PACFG14 [1:0]	Function
00	SWCLK
01	PA14
10	Reserved
11	GT0_CH1

[27:26] PACFG13 Port A bit 13 AFIO Configuration

PACFG13 [1:0]	Function
00	SWDIO
01	PA13
10	Reserved
11	GT0_CH2

Bits	Field	Descriptions
[25:24]	PACFG12	Port A bit 12 AFIO Configuration

PACFG12 [1:0]	Function
00	PA12
01	I²C_SDA
10	Reserved
11	Reserved

[23:22] PACFG11 Port A bit 11 AFIO Configuration

PACFG11 [1:0]	Function
00	PA11
01	I²C_SCL
10	Reserved
11	Reserved

[21:20] PACFG10 Port A bit 10 AFIO Configuration

PACFG10 [1:0]	Function
00	PA10-BOOT1
01	Reserved
10	Reserved
11	Reserved

[19:18] PACFG9 Port A bit 9 AFIO Configuration

PACFG9 [1:0]	Function
00	PA9-BOOT0
01	Reserved
10	UR_TX
11	Reserved

[17:16] PACFG8 Port A bit 8 AFIO Configuration

PACFG8 [1:0]	Function
00	PA8
01	Reserved
10	UR_RX
11	Reserved

[15:14] PACFG7 Port A bit 7 AFIO Configuration

PACFG7 [1:0]	Function
00	PA7
01	ADC_IN7
10	UR_CTS/SCK
11	SPI_SEL

Bits	Field	Descriptions
[13:12]	PACFG6	Port A bit 6 AFIO Configuration

PACFG6 [1:0]	Function
00	PA6
01	ADC_IN6
10	UR_RTS/TXE
11	SPI_SCK

[11:10] PACFG5 Port A bit 5 AFIO Configuration

PACFG5 [1:0]	Function
00	PA5
01	ADC_IN5
10	UR_RI
11	SPI_MISO

[9:8] PACFG4 Port A bit 4 AFIO Configuration

PACFG4 [1:0]	Function
00	PA4
01	ADC_IN4
10	UR_DTR
11	SPI_MOSI

[7:6] PACFG3 Port A bit 3 AFIO Configuration

PACFG3 [1:0]	Function
00	PA3
01	ADC_IN3
10	UR_DSR
11	GT0_CH0

[5:4] PACFG2 Port A bit 2 AFIO Configuration

PACFG2[1:0]	Function
00	PA2
01	ADC_IN2
10	UR_DCD
11	GT0_CH1

[3:2] PACFG1 Port A bit 1 AFIO Configuration

PACFG1[1:0]	Function
00	PA1
01	ADC_IN1
10	Reserved
11	GT0_CH2

Bits	Field	Descriptions
[1:0]	PACFG0	Port A bit 0 AFIO Configuration

PACFG0[1:0]	Function
00	PA0
01	ADC_IN0
10	GT1_ETI
11	GT0_CH3

GPIO B Configuration Register (GPBCFGR)

This register specifies the GPIO Port B alternative function.

Offset: 0x00C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	PBCFG15		PBCFG14		PBCFG13		PBCFG12	
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	23	22	21	20	19	18	17	16
	PBCFG11		PBCFG10		PBCFG9		PBCFG8	
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
	PBCFG7		PBCFG6		PBCFG5		PBCFG4	
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	PBCFG3		PBCFG2		PBCFG1		PBCFG0	
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[31:30]	PBCFG15	Port B bit 15 AFIO Configuration

PBCFG15[1:0]	Function
00	PB15
01	SPI_MOSI
10	UR_RI
11	GT1_CH0

[29:28] PBCFG14 Port B bit 14 AFIO Configuration

PBCFG14[1:0]	Function
00	PB14
01	SPI_MISO
10	UR_DTR
11	GT1_CH1

[27:26] PBCFG13 Port B bit 13 AFIO Configuration

PBCFG13[1:0]	Function
00	PB13
01	SPI_SCK
10	UR_DSR
11	GT1_CH2

Bits	Field	Descriptions
[25:24]	PBCFG12	Port B bit 12 AFIO Configuration

PBCFG12[1:0]	Function
00	PB12
01	SPI_SEL
10	UR_DCD
11	GT1_CH3

[23:22] PBCFG11 Port B bit 11 AFIO Configuration

PBCFG11[1:0]	Function
00	PB11
01	CKOUT
10	Reserved
11	GT0_CH3

[21:20] PBCFG10 Port B bit 10 AFIO Configuration

PBCFG10[1:0]	Function
00	RTCOUT
01	PB10-WAKEUP
10	Reserved
11	GT0_ETI

[19:18] PBCFG9 Port B bit 9 AFIO Configuration

PBCFG9[1:0]	Function
00	XTAL32KOUT
01	PB9
10	Reserved
11	Reserved

If this pin is used as an oscillator pin, this field should not be changed.

[17:16] PBCFG8 Port B bit 8 AFIO Configuration

PBCFG8 [1:0]	Function
00	XTAL32KIN
01	PB8
10	Reserved
11	Reserved

If this pin is used as an oscillator pin, this field should not be changed.

Bits	Field	Descriptions
[15:14]	PBCFG7	Port B bit 7 AFIO Configuration

PBCFG7[1:0]	Function
00	PB7
01	AOUT1
10	UR_CTS/SCK
11	GT0_ETI

[13:12] PBCFG6 Port B bit 6 AFIO Configuration

PBCFG6[1:0]	Function
00	PB6
01	CP1
10	Reserved
11	GT1_ETI

[11:10] PBCFG5 Port B bit 5 AFIO Configuration

PBCFG5[1:0]	Function
00	PB5
01	CN1
10	Reserved
11	GT1_CH3

[9:8] PBCFG4 Port B bit 4 AFIO Configuration

PBCFG4[1:0]	Function
00	PB4
01	AOUT0
10	UR_RTS/TXE
11	GT1_CH2

[7:6] PBCFG3 Port B bit 3 AFIO Configuration

PBCFG3[1:0]	Function
00	PB3
01	CP0
10	Reserved
11	GT1_CH1

[5:4] PBCFG2 Port B bit 2 AFIO Configuration

PBCFG2[1:0]	Function
00	PB2
01	CN0
10	Reserved
11	GT1_CH0

Bits	Field	Descriptions
[3:2]	PBCFG1	Port B bit 1 AFIO Configuration

PBCFG1[1:0]	Function
00	XTALOUT
01	PB1
10	Reserved
11	Reserved

If this pin is used as an oscillator pin, this field should not be changed.

Bits	Field	Descriptions
[1:0]	PBCFG0	Port B bit 0 AFIO Configuration

PACFG0[1:0]	Function
00	XTALIN
01	PB0
10	Reserved
11	Reserved

If this pin is used as an oscillator pin, this field should not be changed.

10 Nested Vectored Interrupt Controller (NVIC)

Introduction

In order to reduce the latency and increase the interrupt processing efficiency, a tightly coupled integrated section, which is named as Nested Vectored Interrupt Controller (NVIC), is provided by the Cortex™-M3. The NVIC controls the system exceptions and the peripheral interrupts which include functions such as the enable/disable control, priority, clear-pending, active status report, software trigger and vector table remapping. Refer to the Technical Reference Manual of Cortex™-M3 for more details.

Additionally, an integrated simple, 24-bit down count timer (SysTick) is provided by the Cortex™-M3 to be used as a tick timer for the Real Timer Operation System (RTOS) or as a simple counter. The SysTick counts down from the preloaded value and generates a system interrupt when it reached zero.

The accompanying table lists the 16 system exception types and the 31 peripheral interrupts.

Table 23. Exception Types

Exception type	Priority	Interrupt Number	Exception Number	Vector Address	Description
	—	—	0	0x000	Initial Stack Point value
Reset	-3 (Highest)	—	1	0x004	Reset
NMI	-2	—	2	0x008	Non-Maskable Interrupt. The clock stuck interrupt signal (clock monitor function provided by the Clock Control Unit) is connected to the NMI input
Hard Fault	-1	—	3	0x00C	All fault classes
Memory Management	Configurable(1)	—	4	0x010	Memory Protection Unit (MPU) mismatch, including access violation and no match
Bus Fault	Configurable(1)	—	5	0x014	Pre-fetch fault, memory access fault and other address/memory related fault.
Usage Fault	Configurable(1)	—	6	0x018	Usage fault, such as undefined executed instruction or illegal state transition attempt
—	—	—	7	0x01C	Reserved
—	—	—	8	0x020	Reserved
—	—	—	9	0x024	Reserved
—	—	—	10	0x028	Reserved
SVCall	Configurable(1)	—	11	0x02C	SVC instruction System Service Call
Debug Monitor	Configurable(1)	—	12	0x030	Debug monitor, when not halted
—	Configurable(1)	—	13	0x034	Reserved
PendSV	Configurable(1)	—	14	0x038	System Service Pendable Request
SySTick	Configurable(1)	—	15	0x03C	SysTick timer decremented to zero

Exception type	Priority	Interrupt Number	Exception Number	Vector Address	Description
CKRDY	Configurable(2)	0	16	0x040	Clock ready interrupt (HSE, HSI, LSE, LSI, or PLL)
LVD	Configurable(2)	1	17	0x044	Low voltage detection interrupt
BOD	Configurable(2)	2	18	0x048	Brown-Out detection interrupt
WDT	Configurable(2)	3	19	0x04C	Watchdog timer global interrupt
RTC	Configurable(2)	4	20	0x050	RTC global interrupt
FMC	Configurable(2)	5	21	0x054	FMC global interrupt
EVWUP	Configurable(2)	6	22	0x058	EXTI Event wakeup interrupt
LPWUP	Configurable(2)	7	23	0x05C	WAKEUP pin interrupt
EXTI0	Configurable(2)	8	24	0x060	EXTI Line 0 interrupt
EXTI1	Configurable(2)	9	25	0x064	EXTI Line 1 interrupt
EXTI2	Configurable(2)	10	26	0x068	EXTI Line 2 interrupt
EXTI3	Configurable(2)	11	27	0x06C	EXTI Line 3 interrupt
EXTI4	Configurable(2)	12	28	0x070	EXTI Line 4 interrupt
EXTI5	Configurable(2)	13	29	0x074	EXTI Line 5 interrupt
EXTI6	Configurable(2)	14	30	0x078	EXTI Line 6 interrupt
EXTI7	Configurable(2)	15	31	0x07C	EXTI Line 7 interrupt
EXTI8	Configurable(2)	16	32	0x080	EXTI Line 8 interrupt
EXTI9	Configurable(2)	17	33	0x084	EXTI Line 9 interrupt
EXTI10	Configurable(2)	18	34	0x088	EXTI Line 10 interrupt
EXTI11	Configurable(2)	19	35	0x08C	EXTI Line 11 interrupt
EXTI12	Configurable(2)	20	36	0x090	EXTI Line 12 interrupt
EXTI13	Configurable(2)	21	37	0x094	EXTI Line 13 interrupt
EXTI14	Configurable(2)	22	38	0x098	EXTI Line 14 interrupt
EXTI15	Configurable(2)	23	39	0x09C	EXTI Line 15 interrupt
COMP	Configurable(2)	24	40	0x0A0	Comparator global interrupt
ADC	Configurable(2)	25	41	0x0A4	ADC interrupt
—	—	26	42	0x0A8	Reserved
—	—	27	43	0x0AC	Reserved
—	—	28	44	0x0B0	Reserved
—	—	29	45	0x0B4	Reserved
—	—	30	46	0x0B8	Reserved
—	—	31	47	0x0BC	Reserved
—	—	32	48	0x0C0	Reserved
—	—	33	49	0x0C4	Reserved
—	—	34	50	0x0C8	Reserved
GPTM0	Configurable(2)	35	51	0x0CC	GPTM0 global interrupt
GPTM1	Configurable(2)	36	52	0x0D0	GPTM1 global interrupt
—	—	37	53	0x0D4	Reserved
—	—	38	54	0x0D8	Reserved

Exception type	Priority	Interrupt Number	Exception Number	Vector Address	Description
—	—	39	55	0x0DC	Reserved
—	—	40	56	0x0E0	Reserved
—	—	41	57	0x0E4	Reserved
—	—	42	58	0x0E8	Reserved
I^2C	Configurable(2)	43	59	0x0EC	I^2C global interrupt
—	—	44	60	0x0F0	Reserved
SPI	Configurable(2)	45	61	0x0F4	SPI global interrupt
—	—	46	62	0x0F8	Reserved
USART	Configurable(2)	47	63	0x0FC	USART global interrupt

NOTES: 1. The exception priority can be changed using the NVIC System Handler Priority Registers. For more information, refer to the ARM “Technical Reference Manual of Cortex™-M3” document.

2. The interrupt priority can be changed using the NVIC Interrupt Priority Registers. For more information, refer to the ARM “Technical Reference Manual of Cortex™-M3” document.

Features

- 16 system Cortex™-M3 exceptions
- Up to 31 maskable peripheral interrupts
- 16 programmable priority levels - 4 bit interrupt priority setup
- Non-Maskable interrupt
- Low-latency exception and interrupt handling
- Vector table remapping capability
  - Integrated simple, 24-bit system timer, SysTick
  - 24-bit down counter
  - Auto-reloading capability
  - Maskable system interrupt generation when counter decrements to 0
  - SysTick clock source derived from the HCLK or AHB clock divided by 8

Functional Descriptions

SysTick Calibration

The SysTick Calibration Value Register (SCALIB) is provided by the NVIC to give a reference time base of 1ms for the RTOS tick timer or other purpose. The TENMS field in the SCALIB register has a fixed value of 9000 which is the counter reload value to indicate 1 ms when the clock source comes from the SysTick reference input clock STCLK with a frequency of 9 MHz (72 MHz divide by 8).

Register Map

The following table shows the NVIC registers and reset values.

Table 24. Register Map of NVIC

Register	Offset	Description	Reset Value
NVIC Base Address = 0xE000_E000			
ICTR	0x004	Interrupt Control Type Register	0x0000_0001
SCTRL	0x010	SysTick Control and Status Register	0x0000_0000
SLOAD	0x014	SysTick Reload Value Register	Unpredictable
SVAL	0x018	SysTick Current Value Register	Unpredictable
SCALIB	0x01C	SysTick Calibration Value Register	0x4000_2328
ISER0_31	0x100	Irq 0 to 31 Set Enable Register	0x0000_0000
ISER32_63	0x104	Irq 32 to 63 Set Enable Register	0x0000_0000
ICER0_31	0x180	Irq 0 to 31 Clear Enable Register	0x0000_0000
ICER32_63	0x184	Irq 32 to 63 Clear Enable Register	0x0000_0000
ISPR0_31	0x200	Irq 0 to 31 Set Pending Register	0x0000_0000
ISPR32_63	0x204	Irq 32 to 63 Set Pending Register	0x0000_0000
ICPR0_31	0x280	Irq 0 to 31 Clear Pending Register	0x0000_0000
ICPR32_63	0x284	Irq 32 to 63 Clear Pending Register	0x0000_0000
IABR0_31	0x300	Irq 0 to 31 Active Bit Register	0x0000_0000
IABR32_63	0x304	Irq 32 to 63 Active Bit Register	0x0000_0000
IRQ0_3	0x400	Irq 0 to 3 Priority Register	0x0000_0000
IRQ4_7	0x404	Irq 4 to 7 Priority Register	0x0000_0000

Register	Offset	Description	Reset Value
IRQ8_11	0x408	Irq 8 to 11 Priority Register	0x0000_0000
IRQ12_15	0x40C	Irq 12 to 15 Priority Register	0x0000_0000
IRQ16_19	0x410	Irq 16 to 19 Priority Register	0x0000_0000
IRQ20_23	0x414	Irq 20 to 23 Priority Register	0x0000_0000
IRQ24_27	0x418	Irq 24 to 27 Priority Register	0x0000_0000
IRQ28_31	0x41C	Irq 28 to 31 Priority Register	0x0000_0000
IRQ32_35	0x420	Irq 32 to 35 Priority Register	0x0000_0000
IRQ36_39	0x424	Irq 36 to 39 Priority Register	0x0000_0000
IRQ40_43	0x428	Irq 40 to 43 Priority Register	0x0000_0000
IRQ44_47	0x42C	Irq 44 to 47 Priority Register	0x0000_0000
ICSR	0xD04	Interrupt Control State Register	0x0000_0000
VTOR	0xD08	Vector Table Offset Register	0x0000_0000
AIRCR	0xD0C	Application Interrupt/Reset Control Register	0xFA05_0000
SCR	0xD10	System Control Register	0x0000_0000
CCR	0xD14	Configuration Control Register	0x0000_0000
SHPR4_7	0xD18	System Handlers 4-7 Priority Register	0x0000_0000
SHPR8_11	0xD1C	System Handlers 8-11 Priority Register	0x0000_0000
SHPR12_15	0xD20	System Handlers 12-15 Priority Register	0x0000_0000
SHCSR	0xD24	System Handler Control and State Register	0x0000_0000
CFSR	0xD28	Configurable Fault Status Registers	0x0000_0000
HFSR	0xD2C	Hard Fault Status Register	0x0000_0000
DFSR	0xD30	Debug Fault Status Register	0x0000_0000
MMFAR	0xD34	Mem Manage Address Register	Unpredictable
BFAR	0xD38	Bus Fault Address Register	Unpredictable
STIR	0xF00	Software Trigger Interrupt Register	0x0000_0000

NOTE: For more information of the above detail register descriptions, please refer to the “Technical Reference Manual of Cortex™-M3” document from ARM.

11 External Interrupt / Event Controller (EXTI)

Introduction

The External Interrupt / Event Controller (EXTI) comprises 16 edge detectors which can generate a wakeup event or interrupt requests independently. The external interrupts have five trigger types, low level, high level, negative edge, positive edge, and both edges, selectable using the SRCnTYPE field in the EXTICFGRn register. In the wakeup event mode, the wakeup event polarity can be configured by setting the EXTInPOL field in the EXTIWAKUPPOLR register. If the EVWUPIEN bit in the EXTIWAKUPCR Register is set, the EVWUP interrupt can be generated when the associated wakeup event occurs and the corresponding EXTI wakeup enable bit is set. Each EXTI line can also be masked independently.

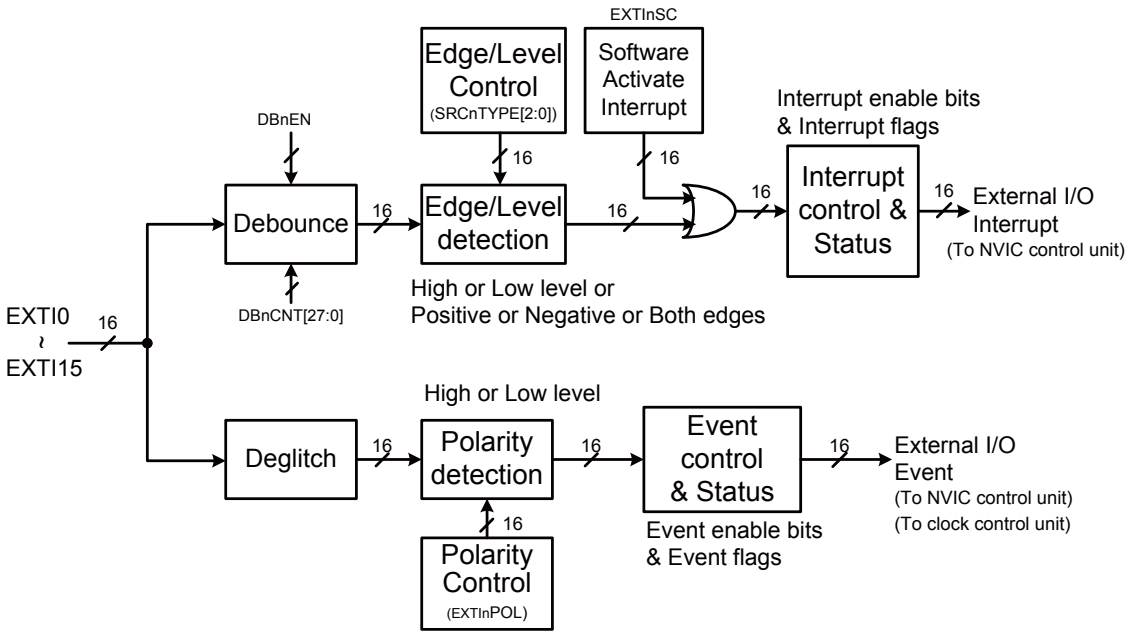


Figure 22. EXTI Block Diagram

Features

- Up to 16 EXTI lines with configurable trigger sources and type
  - All GPIO pins can be selected as an EXTI trigger source
  - Source trigger type includes high level, low level, negative edge, positive edge or both edges
- Individual interrupt enable, wakeup enable and status bits for each EXTI line
- Software interrupt trigger mode for each EXTI line
- Integrated deglitch filter for short pulse blocking

Functional Descriptions

Wakeup Event Management

In order to wakeup the system from the power saving mode, the EXTI controller provides a function which can monitor external events and send them to the Cortex™-M3 core and the Clock Control Unit (CKCU). These External events include EXTI events, Low Voltage Detection, WAKEUP input pin and RTC wakeup functions. By configuring the wakeup event enable bit in the corresponding peripheral, the wakeup signal will be sent to the Cortex™-M3 and the CKCU via the EXTI controller when the corresponding wakeup event occurs. Additionally, the software can enable the event wakeup interrupt function by setting the EVWUPIEN bit in the EXTIWAKUPCR register and the EXTI controller will then assert an interrupt when the wakeup event occurs.

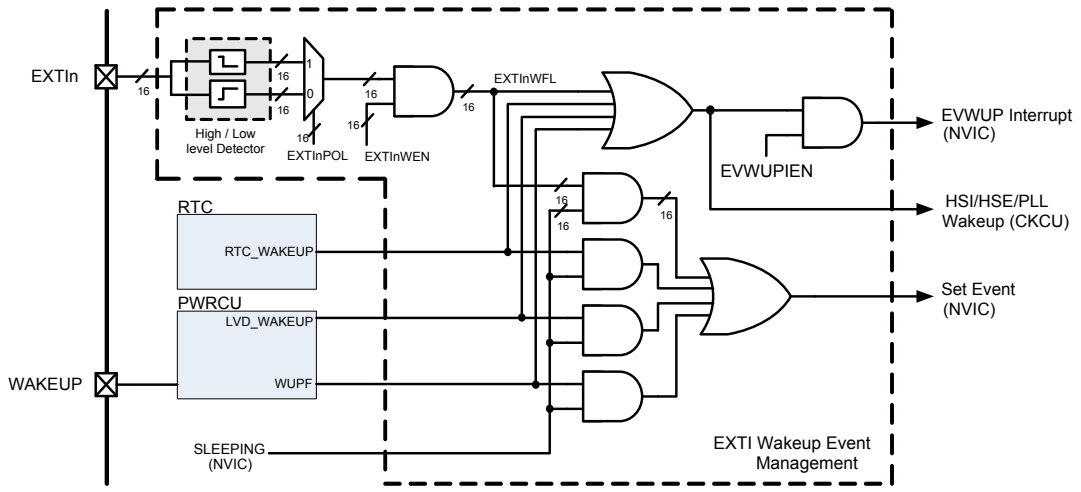


Figure 23. EXTI Wakeup Event Management

External Interrupt / Event Line Mapping

All GPIO pins can be selected as EXTI trigger sources by configuring the EXTInPIN [3:0] field in the AFIO ESSRn register to trigger an interrupt or event. Refer to the AFIO section for more details.

Interrupt and Debounce

The application software can set the DBnEN bit in the EXTIn Interrupt Configuration Register EXTICFGRn to enable the corresponding pin de-bounce function and configure the DBnCNT field in the EXTICFGRn so as to select an appropriate de-bounce time for specific applications. The interrupt signal will however be delayed due to the de-bounce function. When the device is woken up from the power saving mode by an external interrupt, an interrupt request will be generated by the EXTI wakeup flag. After the device has been woken up and the clock has recovered, the EXTI wake-up flag that was triggered by the EXTI line must be read and then cleared by application software. The accompanying diagram shows the relationship between the EXTI input signal and the EXTI interrupt / event request signal.

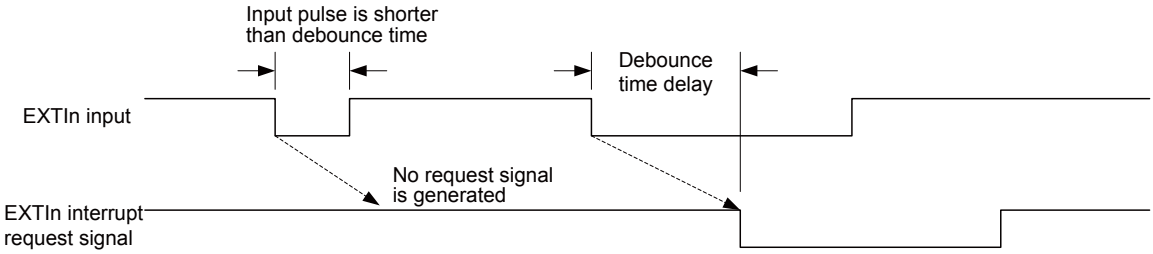


Figure 24. EXTI Debounce Function

Register Map

The following table shows the EXTI registers and reset values.

Table 25. Register Map of EXTI

Register	Offset	Description	Reset Value
EXTI Base Address = 0x4002_4000			
EXTICFGR0	0x000	EXTI Interrupt 0 Configuration Register	0x0000_0000
EXTICFGR1	0x004	EXTI Interrupt 1 Configuration Register	0x0000_0000
EXTICFGR2	0x008	EXTI Interrupt 2 Configuration Register	0x0000_0000
EXTICFGR3	0x00C	EXTI Interrupt 3 Configuration Register	0x0000_0000
EXTICFGR4	0x010	EXTI Interrupt 4 Configuration Register	0x0000_0000
EXTICFGR5	0x014	EXTI Interrupt 5 Configuration Register	0x0000_0000
EXTICFGR6	0x018	EXTI Interrupt 6 Configuration Register	0x0000_0000
EXTICFGR7	0x01C	EXTI Interrupt 7 Configuration Register	0x0000_0000
EXTICFGR8	0x020	EXTI Interrupt 8 Configuration Register	0x0000_0000
EXTICFGR9	0x024	EXTI Interrupt 9 Configuration Register	0x0000_0000
EXTICFGR10	0x028	EXTI Interrupt 10 Configuration Register	0x0000_0000
EXTICFGR11	0x02C	EXTI Interrupt 11 Configuration Register	0x0000_0000
EXTICFGR12	0x030	EXTI Interrupt 12 Configuration Register	0x0000_0000
EXTICFGR13	0x034	EXTI Interrupt 13 Configuration Register	0x0000_0000
EXTICFGR14	0x038	EXTI Interrupt 14 Configuration Register	0x0000_0000
EXTICFGR15	0x03C	EXTI Interrupt 15 Configuration Register	0x0000_0000
EXTICR	0x040	EXTI Interrupt Control Register	0x0000_0000
EXTIEDGEFLGR	0x044	EXTI Interrupt Edge Flag Register	0x0000_0000
EXTIEDGESR	0x048	EXTI Interrupt Edge Status Register	0x0000_0000
EXTISSCR	0x04C	EXTI Interrupt Software Set Command Register	0x0000_0000
EXTIWAKUPCR	0x050	EXTI Interrupt Wakeup Control Register	0x0000_0000
EXTIWAKUPPOLR	0x054	EXTI Interrupt Wakeup Polarity Register	0x0000_0000
EXTIWAKUPFLG	0x058	EXTI Interrupt Wakeup Flag Register	0x0000_0000

Register Descriptions

EXTI Interrupt Configuration Register n (EXTICFGRn, n = 0 ~ 15)

This register is used to specify the debounce function and select the trigger type.

Offset: 0x000 (EXTICFGR0) ~ 0x03C (EXTICFGR15)

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	DBnEN	SRCnTYPE			DBnCNT			
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	23	22	21	20	19	18	17	16
	DBnCNT							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
	DBnCNT							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	DBnCNT							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[31]	DBnEN	EXTIn De-bounce Circuit Enable Bit (n = 0 ~ 15) 0: De-bounce circuit disabled 1: De-bounce circuit enabled
[30:28]	SRCnTYPE	EXTIn Interrupt Source Trigger Type (n = 0 ~ 15)

SRCnTYPE [2:0]			Interrupt Source Type
0	0	0	Low-level Sensitive
0	0	1	High-level Sensitive
0	1	0	Negative-edge Triggered
0	1	1	Positive-edge Triggered
1	X	X	Both-edge Triggered

[27:0]	DBnCNT	EXTIn De-bounce Counter (n = 0 ~ 15) The de-bounce time is calculated with DBnCNT x APB clock period and should be long enough to take effect on the input signal.

EXTI Interrupt Control Register (EXTICR)

This register is used to control the EXTI interrupt.

Offset: 0x040

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	EXTI15EN	EXTI14EN	EXTI13EN	EXTI12EN	EXTI11EN	EXTI10EN	EXTI9EN	EXTI8EN
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	EXTI7EN	EXTI6EN	EXTI5EN	EXTI4EN	EXTI3EN	EXTI2EN	EXTI1EN	EXTI0EN
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	EXTInEN	EXTIn Interrupt Enable Bit (n = 0 ~ 15) 0: EXTI line n interrupt disabled 1: EXTI line n interrupt enabled

EXTI Interrupt Edge Flag Register (EXTIEDGEFLGR)

This register is used to indicate if an EXTI edge has been detected.

Offset: 0x044

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	Reserved							
Type/Reset								
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	EXTI15EDF	EXTI14EDF	EXTI13EDF	EXTI12EDF	EXTI11EDF	EXTI10EDF	EXTI9EDF	EXTI8EDF
Type/Reset	WC 0	WC 0	WC 0	WC 0	WC 0	WC 0	WC 0	WC 0
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	EXTI7EDF	EXTI6EDF	EXTI5EDF	EXTI4EDF	EXTI3EDF	EXTI2EDF	EXTI1EDF	EXTI0EDF
Type/Reset	WC 0	WC 0	WC 0	WC 0	WC 0	WC 0	WC 0	WC 0

Bits	Field	Descriptions
[15:0]	EXTInEDF	EXTIn Edge Detection Flag (n = 0 ~ 15) 0: No edge is detected 1: Positive or negative edge is detected This bit is set by hardware when a positive or negative edge is detected on the corresponding EXTI line. Software should write 1 to clear it.

EXTI Interrupt Edge Status Register (EXTIEDGESR)

This register indicates the polarity of a detected EXTI edge.

Offset: 0x048

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	Reserved							
Type/Reset								
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	EXTI15EDS	EXTI14EDS	EXTI13EDS	EXTI12EDS	EXTI11EDS	EXTI10EDS	EXTI9EDS	EXTI8EDS
Type/Reset	WC 0	WC 0	WC 0	WC 0	WC 0	WC 0	WC 0	WC 0
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	EXTI7EDS	EXTI6EDS	EXTI5EDS	EXTI4EDS	EXTI3EDS	EXTI2EDS	EXTI1EDS	EXTI0EDS
Type/Reset	WC 0	WC 0	WC 0	WC 0	WC 0	WC 0	WC 0	WC 0

Bits	Field	Descriptions
[15:0]	EXTInEDS	EXTIn Edge Detection Status (n = 0 ~ 15) 0: Negative edge detected 1: Positive edge detected Software should write 1 to clear it.

EXTI Interrupt Software Set Command Register (EXTISSCR)

This register is used to activate the EXTI interrupt.

Offset: 0x04C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	EXTI15SC	EXTI14SC	EXTI13SC	EXTI12SC	EXTI11SC	EXTI10SC	EXTI9SC	EXTI8SC
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	EXTI7SC	EXTI6SC	EXTI5SC	EXTI4SC	EXTI3SC	EXTI2SC	EXTI1SC	EXTI0SC
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	EXTInSC	EXTIn Software Set Command (n = 0 ~ 15) 0: Deactivates the EXTIn interrupt 1: Activates the EXTIn interrupt

EXTI Interrupt Wakeup Control Register (EXTIWAKUPCR)

This register is used to control the EXTI interrupt and wakeup function.

Offset: 0x050

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	EVWUPIEN	Reserved						
Type/Reset	RW 0							
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	EXTI15WEN	EXTI14WEN	EXTI13WEN	EXTI12WEN	EXTI11WEN	EXTI10WEN	EXTI9WEN	EXTI8WEN
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	EXTI7WEN	EXTI6WEN	EXTI5WEN	EXTI4WEN	EXTI3WEN	EXTI2WEN	EXTI1WEN	EXTI0WEN
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[31]	EVWUPIEN	EXTI Event Wakeup Interrupt Enable Bit 0: EVWUP interrupt is disabled 1: EVWUP interrupt is enabled
[15:0]	EXTInWEN	EXTIn Wakeup Enable Bit (n = 0 ~ 15) 0: EXTIn wakeup is disabled 1: EXTIn wakeup is enabled

EXTI Interrupt Wakeup Polarity Register (EXTIWAKUPPOLR)

This register is used to select the EXTI line interrupt wakeup polarity.

Offset: 0x054

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	Reserved							
Type/Reset								
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	EXTI15POL	EXTI14POL	EXTI13POL	EXTI12POL	EXTI11POL	EXTI10POL	EXTI9POL	EXTI8POL
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	EXTI7POL	EXTI6POL	EXTI5POL	EXTI4POL	EXTI3POL	EXTI2POL	EXTI1POL	EXTI0POL
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	EXTInPOL	EXTIn Wakeup Polarity (n = 0 ~ 15) 0: EXTIn wakeup is high level active 1: EXTIn wakeup is low level active

EXTI Interrupt Wakeup Flag Register (EXTIWAKUPFLG)

This register indicates if the system has been woken up by the EXTI line

Offset: 0x058

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	Reserved							
Type/Reset								
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	EXTI15WFL	EXTI14WFL	EXTI13WFL	EXTI12WFL	EXTI11WFL	EXTI10WFL	EXTI9WFL	EXIT8WFL
Type/Reset	WC 0	WC 0	WC 0	WC 0	WC 0	WC 0	WC 0	WC 0
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	EXTI7WFL	EXTI6WFL	EXTI5WFL	EXTI4WFL	EXTI3WFL	EXTI2WFL	EXTI1WFL	EXTI0WFL
Type/Reset	WC 0	WC 0	WC 0	WC 0	WC 0	WC 0	WC 0	WC 0

Bits	Field	Descriptions
[15:0]	EXTInWFL	EXTIn Wakeup Flag (n = 0 ~ 15) 0: No wakeup occurs 1: System is woken up by EXTIn Software should write 1 to clear it.

12 Analog to Digital Converter (ADC)

Introduction

A 12-bit multi-channel Analog to Digital Converter is integrated in the device. There are a total of 10 multiplexed channels including 8 external channels on which the external analog signals can be measured, and 2 internal channels. If the input voltage is required to remain within a specific threshold window, the Analog Watchdog function will monitor and detect the signal. An interrupt will then be generated to inform that the input voltage is higher or lower than the set thresholds. There are three conversion modes to convert an analog signal to digital data. The A/D converter can be operated in one shot, continuous and discontinuous conversion modes. A right-aligned 16-bit data register is provided to store the data after conversion.

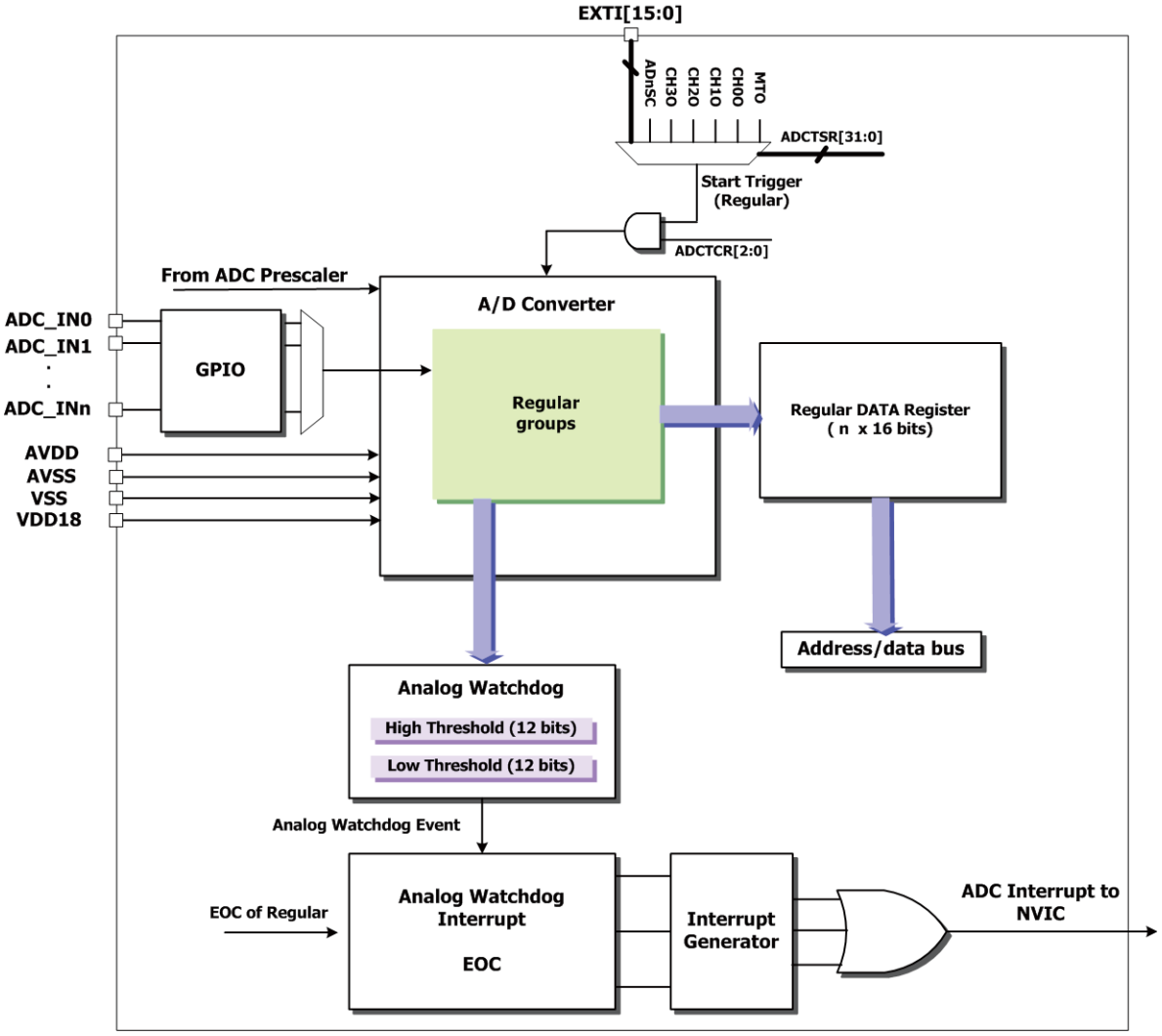


Figure 25. ADC Block Diagram

Features

- 12-bit SAR ADC engine
- Up to 1 MSPS conversion rate
  - 1 μs at 56 MHz, 1.17 μs at 72 MHz
- 8 external analog input channels
- 2 internal reference voltage detect analog input channels - V_{SSA} and V_{DDA}
- Individual programmable sampling time for each channel
- Three conversion modes
  - One shot conversion mode
  - Continuous conversion mode
  - Discontinuous conversion mode.
- Up to 8 dedicated sequencers and data registers for conversion
- Data format : unsigned right-aligned format
- Analog watchdog for predefined voltage range monitor
  - Lower/Upper threshold registers
  - Interrupt generation
- Various trigger start sources for conversion modes
  - Software trigger
  - EXTI - external interrupt input pin
  - GPTM trigger output - MTO and PWM CHnO
- Multiple generated interrupts
  - Single conversion end
  - Subgroup conversion end
  - Cycle conversion end
  - Analog Watchdog
  - Data register overwrite

Functional Descriptions

ADC Clock Setup

The ADC clock (CK_ADC) is provided by the Clock Controller which is synchronous with the APB clock known as PCLK. Refer to the Clock Control Unit chapter for more details.

Channel Selection

The A/D converter supports 8 multiplexed channels and organizes the conversion results into the regular group. A regular group can organize a conversion sequence which can be implemented on the channels arranged in a specific conversion sequence length from 1 to 8. For example, conversions can be carried out with the following channel sequence: CH2, CH4, CH7, CH5, CH6, CH3, CH1 and CH0 one after another.

A regular group is composed of up to 8 conversions. The selected channels of the regular group conversion can be specified in the ADCLST0~ADCLST1 registers. The total conversion sequence length is setup using the ADSEQL[2:0] bits in the ADCCONV register.

Modifying the ADCCONV registers during a conversion process will reset the current conversion, after which a new start pulse is required to restart a new conversion.

Conversion Modes

The A/D has three operating conversion modes. The conversion modes are, One Shot Conversion Mode, Continuous Conversion Mode and Discontinuous Conversion Mode. Details are provided later.

One Shot Conversion Mode

In the one shot conversion mode, the A/D Converter will perform conversion cycles on the channels specified in the A/D conversion list registers ADCLSTn with a specific sequence when an A/D start trigger event occurs. When the A/D conversion mode field ADMODE [1:0] is set to 0x0, the A/D converter will operate in the One Shot Conversion Mode. This mode can be started by a software trigger, an external EXTI event or a GPTM functional determined by the Trigger Control Registers ADCTCR and the Trigger Source Registers ADCTSR.

Regular Conversion

- The converted data will be stored in the 16-bit ADCDRn (n = 0~7) registers.
- The ADIRAWS (ADC regular single sample end of conversion event raw status) flag in the ADCIRAW register will be set when the single sample conversion is finished.
- An interrupt will be generated after a single sample end of conversion if the ADIMS bit in the ADCIMR register is not masked.
- An interrupt will be generated after a regular group cycle end of conversion if the ADIMC bit in the ADCIMR register is not masked.

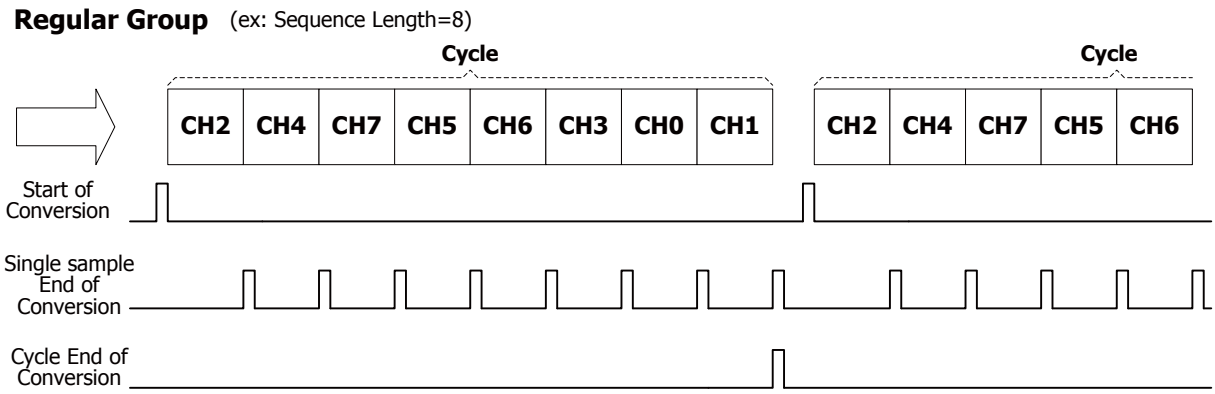


Figure 26. One Shot Conversion Mode

Continuous Conversion Mode

In the Continuous Conversion Mode, repeat conversion cycles will restart automatically without requiring additional A/D start trigger signals after a channel group conversion has completed. When the A/D conversion mode field ADMODE [1:0] is set to 0x2, the A/D converter will operate in the Continuous Conversion Mode which can be started by a software trigger, an external EXTI event or a GPTM functional determined by the Trigger Control Registers ADCTCR and the Trigger Source Registers ADCTSR.

After each conversion:

- The converted data will be stored in the 16-bit ADCDRn (n = 0~7) registers.
- The ADIRAWC (ADC regular group cycle end of conversion event raw status) flag in the ADCIRAW register will be set when the conversion cycle is finished.
- An interrupt will be generated after a single sample end of conversion if the ADIMS bit in the ADCIMR register is not masked.
- An interrupt will be generated after a regular group cycle end of conversion if the ADIMC bit in the ADCIMR register is not masked.

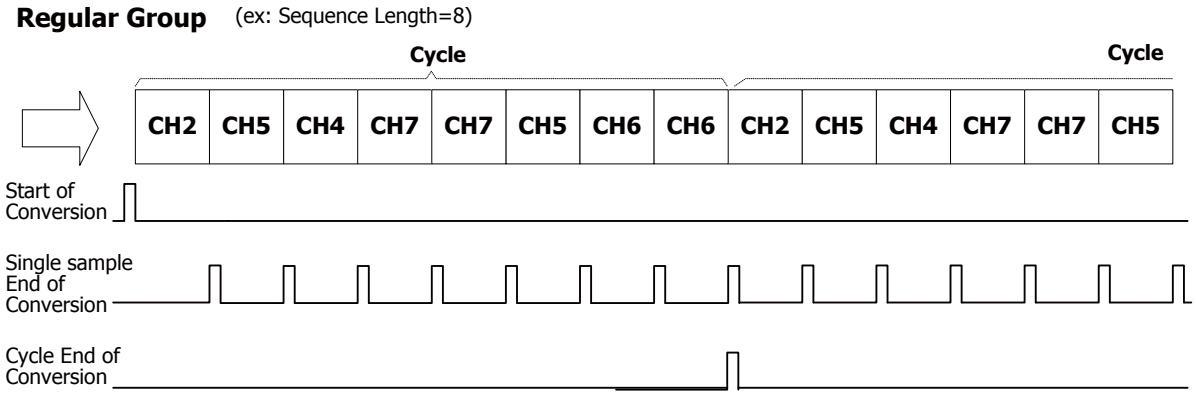


Figure 27. Continuous Conversion Mode

Discontinuous Conversion Mode

Regular group

The A/D converter will operate in the Discontinuous Conversion Mode for regular groups when the A/D conversion mode bit field ADMODE [1:0] in the ADCCONV register is set to 0x3. The regular group to be converted can have up to 8 channels and can be arranged in a specific sequence by configuring the ADCLSTn registers where n ranges from 0 to 1. This mode is provided to convert data for the regular group with a short sequence, named as the A/D regular conversion subgroup, each time a trigger event occurs. The subgroup length is defined in the ADSUBL [2:0] field to specify the subgroup length. In the Discontinuous Conversion Mode the A/D converter can be started by a software trigger, an external EXTI event or a GPTM functional event for regular groups determined by the Trigger Control Register ADCTCR and the Trigger Source Register ADCTSR.

In the Discontinuous Conversion Mode, the A/D Converter will start to convert the next n conversions where the number n is the subgroup length defined by the ADSUBL field. When a trigger event occurs, the channels to be converted with a specific sequence are specified in the ADCLSTn registers. After n conversions have completed, the regular subgroup EOC interrupt raw flag ADIRAWG in the ADCIRAW register will be asserted. The A/D converter will now not continue to perform the next n conversions until the next trigger event occurs. The conversion cycle will end after all the regular group channels, of which the total number is defined by the ADSEQL[2:0] bits in the ADCCONV register, have finished their conversion, at which point the regular cycle EOC interrupt raw flag ADIRAWC in the ADCIRAW register will be asserted. If a new trigger event occurs after all the subgroup channels have all been converted, i.e., a complete conversion cycle has been finished, the conversion will restart from the first subgroup.

Example:

- A/D subgroup length = 3 (ADSUBL=2) and sequence length = 8 (ADSEQL=7), channels to be converted = 2, 4, 7, 5, 6, 3, 0 and 1 - specific converting sequence as defined in the ADCLSTn registers,
  - Trigger 1: subgroup channels to be converted are CH2, CH4 and CH7 with the ADIRAWG flag being asserted after subgroup EOC.
  - Trigger 2: subgroup channels to be converted are CH5, CH6 and CH3 with the ADIRAWG flag being asserted after subgroup EOC.
  - Trigger 3: subgroup channels to be converted are CH0 and CH1 with the ADIRAWG flag being asserted after subgroup EOC. Also a Cycle end of conversion (EOC) interrupt raw flag ADIRAWC will be asserted.
  - Trigger 4: subgroup channels to be converted are CH2, CH4 and CH7 with the ADIRAWG flag being asserted - conversion sequence restarts from the beginning.

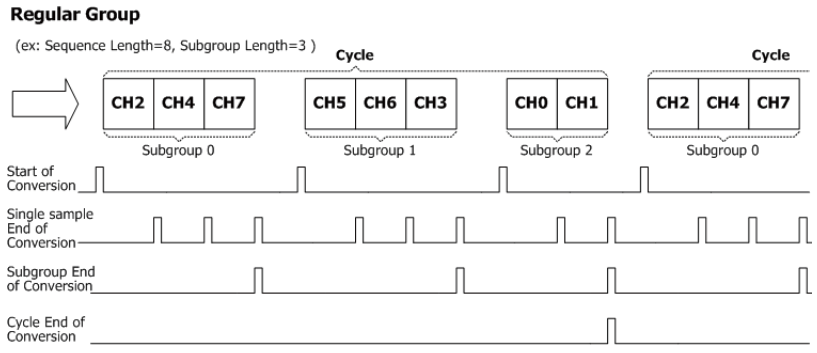


Figure 28. Regular Group Discontinuous Conversion Mode

Start Conversion Trigger Sources

Data conversion can be initiated by a software trigger, a General-Purpose Timer Module (GPTM) event or an external trigger. Each trigger source can be enabled by setting the corresponding enable control bit in the ADCTCR register and then selected by configuring the associated selection bits in the ADCTSR or register to start a group channel conversion.

An A/D converter conversion can be started by setting the software trigger bit ADSC in the ADCTSR register for the regular group channel when the software trigger enable bit ADSW in the ADCTCR register is set to 1. After the A/D converter starts converting the analog data, the corresponding enable bit ADSC will be cleared to 0 automatically.

The A/D converter can also be triggered to start a regular channel conversion by a GPTM event. The GPTM events include a GPTM master trigger output MTO and four GPTM channel outputs CH0~CH3. If the GPTM trigger enable bit ADTM is set to 1 and the MTO or CHn event is selected via the GPTM event selection bits, the A/D converter will start a conversion when a rising edge of the selected trigger event occurs.

In addition to the internal trigger sources, the A/D converter can be triggered to start a conversion by an external trigger event. The external trigger event is derived from the external lines EXTIn. If the external trigger enable bit ADEXTI is set to 1 and the corresponding EXTI line is selected by configuring the ADEXTIS for regular group, the A/D converter will start a conversion when an EXTI line rising edge occurs.

Sampling Time Setting

Each conversion channel can be sampled with a different sampling time. By modifying the ADSTn[7:0] bits in the ADCSTRn (n = 0~7) registers, the sampling time of the analog input signal can be determined.

The total conversion time (Tconv) is calculated using the following formula:

```
Tconv = TSampling + TLatency
```

Where the minimum sampling time TSampling = 1.5 cycles (when ADSTn [7:0] = 0) and the minimum channel conversion latency TLatency = 12.5 cycles

Example:

With the A/D Converter clock CK_ADC = 14 MHz and a sampling time =1.5 cycles:

```
Tconv = 1.5 + 12.5 = 14 cycles = 1 µs
```

Data Alignment

The ADC converted result has a right-aligned and unsigned output format as follows:

```
"0000_d11_d10_d9_d8_d7_d6_d5_d4_d3_d2_d1_d0'.
```

If it is required to turn off the A/D converter, the A/D clock enable bit ADCEN should be cleared to 0 for at least two A/D clock cycles to disable the A/D converter function.

Analog Watchdog

The A/D converter includes a watchdog function to monitor the converted data. There are two kinds of thresholds for the watchdog monitor function, known as the watchdog upper threshold and watchdog lower threshold, which are specified in the Watchdog Upper and Lower Threshold Registers respectively. The watchdog monitor function is enabled by setting the watchdog upper and lower threshold monitor function enable bits, ADWUE and ADWLE, in the watchdog control register ADCWCR. The channel to be monitored can be specified by configuring the ADWCH and ADWALL bits. When the converted data is less or higher than the lower or upper threshold, as defined in the ADCLTR or ADCUTR registers respectively, the watchdog lower or upper threshold interrupt raw flags, ADIRAWL or ADIRAWU in the ADCIRAW register, will be asserted if the watchdog lower or upper threshold monitor function is enabled. If the lower or upper threshold interrupt raw flag is asserted and the corresponding interrupt is enabled by setting the ADIML or ADIMU bit in the ADCIME register, the A/D watchdog lower or upper threshold interrupt will be generated.

Interrupts

When an A/D conversion is completed, an End of Conversion EOC event will occur. There are three kinds of EOC events which are known as single sample EOC, subgroup EOC and cycle EOC for A/D conversion. A single sample EOC event will occur and the single sample EOC interrupt raw flag, ADIRAWS bits in the ADCIRAW register, will be asserted when a single channel conversion has completed. A subgroup EOC event will occur and the subgroup EOC interrupt raw flag, ADIRAWG in the ADCIRAW register, will be asserted when a subgroup conversion has completed. A cycle EOC event will occurs and the cycle EOC interrupt raw flag, ADIRAWC bits in the ADCIRAW register, will be asserted when a cycle conversion is finished. When a single sample EOC, a subgroup EOC or a cycle EOC raw flag is asserted and the corresponding interrupt enable bit, ADIMC, ADIMG or ADIMS bit in the ADCIMR register, is set to 1, the associated interrupt will be generated.

After a conversion has completed, the 12-bit digital data will be stored in the associated ADCDRn register and the value of the data valid flag named as ADVLDn will be changed from low to high. The converted data should be read by the application program, after which the data valid flag ADVLDn will be automatically changed from high to low. Otherwise, a data overwrite event will occur and the data overwrite interrupt raw flag ADIRAWO bit in the ADCIRAW register will be asserted. When the related data overwrite raw flag is asserted, the data overwrite interrupt will be generated if the interrupt enable bit ADIMO in the ADCIMR register is set to 1.

If the A/D watchdog monitor function is enabled and the data after a channel conversion is less than the lower threshold or higher than the upper threshold, the watchdog lower or upper threshold interrupt raw flag ADIRAWL or ADIRAWU in the ADCIRAW register will be asserted. When the ADIRAWL or ADIRAWU flag is asserted and the corresponding interrupt enable bit, ADIML or ADIMU in the ADCIMR register, is set a watchdog lower or upper threshold interrupt will be generated.

The A/D Converter interrupt clear bits used to clear the associated A/D converter interrupt raw and masked status bits. Writing 1 into the specific A/D converter interrupt clear bit in the A/D converter interrupt clear register ADCICLR will clear the corresponding A/D converter interrupt raw and masked status bits. These bits are automatically cleared to 0 by hardware after being set to 1.

Register Map

The following table shows the ADC registers and reset values.

Table 26. Register Map of ADC

Register	Offset	Description	Reset Value
ADC Base Address = 0x4001_0000			
ADCRST	0x004	ADC Reset Register	0x0000_0000
ADCCONV	0x008	ADC Regular Conversion Mode Register	0x0000_0000
ADCLST0	0x010	ADC Regular Conversion List Register 0	0x0000_0000
ADCLST1	0x014	ADC Regular Conversion List Register 1	0x0000_0000
ADCSTR0	0x070	ADC Input 0 Sampling Time Register	0x0000_0000
ADCSTR1	0x074	ADC Input 1 Sampling Time Register	0x0000_0000
ADCSTR2	0x078	ADC Input 2 Sampling Time Register	0x0000_0000
ADCSTR3	0x07C	ADC Input 3 Sampling Time Register	0x0000_0000
ADCSTR4	0x080	ADC Input 4 Sampling Time Register	0x0000_0000
ADCSTR5	0x084	ADC Input 5 Sampling Time Register	0x0000_0000
ADCSTR6	0x088	ADC Input 6 Sampling Time Register	0x0000_0000
ADCSTR7	0x08C	ADC Input 7 Sampling Time Register	0x0000_0000
ADCDR0	0x0B0	ADC Regular Conversion Data Register 0	0x0000_0000
ADCDR1	0x0B4	ADC Regular Conversion Data Register 1	0x0000_0000
ADCDR2	0x0B8	ADC Regular Conversion Data Register 2	0x0000_0000
ADCDR3	0x0BC	ADC Regular Conversion Data Register 3	0x0000_0000
ADCDR4	0x0C0	ADC Regular Conversion Data Register 4	0x0000_0000
ADCDR5	0x0C4	ADC Regular Conversion Data Register 5	0x0000_0000
ADCDR6	0x0C8	ADC Regular Conversion Data Register 6	0x0000_0000
ADCDR7	0x0CC	ADC Regular Conversion Data Register 7	0x0000_0000
ADCTCR	0x100	ADC Regular Trigger Control Register	0x0000_0000
ADCTSR	0x104	ADC Regular Trigger Source Register	0x0000_0000
ADCWCR	0x120	ADC Watchdog Control Register	0x0000_0000
ADCLTR	0x124	ADC Watchdog Lower Threshold Register	0x0000_0000
ADCUTR	0x128	ADC Watchdog Upper Threshold Register	0x0000_0000
ADCIMR	0x130	ADC Interrupt Mask Enable register	0x0000_0000
ADCIRAW	0x134	ADC Interrupt Raw Status Register	0x0000_0000
ADCIMASK	0x138	ADC Interrupt Masked Status Register	0x0000_0000
ADCICLR	0x13C	ADC Interrupt Clear Register	0x0000_0000

Register Descriptions

ADC Reset Register (ADCRST)

This register is used to reset the A/D Converter by software.

Offset: 0x004

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved							ADRST
Type/Reset								RW 0

Bits	Field	Descriptions
[0]	ADRST	ADC Software Reset 0: No reset 1: Reset A/D converter except for the A/D Converter registers.

ADC Regular Conversion Mode Register (ADCCONV)

This register specifies the mode setting, sequence length and subgroup length of the A/D Converter regular group conversion. Note that once the contents of the ADCCONV register have changed, any regular conversion presently in progress will be aborted and the A/D Converter will be reset. The application program has to wait for at least one A/D converter clock CK_ADC before issuing the next command.

Offset: 0x008

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved					ADSUBL		
Type/Reset					RW 0	RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
	Reserved					ADSEQL		
Type/Reset					RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	Reserved						ADMODE	
Type/Reset							RW 0	RW 0

Bits	Field	Descriptions
[18:16]	ADSUBL	A/D Converter Regular Conversion Subgroup Length The ADSUBL field specifies the conversion channel length of each subgroup for the regular group in the discontinuous mode. The subgroup length is equal to the ADSUBL value plus 1. If the regular sequence length is not a multiple of the regular subgroup length, the last subgroup will be the rest of the regular group channels that have not been converted.
[10:8]	ADSEQL	A/D Converter Regular Conversion Sequence Length The ADSEQL field specifies the conversion length of the whole sequence for the regular group. The sequence length is equal to the ADSEQL value plus 1.
[1:0]	ADMODE	A/D Converter Regular Conversion Mode regular channels for the whole sequence continuously until the conversion mode is changed.

ADMODE [1:0]	Mode	Descriptions
00	One shot mode	After a start trigger, the conversion will be executed on the whole sequence of the regular channels once.
01	Reserved	
10	Continuous mode	After a start trigger, the conversion will be executed on the regular channels for the whole sequence continuously until the conversion mode is changed.
11	Discontinuous mode	After a start trigger, the conversion will be executed on the current regular subgroup. When the last subgroup is finished, the conversion restarts from the first subgroup.

ADC Regular Conversion List Register 0 (ADCLST0)

This register specifies the conversion sequence order No.0 ~ No.3 of the A/D Converter regular group.

Offset: 0x010

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved			ADSEQ3				
Type/Reset				RW 0	RW 0	RW 0	RW 0	RW 0
	23	22	21	20	19	18	17	16
	Reserved			ADSEQ2				
Type/Reset				RW 0	RW 0	RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
	Reserved			ADSEQ1				
Type/Reset				RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	Reserved			ADSEQ0				
Type/Reset				RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[28:24]	ADSEQ3	A/D Converter Regular Conversion Sequence No.3 Define the A/D Converter input channel order No.3 of the regular conversion sequence. 0x00~0x07: ADC_IN0 ~ ADC_IN7 0x08 ~ 0x0F: Reserved. 0x10: Analog ground, V_{SSA} (V_{REF-}) 0x11: Analog power, V_{DDA} (V_{REF+}) 0x12 ~ 0x1F: Invalid setting. These values must not be selected as they may cause abnormal ADC operation.
[20:16]	ADSEQ2	A/D Converter Regular Conversion Sequence No.2 Define the A/D Converter input channel order No.2 of the regular conversion sequence. 0x00~0x07: ADC_IN0 ~ ADC_IN7 0x08 ~ 0x0F: Reserved. 0x10: Analog ground, V_{SSA} (V_{REF-}) 0x11: Analog power, V_{DDA} (V_{REF+}) 0x12 ~ 0x1F: Invalid setting. These values must not be selected as they may cause abnormal ADC operation
[12:8]	ADSEQ1	A/D Converter Regular Conversion Sequence No.1 Define the A/D Converter input channel order No.1 of the regular conversion sequence. 0x00~0x07: ADC_IN0 ~ ADC_IN7 0x08 ~ 0x0F: Reserved. 0x10: Analog ground, V_{SSA} (V_{REF-}) 0x11: Analog power, V_{DDA} (V_{REF+}) 0x12 ~ 0x1F: Invalid setting. These values must not be selected as they may cause abnormal ADC operation.
[4:0]	ADSEQ0	A/D Converter Regular Conversion Sequence No.0 Define the A/D Converter input channel order No.0 of the regular conversion sequence. 0x00~0x07: ADC_IN0 ~ ADC_IN7 0x08 ~ 0x0F: Reserved. 0x10: Analog ground, V_{SSA} (V_{REF-}) 0x11: Analog power, V_{DDA} (V_{REF+}) 0x12 ~ 0x1F: Invalid setting. These values must not be selected as they may cause abnormal ADC operation

ADC Regular Conversion List Register 1 (ADCLST1)

This register specifies the conversion sequence order No.4 ~ No.7 of the A/D Converter regular group.

Offset: 0x014

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved			ADSEQ7				
Type/Reset				RW 0	RW 0	RW 0	RW 0	RW 0
	23	22	21	20	19	18	17	16
	Reserved			ADSEQ6				
Type/Reset				RW 0	RW 0	RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
	Reserved			ADSEQ5				
Type/Reset				RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	Reserved			ADSEQ4				
Type/Reset				RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[28:24]	ADSEQ7	A/D Converter Regular Conversion Sequence No.7 Define the A/D Converter input channel order No.7 of the regular conversion sequence. 0x00~0x07: ADC_IN0 ~ ADC_IN7 0x08 ~ 0x0F: Reserved. 0x10: Analog ground, V_{SSA} (V_{REF-}) 0x11: Analog power, V_{DDA} (V_{REF+}) 0x12 ~ 0x1F: Invalid setting. These values must not be selected as they may cause abnormal ADC operation.
[20:16]	ADSEQ6	A/D Converter Regular Conversion Sequence No.6 Define the A/D Converter input channel order No.6 of the regular conversion sequence. 0x00~0x07: ADC_IN0 ~ ADC_IN7 0x08 ~ 0x0F: Reserved. 0x10: Analog ground, V_{SSA} (V_{REF-}) 0x11: Analog power, V_{DDA} (V_{REF+}) 0x12 ~ 0x1F: Invalid setting. These values must not be selected as they may cause abnormal ADC operation.
[12:8]	ADSEQ5	A/D Converter Regular Conversion Sequence No.5 Define the A/D Converter input channel order No.5 of the regular conversion sequence. 0x00~0x07: ADC_IN0 ~ ADC_IN7 0x08 ~ 0x0F: Reserved. 0x10: Analog ground, V_{SSA} (V_{REF-}) 0x11: Analog power, V_{DDA} (V_{REF+}) 0x12 ~ 0x1F: Invalid setting. These values must not be selected as they may cause abnormal ADC operation.
[4:0]	ADSEQ4	A/D Converter Regular Conversion Sequence No.4 Define the A/D Converter input channel order No.4 of the regular conversion sequence. 0x00~0x07: ADC_IN0 ~ ADC_IN7 0x08 ~ 0x0F: Reserved. 0x10: Analog ground, V_{SSA} (V_{REF-}) 0x11: Analog power, V_{DDA} (V_{REF+}) 0x12 ~ 0x1F: Invalid setting. These values must not be selected as they may cause abnormal ADC operation

ADC Input Sampling Time Register n (ADCSTRn, n = 0 ~ 7)

This register specifies the sampling time of the A/D Converter channel n.

Offset: 0x070 ~ 0x08C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	ADSTn							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[7:0]	ADSTn	A/D Converter Input Channel n Sampling Time (n = 0 ~ 7) Sampling time = (ADSTn [7:0] + 1.5) A/D Converter clock cycles.

ADC Regular Conversion Data Register n (ADCDRn, n = 0 ~ 7)

This register is used to store the conversion data of the regular conversion sequence No.n

Offset: 0x0B0 ~ 0x0EC

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	ADVLDn	Reserved						
Type/Reset	RC 0							
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	Reserved							
Type/Reset								
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	ADDn							
Type/Reset	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	ADDn							
Type/Reset	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0

Bits	Field	Descriptions
[31]	ADVLDn	A/D Converter Regular Conversion Data of the sequence No.n Valid Bit (n = 0 ~ 7) 0: Data is invalid or has been read 1: New data is valid
[15:0]	ADDn	A/D Converter Regular Conversion Data of the sequence No.n (n = 0 ~ 7) The regular channel conversion result of the sequence No.n defined in the ADCLST register.

ADC Regular Trigger Control Register (ADCTCR)

This register contains the A/D start conversion trigger enable bits of the regular conversion.

Offset: 0x100

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved					ADTM	ADEXTI	ADSW
Type/Reset						RW 0	RW 0	RW 0

Bits	Field	Descriptions
[2]	ADTM	A/D Converter Regular Conversion GPTM Event Trigger Enable control 0: Disable the regular conversion triggered by the GPTM events 1: Enable the regular conversion triggered by the GPTM events
[1]	ADEXTI	A/D Converter Regular Conversion EXTI Event Trigger Enable control 0: Disable the regular conversion triggered by the EXTI lines 1: Enable the regular conversion triggered by the EXTI lines
[0]	ADSW	A/D Converter Regular Conversion Software Trigger Enable control 0: Disable the regular conversion triggered by the software trigger bit 1: Enable the regular conversion triggered by the software trigger bit

ADC Regular Trigger Source Register (ADCTSR)

This register contains the trigger source selection and the software trigger bit of the regular conversion.

Offset: 0x104

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved					GPTME		
Type/Reset						RW 0	RW 0	RW 0
	23	22	21	20	19	18	17	16
	Reserved					GPTMS		
Type/Reset						RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
	Reserved				ADEXTIS			
Type/Reset					RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	Reserved							ADSC
Type/Reset								RW 0

Bits	Field	Descriptions
[26:24]	GPTME	GPTM Trigger Event Selection of the A/D Converter Regular Conversion 000: GPTM MTO rising edge 001: GPTM CH0 rising edge 010: GPTM CH1 rising edge 011: GPTM CH2 rising edge 100: GPTM CH3 rising edge Others: Reserved -should not be used, otherwise, the conversion results will be unpredictable.
[18:16]	GPTMS	GPTM Trigger Timer Selection of the A/D Converter Regular Conversion 010: GPTM0 011: GPTM1 Others: Reserved -should not be used, otherwise, the results will be unpredictable.
[11:8]	ADEXTIS	EXTI Trigger Source Selection of the A/D Converter Regular Conversion 0x0: EXTI line 0 rising edge 0x1: EXTI line 1 rising edge … 0xF: EXTI line 15 rising edge
[0]	ADSC	A/D Converter Regular Conversion Software Trigger Bit 0: No effect 1: Start the regular conversion This bit is set by software to start the regular conversion manually and then cleared by hardware automatically at the next A/D Converter clock cycle.

ADC Watchdog Control Register (ADCWCR)

This register provides the control bits and status of the A/D Converter watchdog function.

Offset: 0x120

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved				ADUCH			
Type/Reset					RO 0	RO 0	RO 0	RO 0
	23	22	21	20	19	18	17	16
	Reserved				ADLCH			
Type/Reset					RO 0	RO 0	RO 0	RO 0
	15	14	13	12	11	10	9	8
	Reserved				ADWCH			
Type/Reset					RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	Reserved					ADWALL	ADWUE	ADWLE
Type/Reset						RW 0	RW 0	RW 0

Bits	Field	Descriptions
[27:24]	ADUCH	Channel Upper Threshold Status 0000: ADC_IN0 converted data is higher than the threshold ADUT defined in the ADCUTR register. 0001: ADC_IN1 converted data is higher than the threshold ADUT defined in the ADCUTR register. ... 0111: ADC_IN7 converted data is higher than the threshold ADUT defined in the ADCUTR register. Others: Reserved If one of these statuses is set to 1 by the watchdog monitor function, the status field must be stored in the user-defined memory location first in the corresponding ISR. Otherwise, the ADUCH field will be changed if another channel upper threshold event occurs.
[19:16]	ADLCH	Channel Lower Threshold Status 0000: ADC_IN0 converted data is lower than the threshold ADLT defined in the ADCLTR register. 0001: ADC_IN1 converted data is lower than the threshold ADLT defined in the ADCLTR register. ... 0111: ADC_IN7 converted data is lower than the threshold ADLT defined in the ADCLTR register. Others: Reserved If one of these statuses is set to 1 by the watchdog monitor function, the status field must be stored in the user-defined memory location first in the corresponding ISR. Otherwise, the ADLCH field will be changed if another channel lower threshold event occurs.
[11:8]	ADWCH	A/D Converter Channel Selection for Watchdog function 0000: ADC_IN0 is monitored 0001: ADC_IN1 is monitored ... 0111: ADC_IN7 is monitored Others: Reserved

Bits	Field	Descriptions
[2]	ADWALL	A/D Converter Specific or All Channel control for watchdog function 0: Only the channel specified by the ADWCH field is monitored 1: All channels are monitored
[1]	ADWUE	A/D Converter Watchdog Upper Threshold Monitor Enable Bit 0: Disable the upper threshold monitor function 1: Enable the upper threshold monitor function
[0]	ADWLE	A/D Converter Watchdog Lower Threshold Monitor Enable Bit 0: Disable the lower threshold monitor function 1: Enable the lower threshold monitor function

ADC Watchdog Lower Threshold Register (ADCLTR)

This register specifies the lower threshold of the A/D Converter watchdog function.

Offset: 0x124

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved				ADLT			
Type/Reset					RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	ADLT							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[11:0]	ADLT	A/D Converter Watchdog Lower Threshold Value Specifies the lower threshold of the A/D Conversion data.

ADC Watchdog Upper Threshold Register (ADCUTR)

This register specifies the upper threshold of the A/D Converter watchdog function.

Offset: 0x128

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved				ADUT			
Type/Reset					RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	ADUT							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[11:0]	ADUT	A/D Converter Watchdog Upper Threshold Value Specifies the upper threshold of the A/D Conversion data.

ADC Interrupt Mask Enable Register (ADCIMR)

This register contains the A/D Converter interrupt enable bits.

Offset: 0x130

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							ADIMO
Type/Reset								RW 0
	23	22	21	20	19	18	17	16
	Reserved						ADIMU	ADIML
Type/Reset							RW 0	RW 0
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved					ADIMC	ADIMG	ADIMS
Type/Reset						RW 0	RW 0	RW 0

Bits	Field	Descriptions
[24]	ADIMO	A/D Converter Regular Data Register Overwrite Interrupt Mask 0: A/D Converter regular data register overwrite interrupt is masked 1: A/D Converter regular data register overwrite interrupt is not masked
[17]	ADIMU	A/D Converter Watchdog Upper Threshold Interrupt Mask 0: A/D Converter watchdog upper threshold interrupt is masked 1: A/D Converter watchdog upper threshold interrupt is not masked
[16]	ADIML	A/D Converter Watchdog Lower Threshold Interrupt Mask 0: A/D Converter watchdog lower threshold interrupt is masked 1: A/D Converter watchdog lower threshold interrupt is not masked
[2]	ADIMC	A/D Converter Regular Cycle EOC Interrupt Mask 0: A/D Converter regular cycle end of conversion interrupt is masked 1: A/D Converter regular cycle end of conversion interrupt is not masked
[1]	ADIMG	A/D Converter Regular Subgroup EOC Interrupt Mask 0: A/D Converter regular subgroup end of conversion interrupt is masked 1: A/D Converter regular subgroup end of conversion interrupt is not masked
[0]	ADIMS	A/D Converter Regular Single EOC Interrupt Mask 0: A/D Converter regular single sample end of conversion interrupt is masked 1: A/D Converter regular single sample end of conversion interrupt is not masked

ADC Interrupt Raw Status Register (ADCIRAW)

This register contains the A/D Converter interrupt raw status bits.

Offset: 0x134

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							ADIRAWO
Type/Reset								RO 0
	23	22	21	20	19	18	17	16
	Reserved						ADIRAWU	ADIRAWL
Type/Reset							RO 0	RO 0
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved					ADIRAWC	ADIRAWG	ADIRAWS
Type/Reset						RO 0	RO 0	RO 0

Bits	Field	Descriptions
[24]	ADIRAWO	A/D Converter Regular Data Register Overwrite Interrupt Raw Status 0: A/D Converter regular data register overwrite event does not occur 1: A/D Converter regular data register overwrite event occurs The A/D Converter regular data overwrite event will occur at the end of the 3rd regular conversion if the 1st regular conversion data has not been read by the application program.
[17]	ADIRAWU	A/D Converter Watchdog Upper Threshold Interrupt Raw Status 0: A/D Converter watchdog upper threshold event does not occur 1: A/D Converter watchdog upper threshold event occurs
[16]	ADIRAWL	A/D Converter Watchdog Lower Threshold Interrupt Raw Status 0: A/D Converter watchdog lower threshold event does not occur 1: A/D Converter watchdog lower threshold event occurs
[2]	ADIRAWC	A/D Converter Regular Cycle EOC Interrupt Raw Status 0: A/D Converter regular cycle end of conversion event does not occur 1: A/D Converter regular cycle end of conversion event occurs
[1]	ADIRAWG	A/D Converter Regular Subgroup EOC Interrupt Raw Status 0: A/D Converter regular subgroup end of conversion event does not occur 1: A/D Converter regular subgroup end of conversion event occurs
[0]	ADIRAWS	A/D Converter Regular Single EOC Interrupt Raw Status 0: A/D Converter regular single sample end of conversion event does not occur 1: A/D Converter regular single sample end of conversion event occurs

ADC Interrupt Masked Status Register (ADCIMASK)

This register contains the A/D Converter interrupt masked status bits. The corresponding masked status will be set to 1 if the associated interrupt event occurs and the related enable bit is set to 1.

Offset: 0x138

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							ADIMASKO
Type/Reset								RO 0
	23	22	21	20	19	18	17	16
	Reserved						ADIMASKU	ADIMASKL
Type/Reset							RO 0	RO 0
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved					ADIMASKC	ADIMASKG	ADIMASKS
Type/Reset						RO 0	RO 0	RO 0

Bits	Field	Descriptions
[24]	ADIMASKO	A/D Converter Regular Data Register Overwrite Interrupt Masked Status 0: A/D Converter regular data register overwrite event does not occur or the related interrupt control is disabled. 1: A/D Converter regular data register overwrite interrupt occurs as the related interrupt control is enabled.
[17]	ADIMASKU	A/D Converter Watchdog Upper Threshold Interrupt Masked Status 0: A/D Converter watchdog upper threshold event does not occur or the related interrupt control is disabled. 1: A/D Converter watchdog upper threshold interrupt occurs as the related interrupt control is enabled.
[16]	ADIMASKL	A/D Converter Watchdog Lower Threshold Interrupt Masked Status 0: A/D Converter watchdog lower threshold event does not occur or the related interrupt control is disabled. 1: A/D Converter watchdog lower threshold interrupt occurs as the related interrupt control is enabled.
[2]	ADIMASKC	A/D Converter Regular Cycle EOC Interrupt Masked Status 0: A/D Converter regular cycle end of conversion event does not occur or the related interrupt control is disabled. 1: A/D Converter regular cycle end of conversion interrupt occurs as the related interrupt control is enabled.
[1]	ADIMASKG	A/D Converter Regular Subgroup EOC Interrupt Masked Status 0: A/D Converter regular subgroup end of conversion event does not occur or the related interrupt control is disabled. 1: A/D Converter regular subgroup end of conversion interrupt occurs as the related interrupt control is enabled.
[0]	ADIMASKS	A/D Converter Regular Single EOC Interrupt Masked Status 0: A/D Converter regular single sample end of conversion event does not occur or the related interrupt control is disabled. 1: A/D Converter regular single sample end of conversion interrupt occurs as the related interrupt control is enabled.

ADC Interrupt Clear Register (ADCICLR)

This register provides the clear bits used to clear the interrupt raw and masked status of the A/D Converter. These bits are set to 1 by software to clear the interrupt status and automatically cleared to 0 by hardware after being set to 1.

Offset: 0x13C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							ADICLRO
Type/Reset								WO 0
	23	22	21	20	19	18	17	16
	Reserved						ADICLRU	ADICLRL
Type/Reset							WO 0	WO 0
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved					ADICLRC	ADICLRG	ADICLRS
Type/Reset						WO 0	WO 0	WO 0

Bits	Field	Descriptions
[24]	ADICLRO	A/D Converter Regular Data Register Overwrite Interrupt Status Clear Bit 0: No effect 1: Clear ADIRAWO and ADIMASKO bits
[17]	ADICLRU	A/D Converter Watchdog Upper Threshold Interrupt Status Clear Bit 0: No effect 1: Clear ADIRAWU and ADIMASKU bits
[16]	ADICLRL	A/D Converter Watchdog Lower Threshold Interrupt Status Clear Bit 0: No effect 1: Clear ADIRAWL and ADIMASKL bits
[2]	ADICLRC	A/D Converter Regular Cycle EOC Interrupt Status Clear Bit 0: No effect 1: Clear ADIRAWC and ADIMASKC bits
[1]	ADICLRG	A/D Converter Regular Subgroup EOC Interrupt Status Clear Bit 0: No effect 1: Clear ADIRAWG and ADIMASKG bits
[0]	ADICLRS	A/D Converter Regular Single EOC Interrupt Status Clear Bit 0: No effect 1: Clear ADIRAWS and ADIMASKS bits

13 Operational Amplifier/Comparator (OPA/CMP)

Introduction

Two Operational Amplifiers/Comparators (OPA/CMP) are implemented within the devices. They can be configured either as Operational Amplifiers or as Analog Comparators. When configured as comparators, they are capable of asserting interrupts to the NVIC.

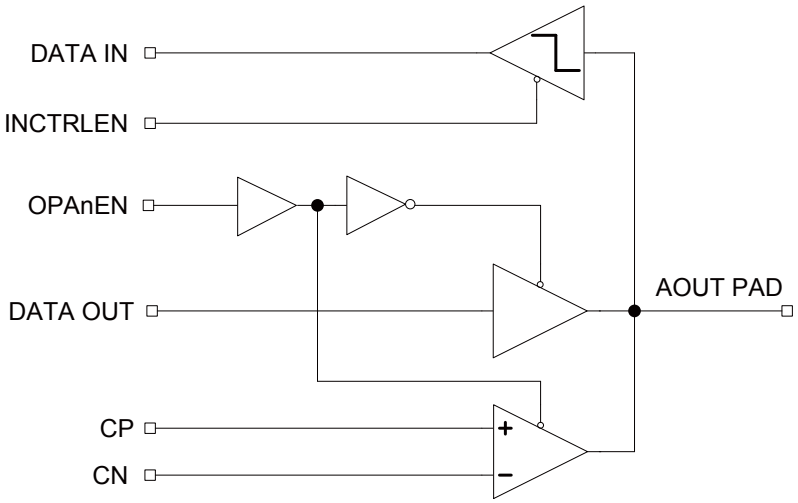


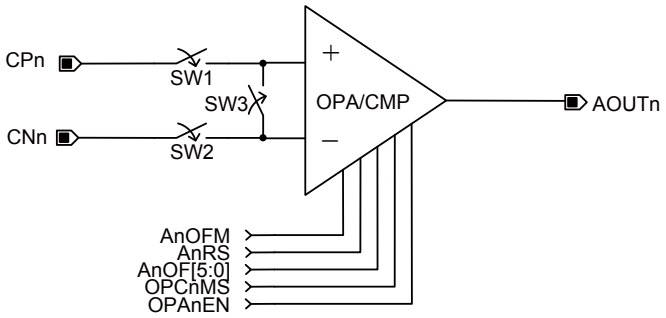
Figure 29. Simplied Block Diagram of OPA/CMP with Digital I/O

Features

- Operational Amplifier or Comparator function determined by software
- Supply Voltage Range: 2.7 V ~ 3.6 V
- Typical Operating Current: 230 uA (@V_{DD} = 3.3 V and Room Temperature = 25°C)
- Power Down Supply Current (OPAnEN = 0 and AnOFM = 0): < 0.1 uA
- Comparator Offset (After Calibration): < ±1 mV
- Comparator Response Time: < 2 us (@ overdrive voltage = 10 mV)

Functional Descriptions

Functional Diagram



AnOFM	AnRS	SW1	SW2	SW3
0	X	ON	ON	OFF
1	0	OFF	ON	ON
1	1	ON	OFF	ON

Figure 30. OPA/CMP Functional Diagram

Table 27. OPA/CMP Functional Signal Definition

AnOFM	AnRS	SW1	SW2	SW3
0	X	ON	ON	OFF
1	0	OFF	ON	ON
1	1	ON	OFF	ON

Interrupts and Status

The analog comparator can generate an interrupt when its output waveform generates a rising or falling edge and its corresponding interrupt enable control bit is also set.

For example, when a comparator output rising edge occurs, the comparator rising edge raw flag CRnRAW in the Comparator Raw Status Register CMPRSRn will be set. If the comparator output rising edge interrupt enable control bit CRnIEN in the Comparator Interrupt Enable Register CMPIERn is enabled, the comparator output rising edge masked interrupt status bit CRnIS in the Comparator Masked Interrupt Status Register CMPISRn, will be set when the comparator output rising edge occurs. An interrupt will then be generated and sent to the NVIC unit. Writing 1 into the comparator output rising edge interrupt clear bit CRnICLR in the Comparator Interrupt Clear Register CMPICLRn will clear the CRnIS and CRnRAW status bits. The comparator output falling edge interrupt also has the same corresponding interrupt setting.

Offset Cancellation Procedures

The device provides an offset cancellation function. Users can cancel the input voltage offset by using a specific procedure by configuring the corresponding registers. The offset cancellation procedure is shown in the following steps.

Cancellation procedure:

1. Set the AnOFM bit in the OPACRn register to 1 to enter the offset cancellation mode.
2. Configure the AnRS bit in the OPACRn register to select whether the reference voltage input comes from the comparator negative or positive input pin. If the AnRS bit is set to 1, the reference voltage input will come from the comparator positive input pin. Otherwise, the reference voltage input will come from the comparator negative input pin when the AnRS bit is cleared to 0.
3. Specify the OFVCRn register with a value of 0x00 to start the cancellation procedure.
4. If the CMPnS bit in the OPACRn register is equal to 0, then increase the OFVCRn register content AnOF by 1 and check whether the CMPnS bit state has changed from 0 to 1. If not then keep increasing the register content until the CMPnS bit state changes from 0 to 1
5. When the CMPnS bit changes to 1, then the AnOF data which is equal to N or (N-1) is the specific value written into the OFVCRn register to cancel the comparator input offset voltage.

Note that the reference input voltage must be in the range from (V_{DDA}-1.2V) to (V_{SSA}+0.5V) to obtain a more accurate cancellation result.

Register Map

The following table shows the OPA/CMP registers and reset values.

Table 28. Register Map of OPA/CMP

Register	Offset	Description	Reset Value
OPCMP Base Address = 0x4001_8000			
OPACR0	0x000	Operational Amplifier Control Register 0	0x0000_0000
OFVCR0	0x004	Comparator Input Offset Voltage Cancellation Register 0	0x0000_0000
CMPIER0	0x008	Comparator Interrupt Enable Register 0	0x0000_0000
CMPRSR0	0x00C	Comparator Raw Status Register 0	0x0000_0000
CMPISR0	0x010	Comparator Interrupt Status Register 0	0x0000_0000
CMPICLR0	0x014	Comparator Interrupt Clear Register 0	NA
OPACR1	0x100	Operational Amplifier Control Register 1	0x0000_0000
OFVCR1	0x104	Comparator Input Offset Voltage Cancellation Register 1	0x0000_0000
CMPIER1	0x108	Comparator Interrupt Enable Register 1	0x0000_0000
CMPRSR1	0x10C	Comparator Raw Status Register 1	0x0000_0000
CMPISR1	0x110	Comparator Interrupt Status Register 1	0x0000_0000
CMPICLR1	0x114	Comparator Interrupt Clear Register 1	NA

Register Descriptions

Operational Amplifier Control Register n (OPACRn, n = 0 or 1)

This register contains the OPA/CMP enable control, the OPA/CMP mode selection, input offset cancellation control bits and the comparator digital output status.

Offset: 0x000 (0), 0x100 (1)

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							CMPnS
Type/Reset								RO 0
	7	6	5	4	3	2	1	0
	Reserved				AnRS	AnOFM	OPCnMS	OPAnEN
Type/Reset					RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[8]	CMPnS	Comparator Digital Output Status This bit is read only and has the same polarity as the Comparator output. It can be used for the software to monitor the Comparator output in the input offset voltage cancellation mode.
[3]	AnRS	Operational Amplifier Input Offset Cancellation Reference Voltage Selection Bit 0: Comparator negative input is selected as the reference input 1: Comparator positive input is selected as the reference input
[2]	AnOFM	Operational Amplifier / Comparator Mode or Input Offset Voltage Cancellation Mode Selection 0: Operational Amplifier / Comparator mode 1: Input offset voltage cancellation mode
[1]	OPCnMS	Operational Amplifier or Comparator Mode Selection 0: Operational Amplifier mode 1: Comparator mode
[0]	OPAnEN	Operational Amplifier / Comparator Enable Control Bit 0: Disable Operational Amplifier / Comparator (entering the power down mode) 1: Enable Operational Amplifier / Comparator

Comparator Input Offset Voltage Cancellation Register n (OFVCRn, n = 0 or 1)

This register is used to cancel the comparator n input offset voltage.

Offset: 0x004 (0), 0x104 (1)

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved		AnOF					
Type/Reset			RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[5:0]	AnOF	Operational Amplifier / Comparator Input Offset Voltage Cancellation Control Bit 000000: Minumun ... 100000: Center ... 111111: Maxumun

Comparator Interrupt Enable Register n (CMPIERn, n = 0 or 1)

This register provides the comparator n output transition interrupt enable control bits.

Offset: 0x008 (0), 0x108 (1)

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved						CRnIEN	CFnIEN
Type/Reset							RW 0	RW 0

Bits	Field	Descriptions
[1]	CRnIEN	Comparator Output Rising Edge Interrupt Enable Control Bit 0: Comparator output rising edge interrupt is disabled. 1: Comparator output rising edge interrupt is enabled.
[0]	CFnIEN	Comparator Output Falling Edge Interrupt Enable Control Bit 0: Comparator output falling edge interrupt is disabled. 1: Comparator output falling edge interrupt is enabled.

Comparator Raw Status Register n (CMPRSRn, n = 0 or 1)

This register contains the comparator n output transition event raw status.

Offset: 0x00C (0), 0x10C (1)

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved						CRnRAW	CFnRAW
Type/Reset							RO 0	RO 0

Bits	Field	Descriptions
[1]	CRnRAW	Comparator Output Rising Edge Raw Flag Bit. 0: No Comparator output rising edge occurs. 1: Comparator rising output edge occurs. This bit can be cleared by writing 1 into the CRnICLR bit in the CMPICLRn register.
[0]	CFnRAW	Comparator Output Falling Edge Interrupt Raw Flag Bit. 0: No Comparator output falling edge occurs. 1: Comparator output falling edge occurs. This bit can be cleared by writing 1 into the CFnICLR bit in the CMPICLRn register.

Comparator Masked Interrupt Status Register n (CMPISRn, n = 0 or 1)

This register contains the comparator n transition event masked interrupt status.

Offset: 0x010 (0), 0x110 (1)

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved						CRnIS	CFnIS
Type/Reset							RO 0	RO 0

Bits	Field	Descriptions
[1]	CRnIS	Comparator Output Rising Edge Masked Interrupt Flag Bit 0: No Comparator output rising edge occurs or the Comparator output rising edge interrupt is disabled. 1: Comparator output rising edge occurs and the Comparator output rising edge interrupt is enabled.
[0]	CFnIS	Comparator Output Falling Edge Masked Interrupt Flag Bit 0: No Comparator output falling edge occurs or the Comparator output falling edge interrupt is disabled. 1: Comparator output falling edge occurs and the Comparator output falling edge interrupt is enabled.

Comparator Interrupt Clear Register n (CMPICLRn, n = 0 or 1)

The register provides the interrupt status clear bits used to indicate the comparator n output transition interrupt raw and masked status. These bits are set to 1 by software to clear the associated interrupt raw and masked status bits and cleared to 0 by hardware automatically after being set to 1.

Offset: 0x014 (0), 0x114 (1)

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved						CRnICLR	CFnICLR
Type/Reset							WO 0	WO 0

Bits	Field	Descriptions
[1]	CRnICLR	Comparator Output Rising Edge Interrupt status Clear Control Bit 0: No effect 1: Comparator output rising edge interrupt raw status and masked status is cleared.
[0]	CFnICLR	Comparator Output Falling Edge Interrupt status Clear Control Bit 0: No effect 1: Comparator output falling edge interrupt raw status and masked status is cleared.

14 General-Purpose Timers (GPTM0 & GPTM1)

Introduction

The General-Purpose Timer consists of one 16-bit up/down-counter, four 16-bit Capture/ Compare Registers (CCRs), one 16-bit Counter-Reload Register (CRR) and several control/status registers. It can be used for a variety of purposes including general timer, input signal pulse width measurement or output waveform generation such as single pulse generation or PWM output. The GPTM supports an encoder interface using a quadrature decoder with two inputs.

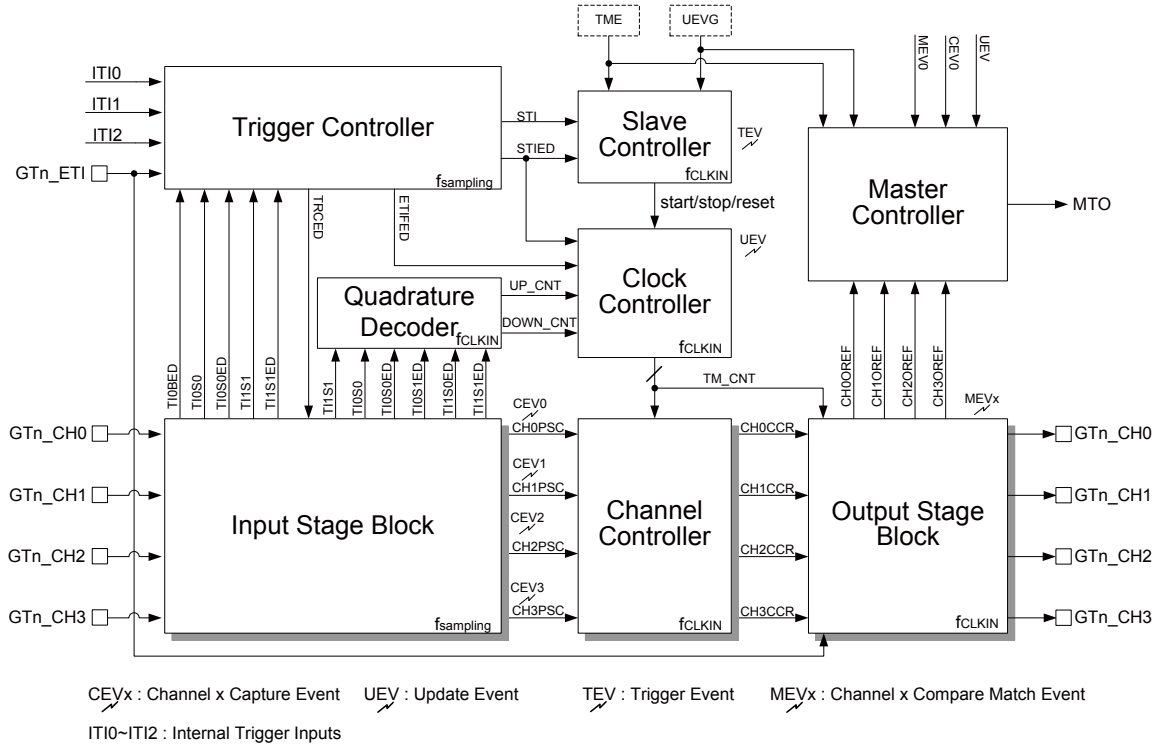


Figure 31. Block Diagram of GPTM

Features

- 16-bit up/down auto-reload counter
- 16-bit programmable prescaler that allows division of the counter clock frequency by any factor between 1 and 65536
- Up to 4 independent channels for:
  - Input Capture function
  - Compare Match Output
  - Generation of PWM waveform - Edge-aligned and Center-aligned Counting Modes
  - Single Pulse Mode Output
- Encoder interface controller with two inputs using quadrature decoder
- Synchronization circuit to control the timer with external signals and to interconnect several timers together
- Interrupt generation with the following events:
  - Update event
  - Trigger event
  - Input capture event
  - Output compare match event
- GPTM Master/Slave mode controller

Functional Descriptions

Counter Modes

Up-counting

In this mode the counter counts continuously from 0 to the counter-reload value, which is defined in the CRR register, in a count-up direction. Once the counter reaches the counter-reload value, the Timer Module generates an overflow event and the counter restarts to count once again from 0. This action will continue repeatedly. The counting direction bit DIR in the CNTCFR register should be set to 0 for the up-counting mode.

When the update event is set by the UEVG bit in the EVGR register, the counter value will be initialized to 0.

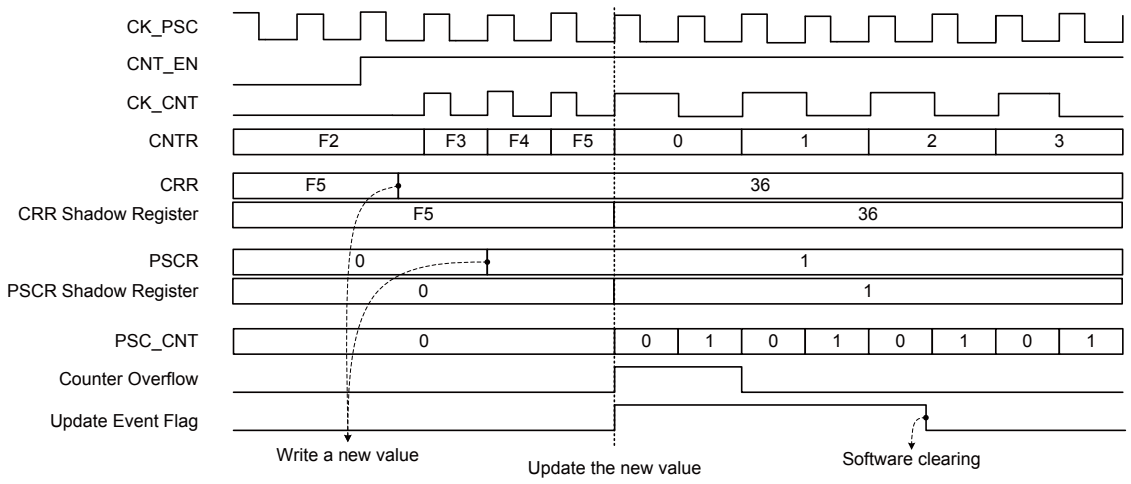


Figure 32. Up-counting Example

Down-counting

In this mode the counter counts continuously from the counter-reload value, which is defined in the CRR register, to 0 in a count-down direction. Once the counter reaches 0, the Timer module generates an underflow event and the counter restarts to count once again from the counter-reload value. This action will continue repeatedly. The counting direction bit DIR in the CNTCFR register should be set to 1 for the down-counting mode.

When the update event is set by the UEVG bit in the EVGR register, the counter value will be initialized to the counter-reload value.

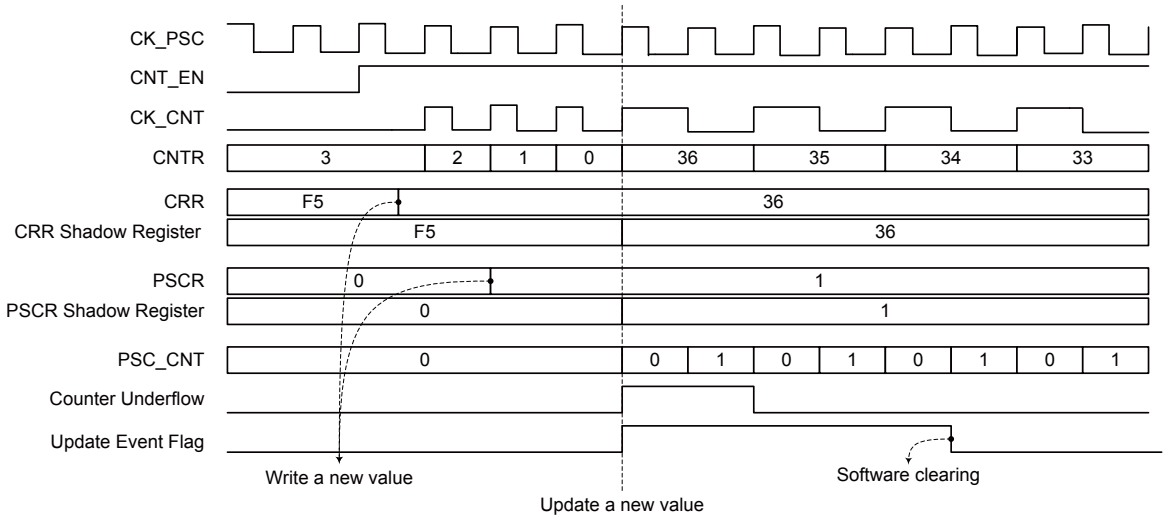


Figure 33. Down-counting Example

Center-aligned Counting

In the center-aligned counting mode, the counter counts up from 0 to the counter-reload value and then counts down to 0 alternatively. The Timer module generates an overflow event when the counter counts to the counter-reload value in the up-counting mode and generates an underflow event when the counter counts to 0 in the down-counting mode. The counting direction bit DIR in the CNTCFR register is read-only and indicates the counting direction when in the center-aligned counting mode. The counting direction is updated by hardware automatically.

Setting the UEVG bit in the EVGR register will initialize the counter value to 0 irrespective of whether the counter is counting up or down in the center-aligned counting mode.

The UEVIF bit in the INTSR register can be set to 1 according to the CMSEL field setting in the CNTCFR register. When CMSEL=0x01, an underflow event will set the UEVIF bit to 1. When CMSEL=0x10, an overflow event will set the UEVIF bit to 1. When CMSEL=0x11, either underflow or overflow event will set the UEVIF bit to 1.

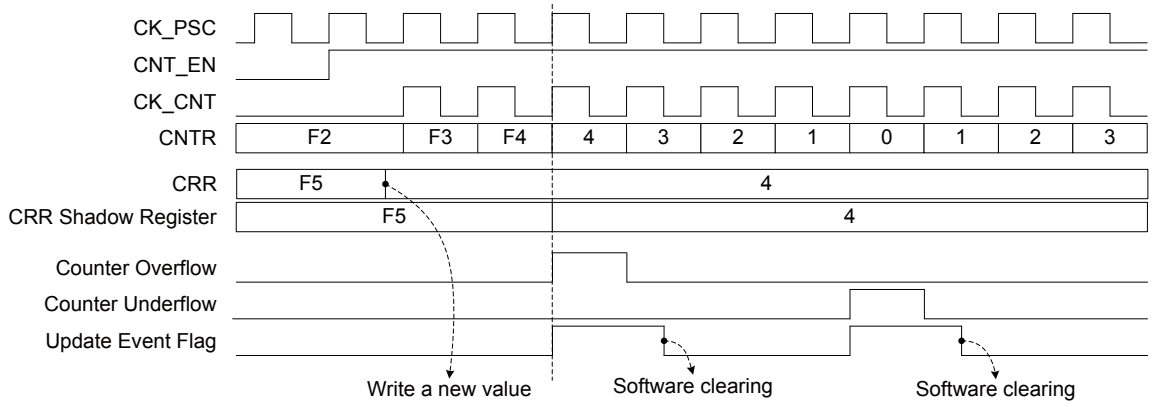


Figure 34. Center-aligned Counting Example

Clock Controller

The following describes the Timer Module clock controller which determines the clock source of the internal prescaler counter.

■ Internal APB clock f_{CLKIN}:

The default internal clock source is the APB clock fCLKIN used to drive the counter prescaler when the slave mode is disabled. When the slave mode selection bits SMSEL are set to 0x4, 0x5 or 0x6, the internal APB clock fCLKIN is the counter prescaler driving clock source.

■ Quadrature Decoder:

To select Quadrature Decoder mode the SMSEL field should be set to 0x1, 0x2 or 0x3 in the MDCFR register. The Quadrature Decoder function uses two input states of the GTn_CH0 and GTn_CH1 pins to generate the clock pulse to drive the counter prescaler. The counting direction bit DIR is modified by hardware automatically at each transition on the input source signal.

■ STIED:

The counter prescaler can count during each rising edge of the STI signal. This mode can be selected by setting the SMSEL field to 0x7 in the MDCFR register; here the counter will act as an event counter. The input event, known as STI here, can be selected by setting the TRSEL field to an available value except the value of 0x0. When the STI signal is selected as the clock source, the internal edge detection circuitry will generate a clock pulse during each STI signal rising edge to drive the counter prescaler. It is important to note that if the TRSEL field is set to 0x0 to select the software UEVG bit as the trigger source, then when the SMSEL field is set to 0x7, the counter will be updated instead of counting.

■ ETIFED:

The counter prescaler can be driven to count during each rising edge ETIF. This mode can be selected by setting the ECME bit in the TRCFR register to 1. The other way to select the ETIF signal as the clock source is to set the SMSEL field to 0x7 and the TRSEL field to 0x3 respectively. When the clock source is selected to come from the ETIF signal, the Trigger Controller including the edge detection circuitry will generate a clock pulse during each ETIF signal rising edge to clock the counter prescaler.

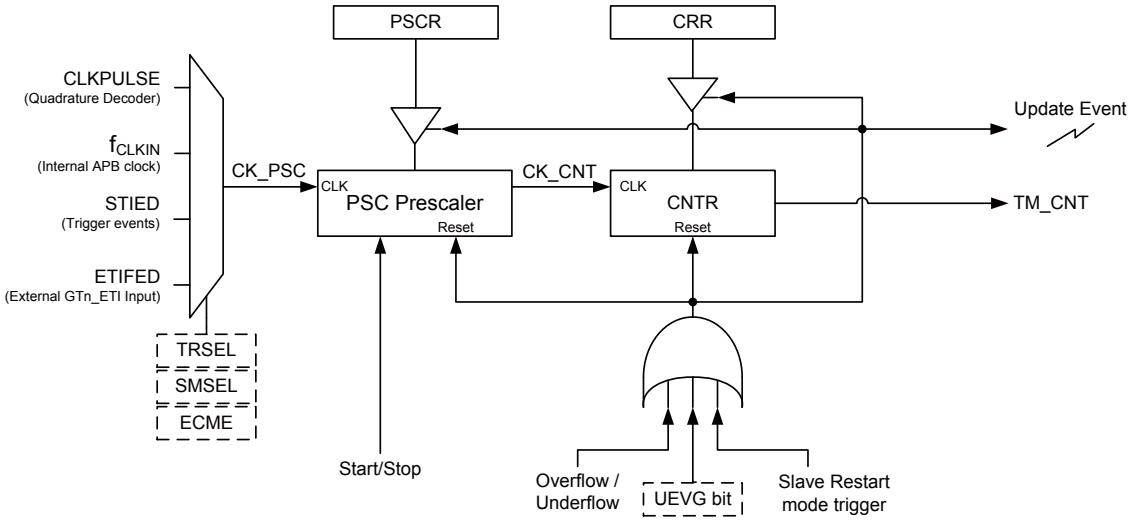


Figure 35. GPTM Clock Selection Source

Trigger Controller

The trigger controller is used to select the trigger source and setup the trigger level or edge trigger condition. The active polarity of the external trigger input signal GTn_ETI can be configured by the External Trigger Polarity control bit ETIPOL in the GPTM Trigger Configuration Register TRCFR. The frequency of the external trigger input can be divided by configuring the related bits, named as External Trigger Prescaler control bits ETIPSC, in the TRCFR register. The trigger signal can also be filtered by configuring the External Trigger Filter ETF selection bits in the TRCFR register if a filtered signal is necessary for specific applications. For the internal trigger input, it can be selected by the Trigger Selection bits TRSEL in the TRCFR register. For all the trigger sources except the UEVG bit software trigger, the internal edge detection circuitry will generate a clock pulse at each trigger signal rising edge to stimulate some GPTM functions which are triggered by a trigger signal rising edge.

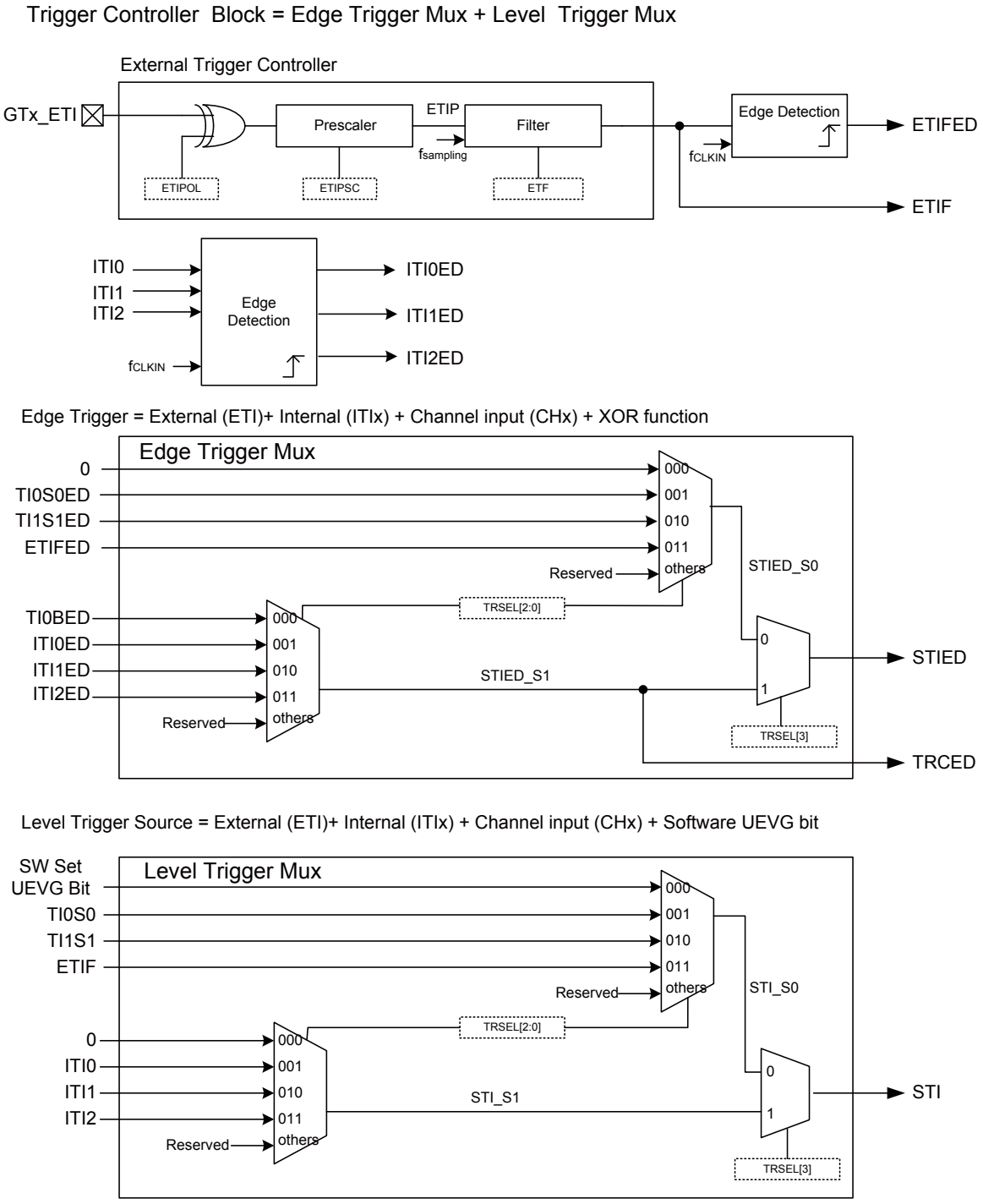


Figure 36. Trigger Control Block

Slave Controller

The GPTM can be synchronized with an internal/external trigger in several modes including the Restart mode, the Pause mode and the Trigger mode which is selected by the SMSEL field in the MDCFR register. The trigger input of these modes comes from the STI signal which is selected by the TRSEL field in the TRCFR register. The operation modes in the Slave Controller are described in the accompanying sections.

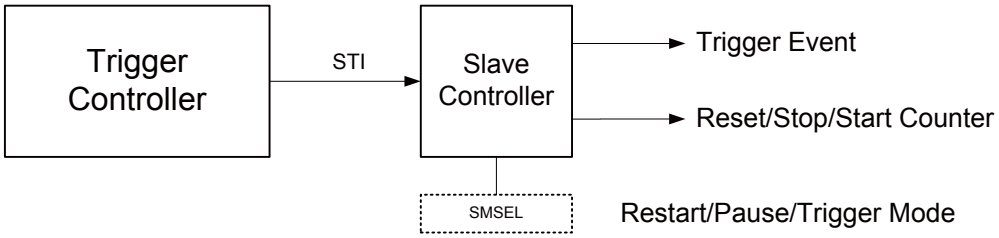


Figure 37. Slave Controller Diagram

Restart Mode

The counter and its prescaler can be reinitialized in response to a rising edge of the STI signal. When a STI rising edge occurs, the update event software generation bit named UEVG will automatically be asserted by hardware and the trigger event flag will also be set. Then the counter and prescaler will be reinitialized. Although the UEVG bit is set to 1 by hardware, the update event does not really occur. It depends upon whether the update event disable control bit UEVDIS is set to 1 or not. If the UEVDIS is set to 1 to disable the update event to occur, no update event will be generated, however the counter and prescaler are still reinitialized when the STI rising edge occurs. If the UEVDIS bit in the CNTCFR register is cleared to enable the update event to occur, an update event will be generated together with the STI rising edge, then all the preloaded registers will be updated.

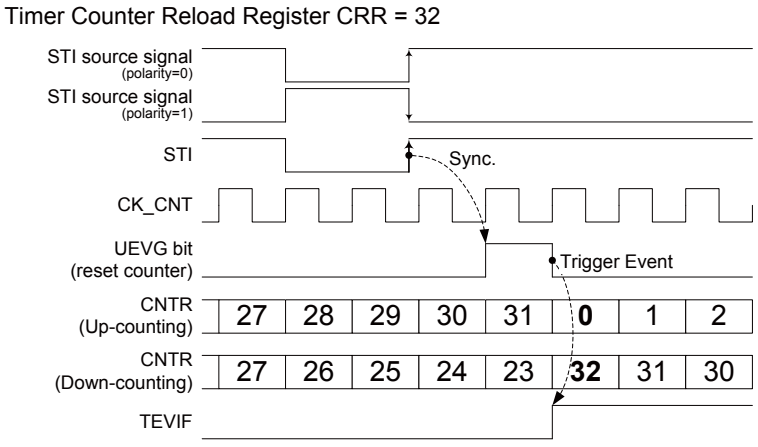


Figure 38. GPTM in Restart Mode

Pause Mode

In the Pause Mode, the selected STI input signal level is used to control the counter start/stop operation. The counter starts to count when the selected STI signal is at a high level and stops counting when the STI signal is changed to a low level, here the counter will maintain its present value and will not be reset. Since the Pause function depends upon the STI level to control the counter stop/start operation, the selected STI trigger signal can not be derived from the TI0BED signal.

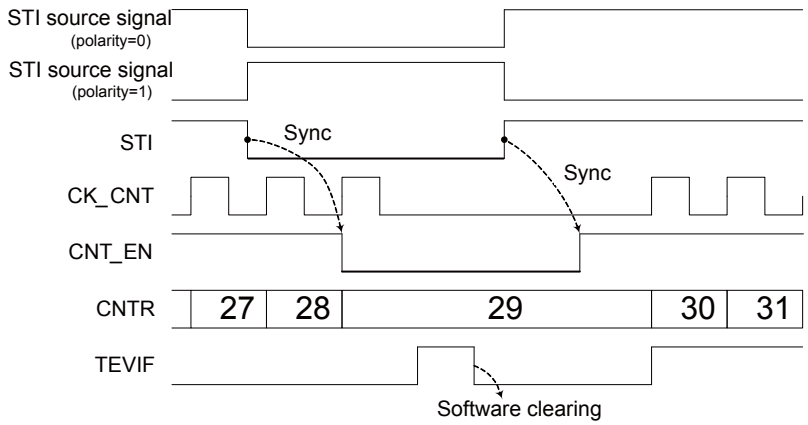


Figure 39. GPTM in Pause Mode

Trigger Mode

After the counter is disabled to count, the counter can resume counting when a STI rising edge signal occurs. When an STI rising edge occurs, the counter will start to count from the current value in the counter. Note that if the STI signal is selected to be derived from the UEVG bit software trigger, the counter will not resume counting. When software triggering using the UEVG bit is selected as the STI source signal, there will be no clock pulse generated which can be used to make the counter resume counting. Note that the STI signal is only used to enable the counter to resume counting and has no effect on controlling the counter to stop counting.

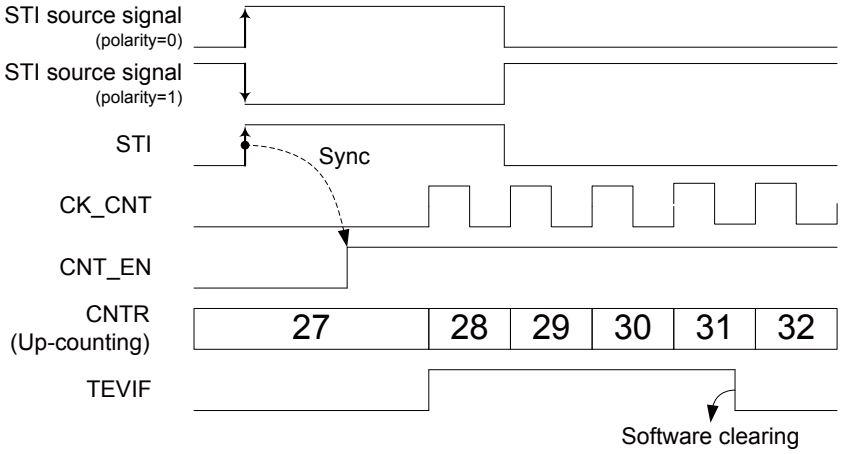


Figure 40. GPTM in Trigger Mode

Master Controller

The GPTMs can be linked together internally for timer synchronization or chaining. When one GPTM is configured to be in the Master Mode, the GPTM Master Controller will generate a Master Trigger Output (MTO) signal which can reset, start, stop the Slave counter or be a clock source of the Slave counter. This can be selected by the MMSEL field in the MDCFR register to trigger or drive another GPTM which is configured in the Slave Mode.

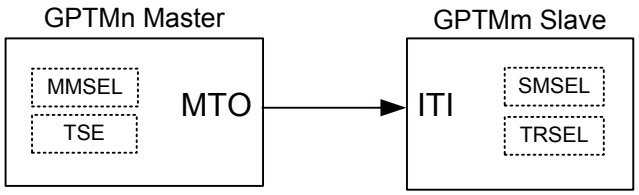


Figure 41. Master GPTMn and Slave GPTMm Connection

The Master Mode Selection bits (MMSEL) in the MDCFR register are used to select the MTO source for synchronizing another slave GPTM.

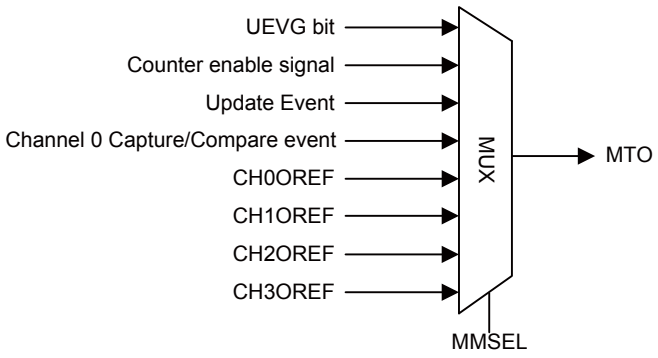


Figure 42. MTO Selection

For example, set the MMSEL field to 0x5 is to select the CH1OREF signal as the MTO signal to synchronize another slave GPTM. For a more detailed description, refer to the related MMSEL field definitions in the MDCFR register.

Channel Controller

The GPTM has four independent channels which can be used as capture inputs or compare match outputs. Each capture input or compare match output channel is composed of a preload register and a shadow register. Data access of the APB bus is always through the read/write preload register.

When used in the input capture mode, the counter value is captured into the CHxCCR shadow register first and then transferred into the CHxCCR preload register when the capture event occurs.

When used in the compare match output mode, the contents of the CHxCCR preload register is copied into the associated shadow register; the counter value is then compared with the register value.

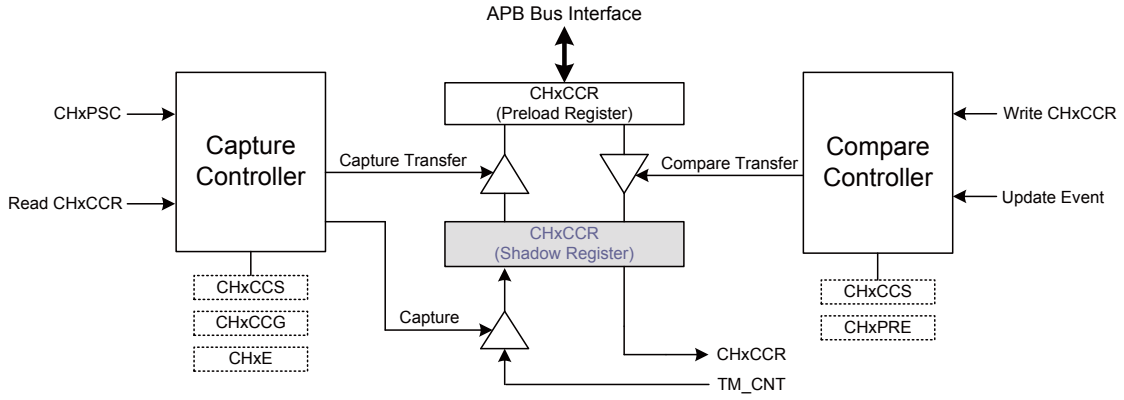


Figure 43. Capture/Compare Block Diagram

Capture Counter Value transfer to CHxCCR

When the channel is used as a capture input, the counter value is captured into the Channel Capture/Compare Register (CHxCCR) when an effective input signal transition occurs. Once the capture event occurs, the CHxCCIF flag in the INTSR register is set accordingly. If the CHxCCIF bit is already set, i.e., the flag has not yet been cleared by software, and another capture event on this channel occurs, the corresponding channel Over-Capture flag, named CHxOCF, will be set.

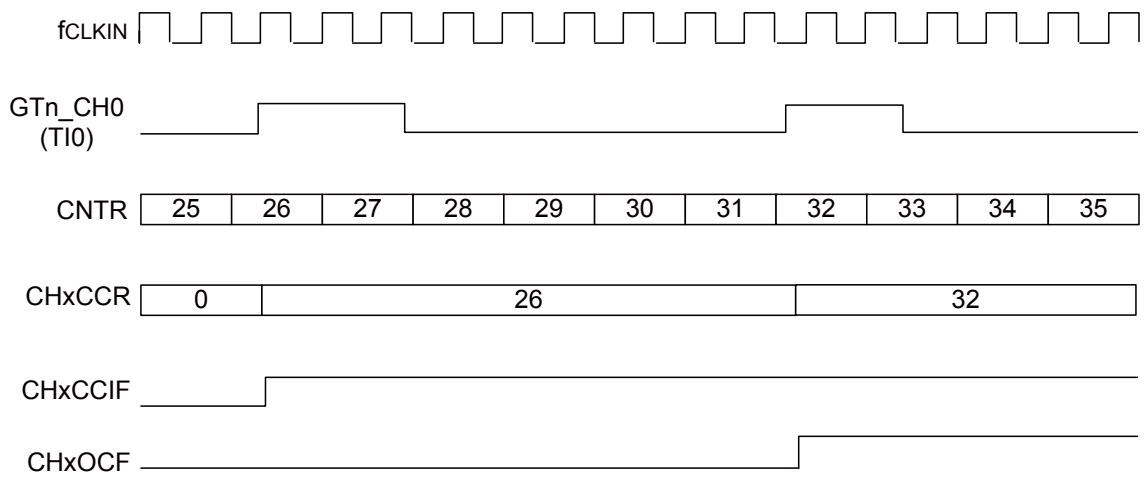


Figure 44. Input Capture Mode

Pulse Width Measurement

The input capture mode can be also used for pulse width measurement from signals on the GTn_CHx pins (TIx). The following example shows how to configure the GPTM operated in the input capture mode to measure the high pulse width and the input period on the GTn_CH0 pin using channel 0 and channel 1. The basic steps are shown as follows.

- Configure the capture channel 0 (CH0CCS = 0x1) to select the TI0 signal as the capture input.
- Configure the CH0P bit to 0 to choose the rising edge of the TI0 input as the active polarity.
- Configure the capture channel 1 (CH1CCS = 0x2) to select the TI0 signal as the capture input.
- Configure the CH1P bit to 1 to choose the falling edge of the TI0 input as the active polarity.
- Configure the TRSEL bits to 0x0001 to select TI0S0 as the trigger input.
- Configure the Slave controller to operate in the Restart mode by setting the SMSEL field in the MDCFR register to 0x4
- Enable the input capture mode by setting the CH0E and CH1E bits in the CHCTR register to 1.

As the following diagram shows, the high pulse width on the GTn_CH0 pin will be captured into the CH1CCR register while the input period will be captured into the CH0CCR register after input capture operation.

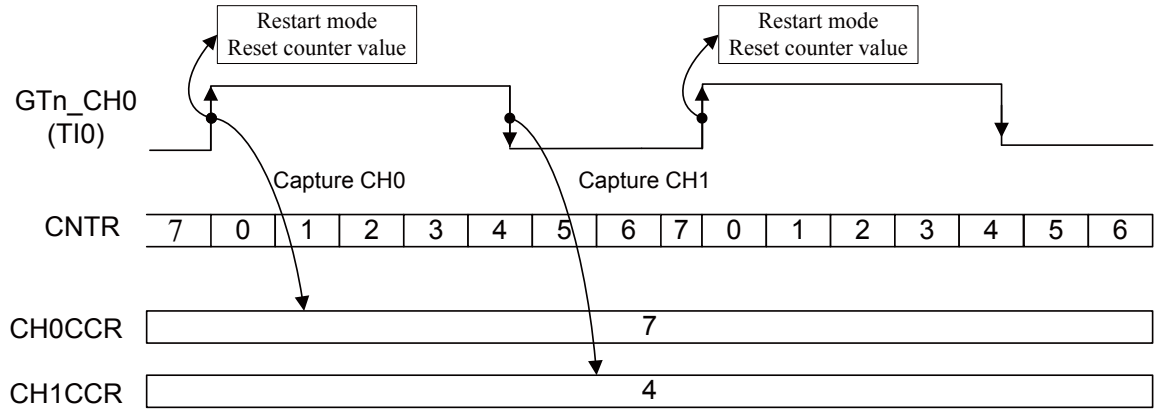


Figure 45. PWM Pulse Width Measurement Example

Input Stage

The input stage consists of a digital filter, a channel polarity selection, edge detection and a channel prescaler. The channel 0 input signal (TI0) can be chosen to come from the GTn_CH0 signal or the Excusive-OR function of the GTn_CH0, GTn_CH1 and GTn_CH2 signals. The channel input signal (TIx) is sampled by a digital filter to generate a filtered input signal TIxFP. Then the channel polarity and the edge detection block can generate a TIxSxED signal for the input capture function. The effective input event number can be set by the channel input prescaler register (CHxPSC).

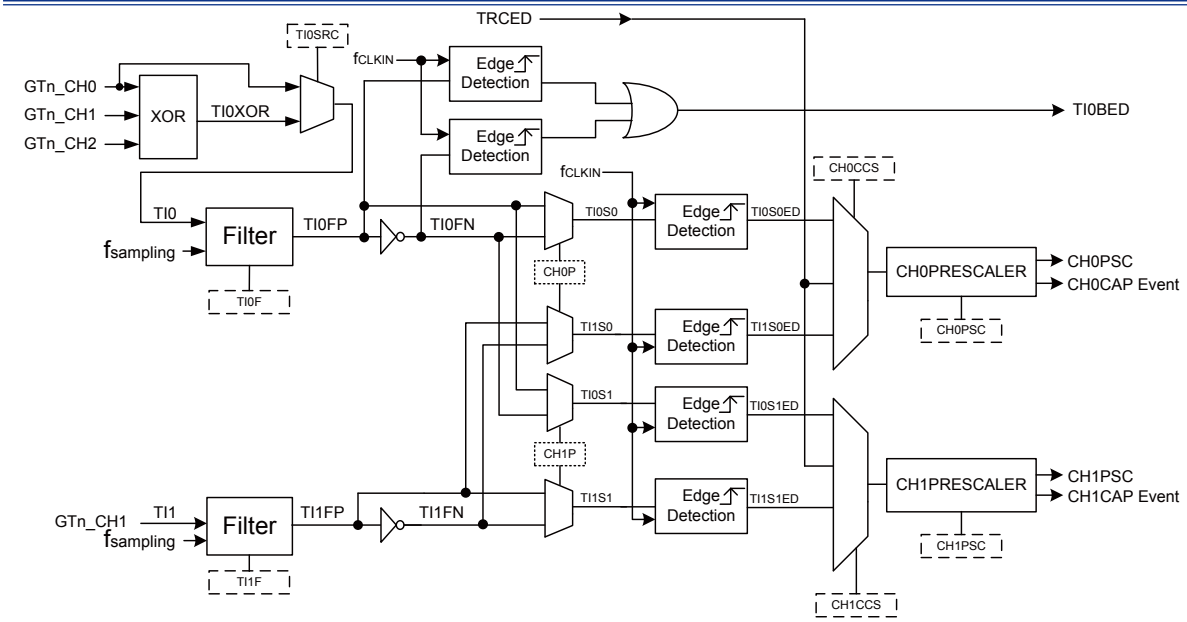


Figure 46. Channel 0 and Channel 1 Input Stage

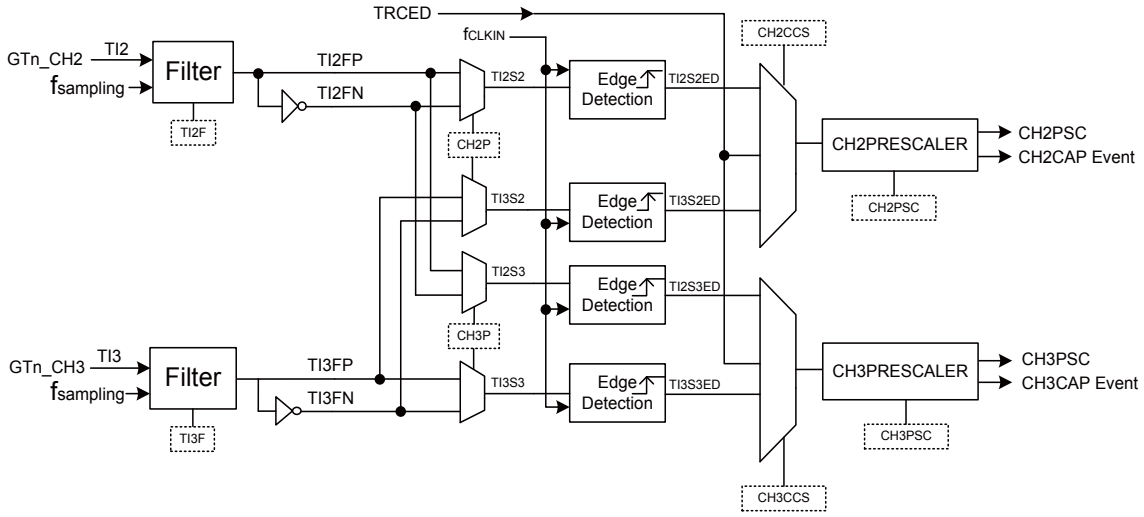


Figure 47. Channel 2 and Channel 3 Input Stage

Output Stage

The GPTM has four channels for compare match, single pulse or PWM output function. The channel output GTn_CHx is controlled by the REFxCE, CHxOM, CHxP and CHxE bits in the corresponding CHxOCFR, CHPOLR and CHCTR registers.

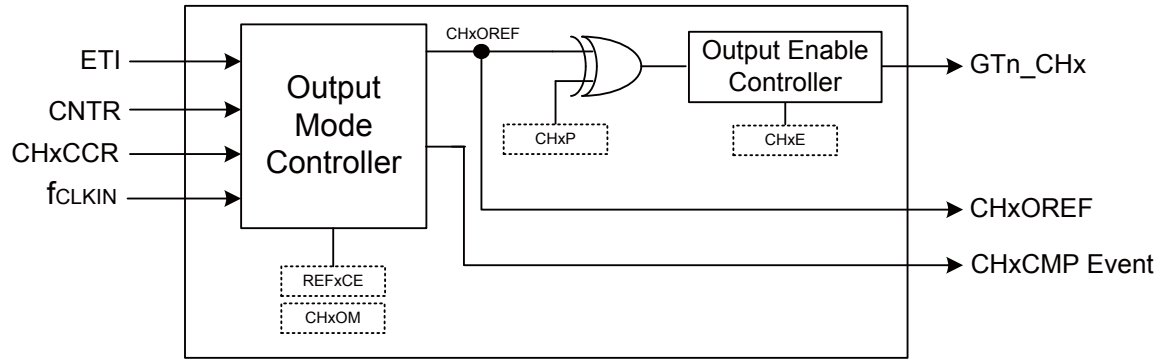


Figure 48. Output Stage Block Diagram

Channel Output Reference Signal

When the GPTM is used in the compare match output mode, the CHxOREF signal (Channel x Output Reference signal) is defined by setting the CHxOM bits. The CHxOREF signal has several types of output function. These include, keeping the original level by setting the CHxOM field to 0x00, set to 0 by setting the CHxOM field to 0x01, set to 1 by setting the CHxOM field to 0x02 or signal toggle by setting the CHxOM field to 0x03 when the counter value matches the content of the CHxCCR register.

The PWM mode 1 and PWM mode 2 outputs are also another kind of CHxOREF output which is setup by setting the CHxOM field to 0x06/0x07. In these modes, the CHxOREF signal level is changed according to the counting direction and the relationship between the counter value and the CHxCCR content. With regard to a more detailed description refer to the relative bits definitions.

Another special function of the CHxOREF signal is a forced output which can be achieved by setting the CHxOM field to 0x04/0x05. Here the output can be forced to an inactive/active level irrespective of the comparison condition between the counter and the CHxCCR values.

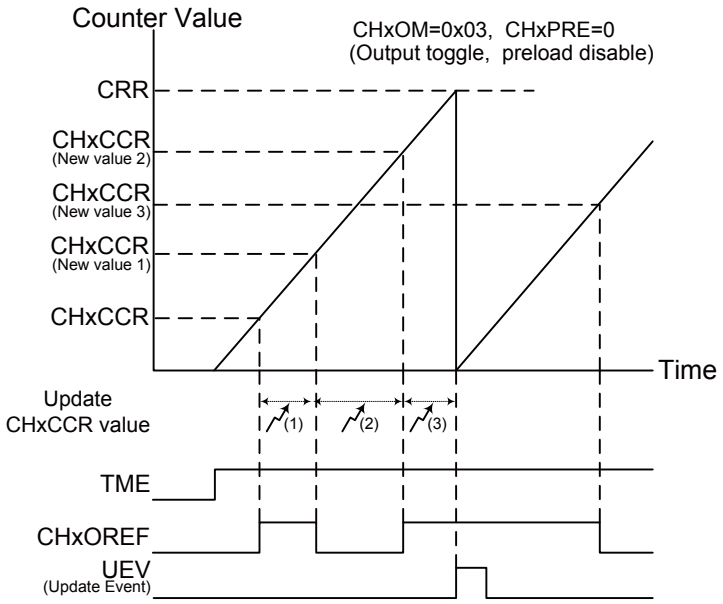


Figure 49. Toggle Mode Channel Output Reference Signal (CHxPRE = 0)

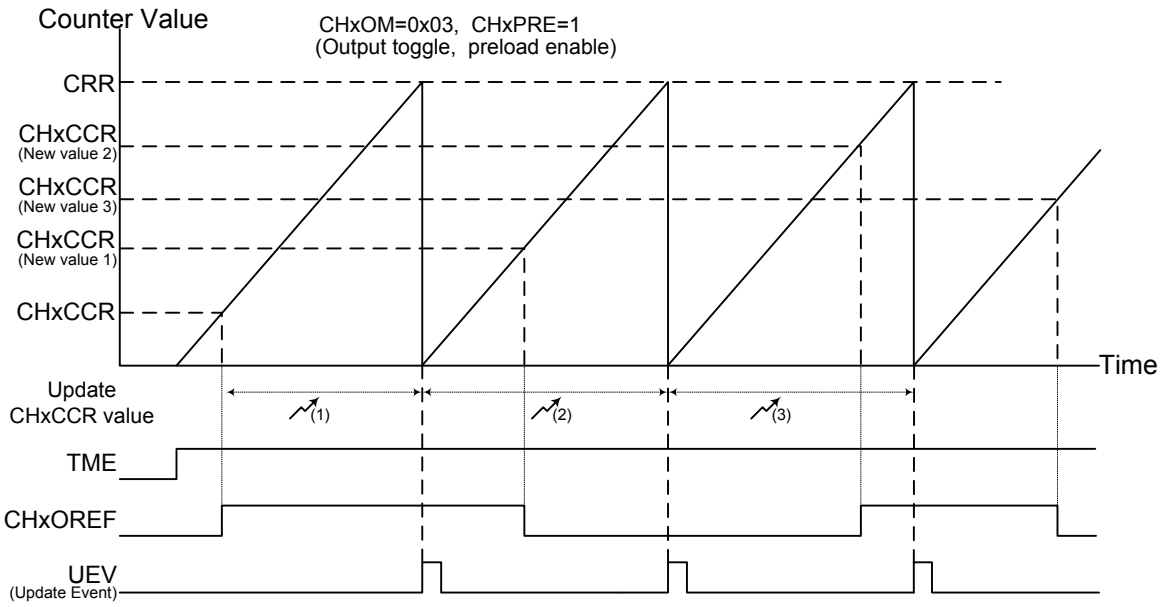


Figure 50. Toggle Mode Channel Output Reference Signal (CHxPRE = 1)

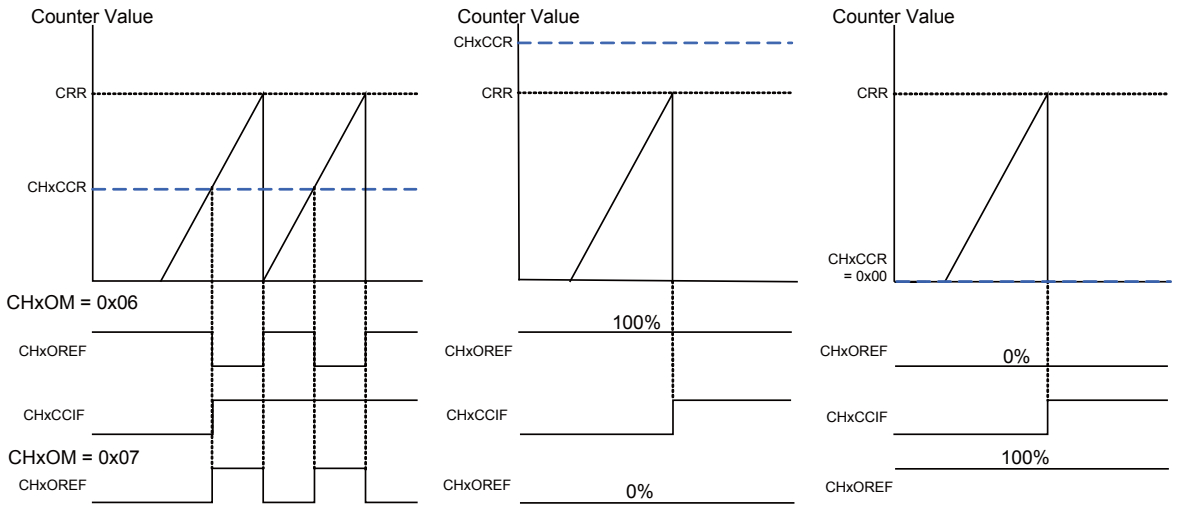


Figure 51. PWM Mode Channel Output Reference Signal and Counter in Up-counting Mode

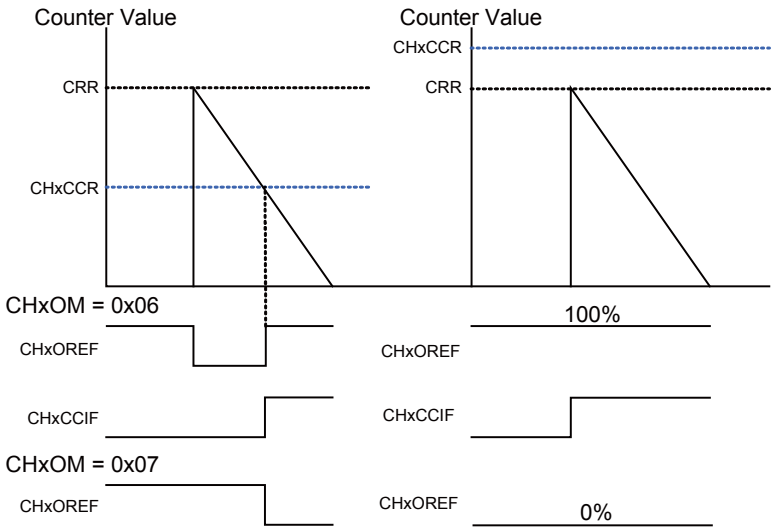


Figure 52. PWM Mode Channel Output Reference Signal and Counter in Down-counting Mode

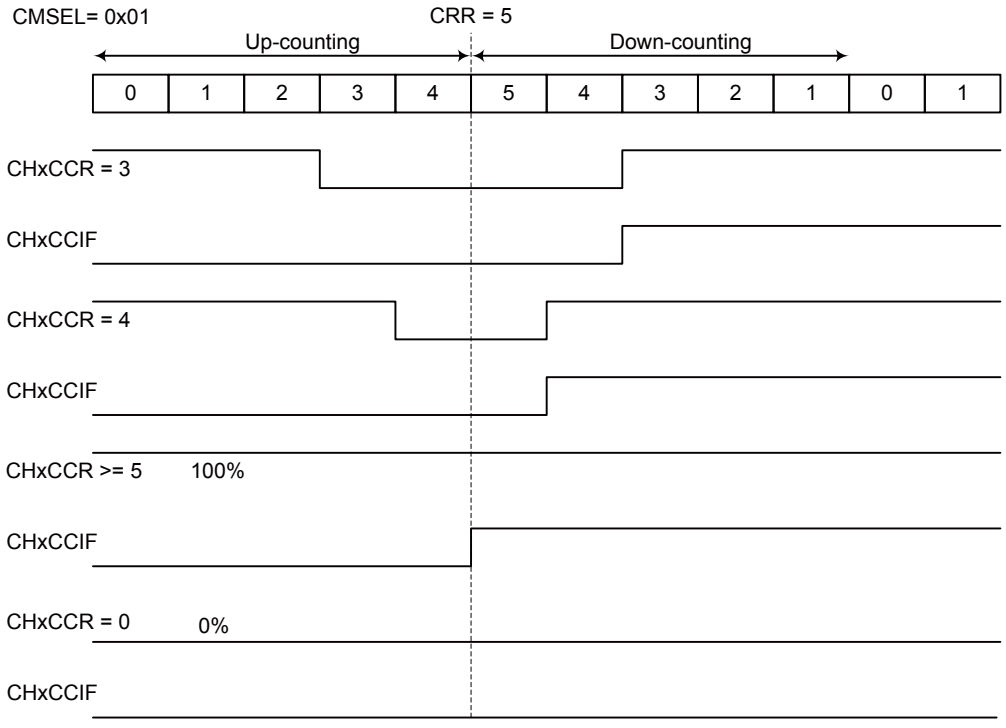


Figure 53. PWM Mode 1 Channel Output Reference Signal and Counter in Center-aligned Counting Mode

Update Management

The Update event is used to update the CRR, the PSCR and the CHxCCR values from the actual registers to the corresponding shadow registers. An update event is generated when counter overflow/underflow or by the software trigger and slave controller.

The UEVDIS bit in the CNTCFR register can determine whether the update event occurs or not. When the update event occurs, the corresponding update event interrupt will be generated depending upon whether the update event interrupt generation function is enabled or not by configuring the UGDIS bit in the CNTCFR register. For more detail description, refer to the UEVDIS and UGDIS bit definition in the CNTCFR register.

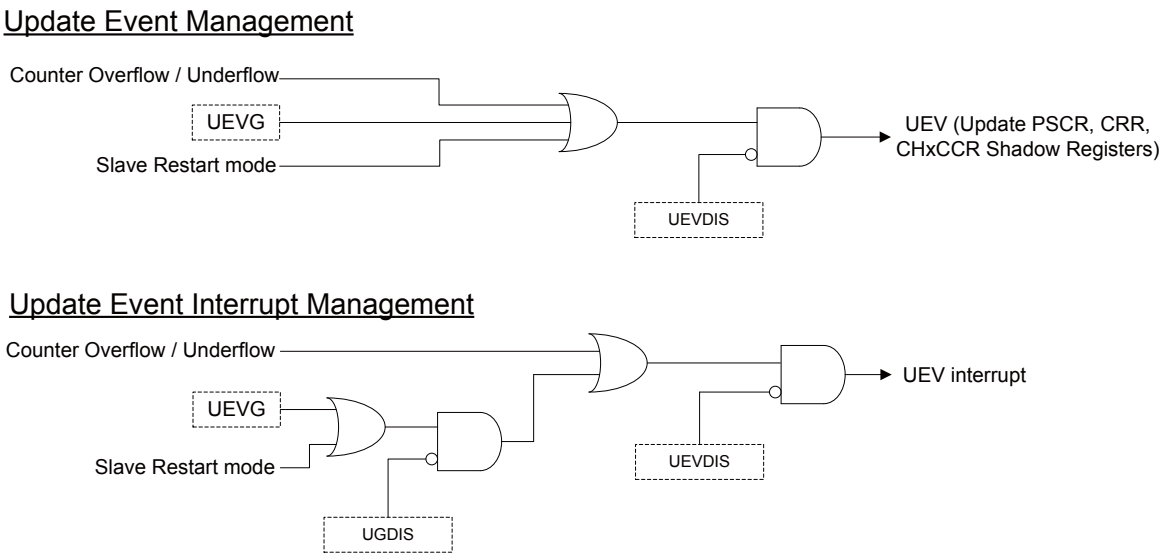


Figure 54. Update Event setting Diagram

Quadrature Decoder

The Quadrature Decoder function uses two quadrantal inputs TI0 and TI1 derived from the GTx_CH0 and GTx_CH1 pins respectively to interact to generate the counter value. The DIR bit is modified by hardware automatically during each input source transition. The counter is countering on TI0 edges only, TI1 edges only or both TI0 and TI1 edges. The selection is made by setting the SMSEL field to 0x01, 0x02 or 0x03. The mechanism for changing the counter direction is shown in the following table. The Quadrature decoder can be regarded as an external clock with a directional selection. This means that the counter counts continuously in the interval between 0 and the counter-reload value. Therefore, users must configure the CRR register before the counter starts to count.

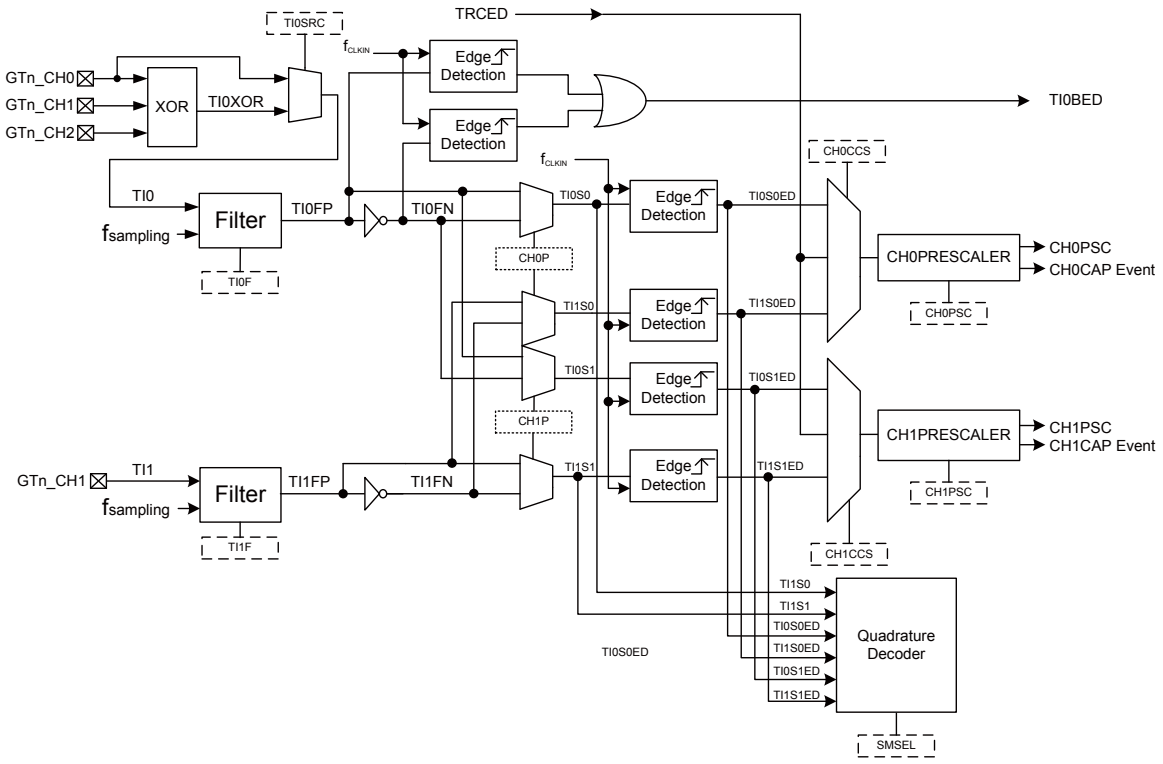


Figure 55. Input Stage and Quadrature Decoder Block Diagram

Table 29. Counting Direction and Encoding Signals

Counting mode	Level	TI0S0		TI0S1	
		Rising	Falling	Rising	Falling
Counting on TI0 only (SMSEL = 0x01)	TI1S1 = High	Down	Up	—	—
	TI1S1 = Low	Up	Down	—	—
Counting on TI1 only (SMSEL = 0x02)	TI0S0 = High	—	—	Up	Down
	TI0S0 = Low	—	—	Down	Up
Counting on TI0 and TI1 (SMSEL = 0x03)	TI1S1 = High	Down	Up	X	X
	TI1S1 = Low	Up	Down	X	X
	TI0S0 = High	X	X	Up	Down
	TI0S0 = Low	X	X	Down	Up

NOTE: "—" → means "no counting"; " X " → impossible

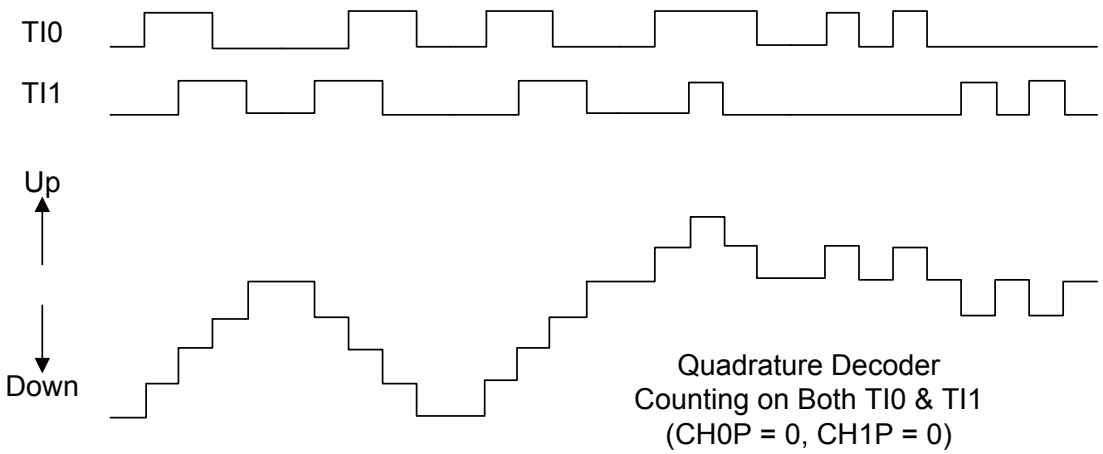


Figure 56. Both TI0 and TI1 Quadrature Decoder Counting

Digital Filter

The digital filters are embedded in the input stage and clock controller block for the GTn_CH0 ~ GTn_CH3 and GTn_ETI pins respectively. The digital filter in the GPTM is an N-event counter where N refers to how many valid transitions are necessary to output a filtered signal. The N value can be 0, 2, 4, 5, 6 or 8 according to the user selection for each filter.

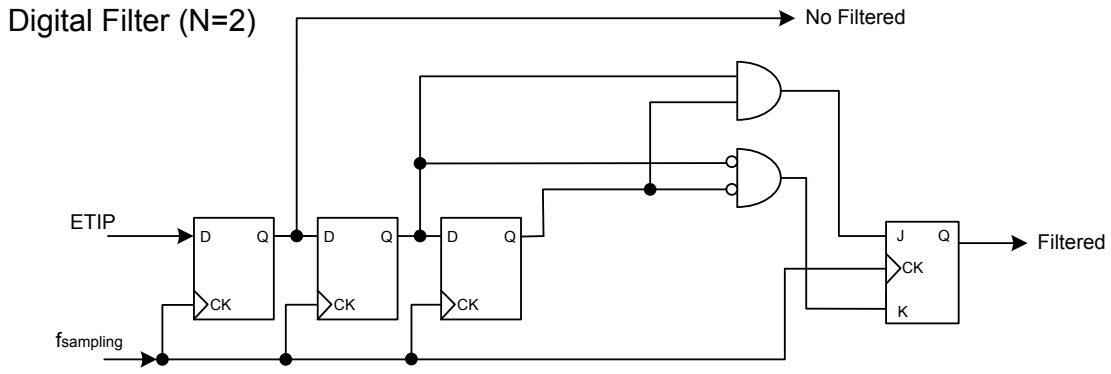


Figure 57. GTn_ETI Pin Digital Filter Diagram with N = 2

Clearing CHxOREF when ETIF is high

The CHxOREF signal can be forced to 0 when the ETIF signal is set to a high level by setting the REFxCE bit to 1 in the CHxOCFR register. The CHxOREF signal will not return to its active level until the next update event occurs.

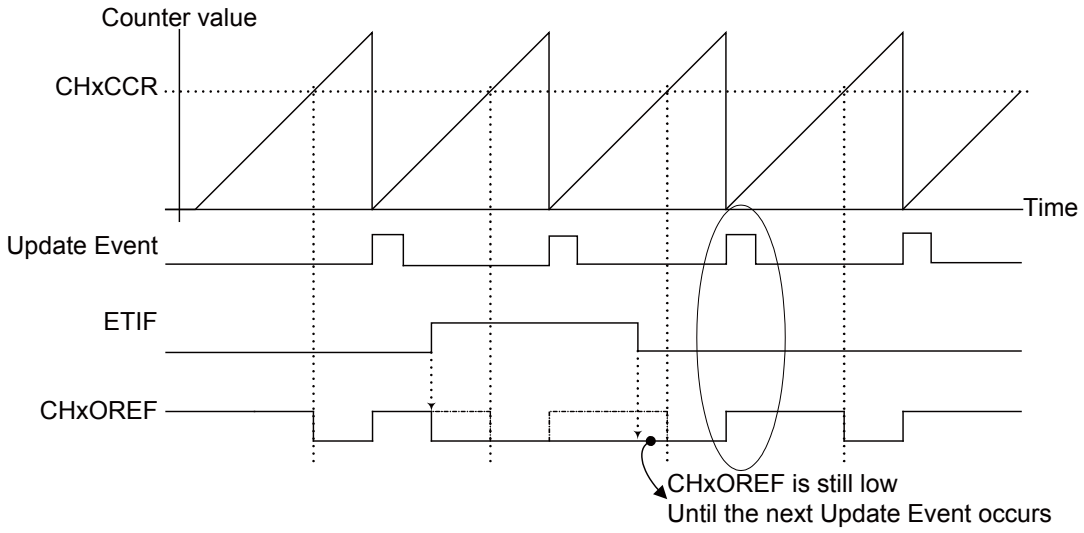


Figure 58. Clearing CHxOREF by ETIF

Single Pulse Mode

Once the timer is set to operate in the single pulse mode, it is not necessary to set the timer enable bit TME in the CTR register to 1 to enable the counter. The trigger to generate a pulse can be sourced from the STI signal rising edge or by setting the TME bit to 1 using software. Setting the TME bit to 1 or a trigger from the STI signal rising edge can generate a pulse and then keep the TME bit at a high state until the update event occurs or the TME bit is written to 0 by software. If the TME bit is cleared to 0 using software, the counter will be stopped and its value held. If the TME bit is automatically cleared to 0 by a hardware update event, the counter will be reinitialized.

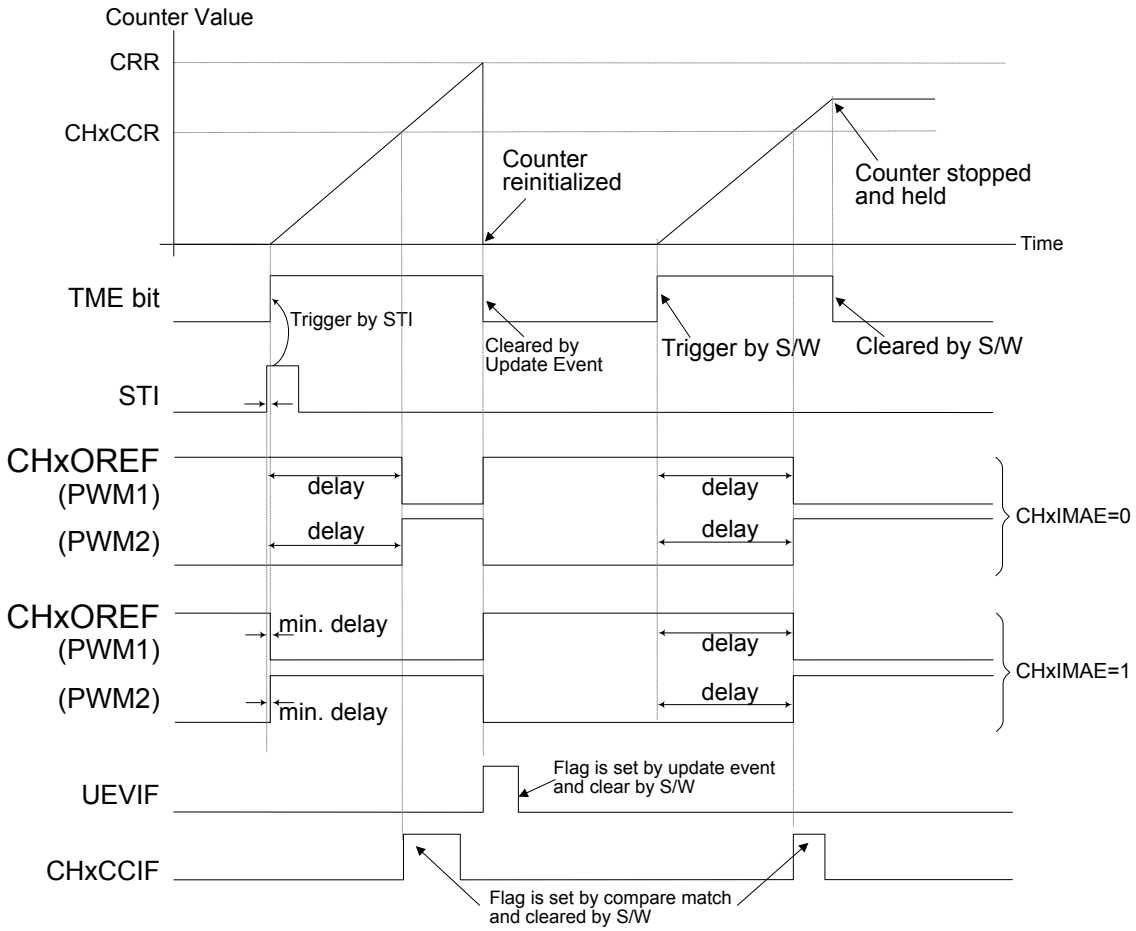


Figure 59. Single Pulse Mode

In the Single Pulse mode, the STI active edge which sets the TME bit to 1 will enable the counter. However, there exist several clock delays to perform the comparison result between the counter value and the CHxCCR value. In order to reduce the delay to a minimum value, the user can set the CHxIMAE bit in each CHxOCFR register. After a STI rising edge trigger occurs in the single pulse mode, the CHxOREF signal will immediately be forced to the state which the CHxOREF signal will change to as the compare match event occurs without taking the comparison result into account. The CHxIMAE bit is available only when the output channel is configured to operate in the PWM1 or PWM2 output mode and the trigger source is derived from the STI signal.

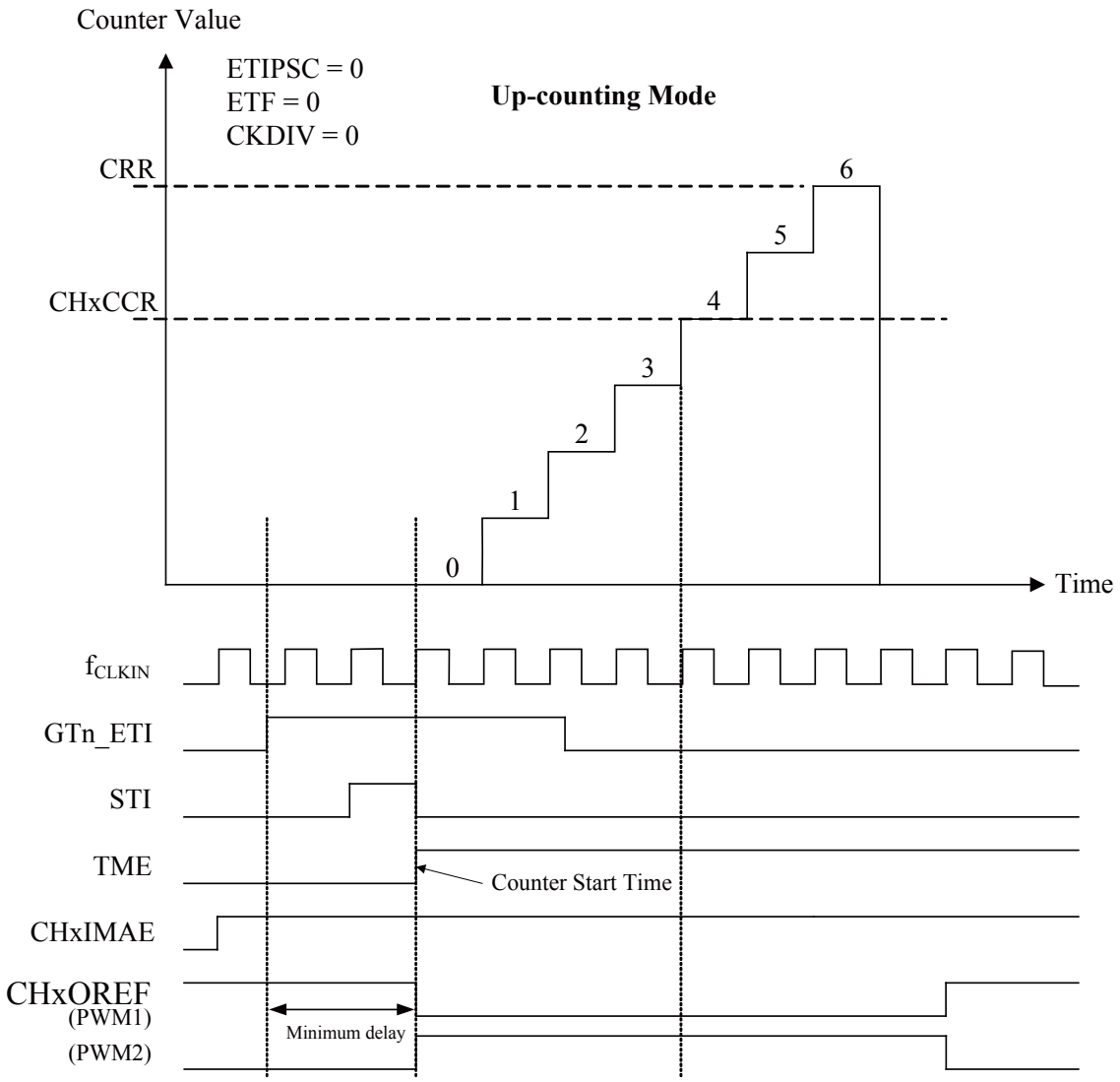


Figure 60. Immediate Active Mode Minimum Delay

Timer Interconnection

The timers can be internally connected together for timer chaining or synchronization. This can be implemented by configuring one timer to operate in the Master mode while configuring another timer to be in the Slave mode. The following figures present several examples of trigger selection for the master and slave modes.

Using one timer to trigger another timer start or stop counting

- Configure GPTM0 as the master mode to send its channel 0 Output Reference signal CH0OREF as a trigger output (MMSEL = 0x04).
- Configure GPTM0 CH0OREF waveform.
- Configure GPTM1 to receive its input trigger source from the GPTM0 trigger output (TRSEL = 0x09).
- Configure GPTM1 to operate in the pause mode (SMSEL = 0x05).
- Enable GPTM1 by writing 1 to the TME bit.
- Enable GPTM0 by writing 1 to the TME bit.

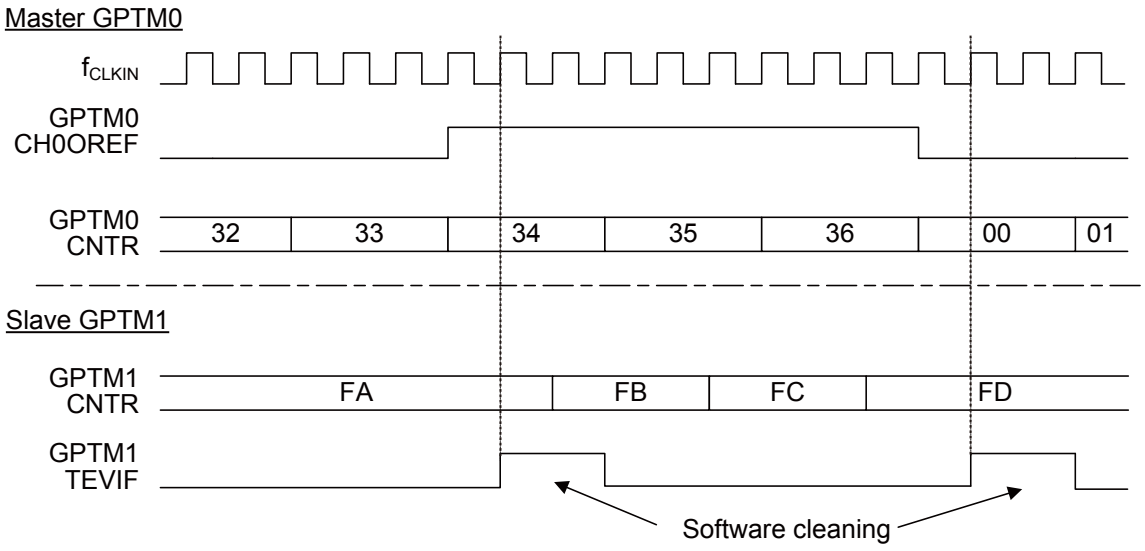


Figure 61. Pausing GPTM1 using the GPTM0 CH0OREF Signal

Using one timer to trigger another timer start counting

- Configure GPTM0 to operate in the master mode to send its Update Event UEV as the trigger output (MMSEL = 0x02).
- Configure the GPTM0 period by setting the CHxCRR register.
- Configure GPTM1 to get the input trigger source from the GPTM0 trigger output (TRSEL = 0x09).
- Configure GPTM1 to be in the slave trigger mode (SMSEL = 0x06).
- Start GPTM0 by writing 1 to the TME bit.

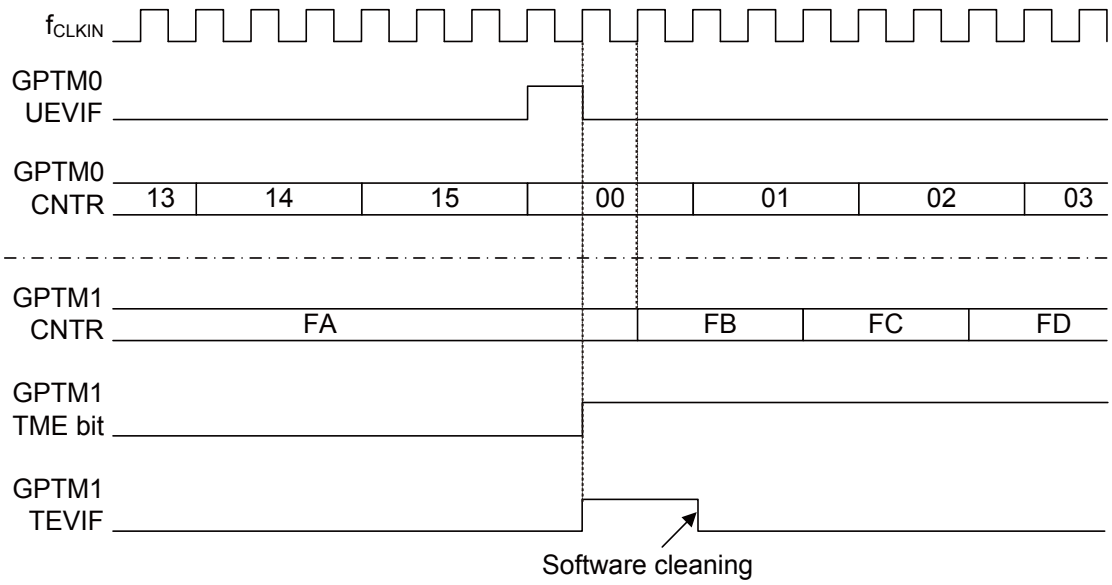


Figure 62. Triggering GPTM1 with GPTM0 Update Event

Starting two timers synchronously in response to an external trigger

- Configure GPTM0 to operate in the master mode to send its enable signal as a trigger output (MMSEL = 0x01).
- Configure GPTM0 slave mode to receive its input trigger source from GTn_CH0 pin (TRSEL = 0x01).
- Configure GPTM0 to be in the slave trigger mode (SMSEL = 0x06).
- Enable the GPTM0 master timer synchronization function by setting the TSE bit in the MDCFR register to 1 to synchronize the slave timer.
- Configure GPTM1 to receive its input trigger source from the GPTM0 trigger output (TRSEL = 0x09).
- Configure GPTM1 to be in the slave trigger mode (SMSEL = 0x06).

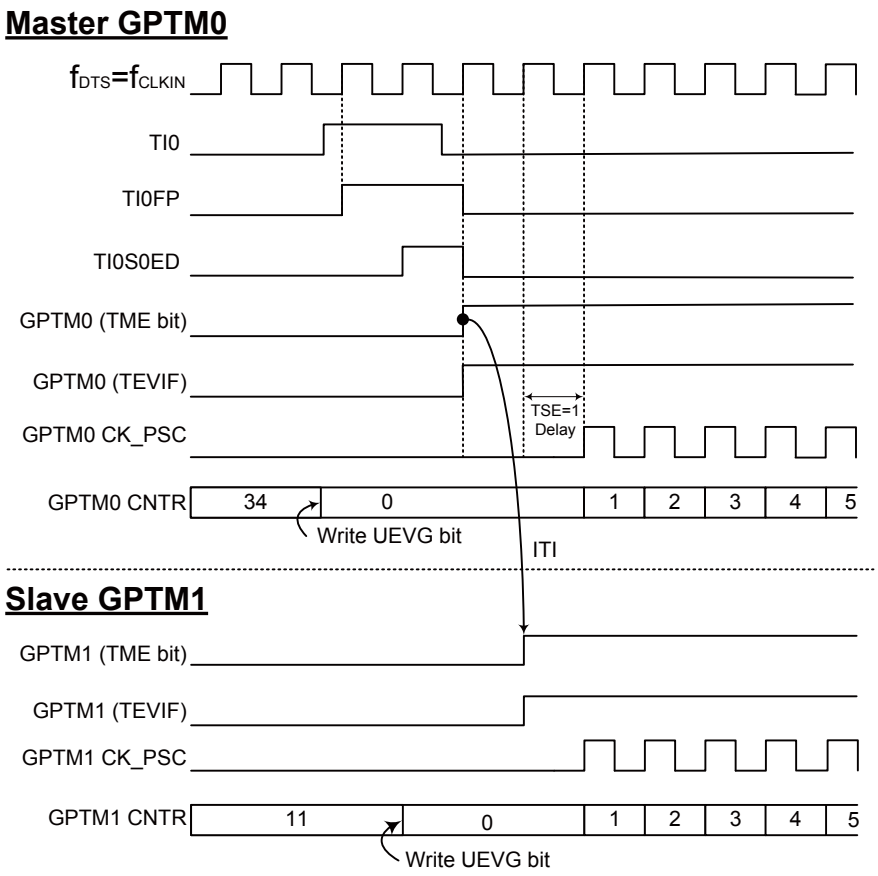


Figure 63. Trigger GPTM0 and GPTM1 with the GPTM0 CH0 Input

Trigger ADC Start

To interconnect with the Analog-to-Digital Converter, the GPTM can output the MTO signal or the channel output GTn_CHx (x = 0 ~ 3) signal to be used as the Analog-to-Digital Converter input trigger signal.

Register Map

The following table shows the GPTM registers and reset values.

Table 30. Register map of GPTM

Register	Offset	Description	Reset Value
GPTMn Base Address = 0x4006_E000 (0); 0x4006_F000 (1)			
CNTCFR	0x000	Timer Counter Configuration Register	0x0000_0000
MDCFR	0x004	Timer Mode Configuration Register	0x0000_0000
TRCFR	0x008	Timer Trigger Configuration Register	0x0000_0000
CTR	0x010	Timer Control Register	0x0000_0000
CH0ICFR	0x020	Channel 0 Input Configuration Register	0x0000_0000
CH1ICFR	0x024	Channel 1 Input Configuration Register	0x0000_0000
CH2ICFR	0x028	Channel 2 Input Configuration Register	0x0000_0000
CH3ICFR	0x02C	Channel 3 Input Configuration Register	0x0000_0000
CH0OCFR	0x040	Channel 0 Output Configuration Register	0x0000_0000
CH1OCFR	0x044	Channel 1 Output Configuration Register	0x0000_0000
CH2OCFR	0x048	Channel 2 Output Configuration Register	0x0000_0000
CH3OCFR	0x04C	Channel 3 Output Configuration Register	0x0000_0000
CHCTR	0x050	Channel Control Register	0x0000_0000
CHPOLR	0x054	Channel Polarity Configuration Register	0x0000_0000
EVGR	0x078	Timer Event Generator Register	0x0000_0000
INTSR	0x07C	Timer Interrupt Status Register	0x0000_0000
CNTR	0x080	Timer Counter Register	0x0000_0000
PSCR	0x084	Timer Prescaler Register	0x0000_0000
CRR	0x088	Timer Counter Reload Register	0x0000_FFFF
CH0CCR	0x090	Channel 0 Capture/Compare Register	0x0000_0000
CH1CCR	0x094	Channel 1 Capture/Compare Register	0x0000_0000
CH2CCR	0x098	Channel 2 Capture/Compare Register	0x0000_0000
CH3CCR	0x09C	Channel 3 Capture/Compare Register	0x0000_0000

Register Descriptions

Timer Counter Configuration Register (CNTCFR)

This register specifies the GPTM counter configuration.

Offset: 0x000

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							DIR
Type/Reset								RW 0
	23	22	21	20	19	18	17	16
	Reserved							CMSEL
Type/Reset							RW 0	RW 0
	15	14	13	12	11	10	9	8
	Reserved							CKDIV
Type/Reset							RW 0	RW 0
	7	6	5	4	3	2	1	0
	Reserved						UGDIS	UEVDIS
Type/Reset							RW 0	RW 0

Bits	Field	Descriptions
[24]	DIR	Counting Direction 0: Up-counting 1: Down-counting **NOTE:** This bit is read only when the Timer is configured to be in the center-aligned counting mode or when used as a Quadrature decoder
[17:16]	CMSEL	Counter Mode Selection 00: Edge-aligned counting. Normal up-counting and down-counting available for this mode. Counting direction is defined by the DIR bit. 01: Center-aligned counting mode 1. The counter counts up and down alternatively. The compare match interrupt flag is set during the down-counting period. 10: Center-aligned counting mode 2. The counter counts up and down alternatively. The compare match interrupt flag is set during the up-counting period. 11: Center-aligned counting mode 3. The counter counts up and down alternatively. The compare match interrupt flag is set during the up-counting or down-counting period.
[9:8]	CKDIV	Clock Division These two bits define the frequency ratio between the timer clock (f_{CLKIN}) and the digital filter clock (f_D). The f_D clock is also used for digital filter sampling clock. 00: $f_D = f_{CLKIN}$ 01: $f_D = f_{CLKIN} / 2$ 10: $f_D = f_{CLKIN} / 4$ 11: Reserved
[1]	UGDIS	Update event interrupt generation disable control 0: Any of the following events will generate an update event interrupt - Counter overflow/underflow - Setting the UEVG bit - Update generation through the slave mode 1: Only counter overflow/underflow generates an interrupt

Bits	Field	Descriptions
[0]	UEVDIS	Update event Disable control 0: Enable the update request event by one of following events: - Counter overflow/underflow - Setting the UEVG bit - Update generation through the slave mode 1: Disable the update event (However the counter and the prescaler are reinitialized if the UEVG bit is set or if a hardware restart is received from the slave mode)

Timer Mode Configuration Register (MDCFR)

This register specifies the GPTM master and slave mode selection and single pulse mode.

Offset: 0x004

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							SPMSET
Type/Reset								RW 0
	23	22	21	20	19	18	17	16
	Reserved					MMSEL		
Type/Reset						RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
	Reserved					SMSEL		
Type/Reset						RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	Reserved							TSE
Type/Reset								RW 0

Bits	Field	Descriptions
[24]	SPMSET	Single Pulse Mode Setting 0: Counter counts normally irrespective of whether the update event occurred or not 1: Counter stops counting at the next update event and then the TME bit is cleared by hardware.

Bits	Field	Descriptions
[18:16]	MMSEL	Master Mode Selection Master mode selection is used to select the MTO signal source which is used to synchronize the other slave timer.

MMSEL [2:0]	Mode	Descriptions
000	Reset Mode	The MTO in the Reset mode is an output derived from one of the following cases: 1. Software setting UEVG bit 2. Slave has trigger input when used in slave restart mode
001	Enable Mode	The Counter Enable signal is used as the trigger output.
010	Update Mode	The update event is used as the trigger output according to one of the following cases when the UEVDIS bit is cleared to 0: 1. Counter overflow / underflow 2. Software setting UEVG 3. Slave has trigger input when used in slave Restart mode
011	Capture/Compare Mode	When a Channel 0 capture or compare match event occurs, it will generate a positive pulse used as the master trigger output.
100	Compare output 0	The Channel 0 Output reference signal named CH0OREF is used as the trigger output.
101	Compare output 1	The Channel 1 Output reference signal named CH1OREF is used as the trigger output.
110	Compare output 2	The Channel 2 Output reference signal named CH2OREF is used as the trigger output.
111	Compare output 3	Channel 3 Output reference signal named CH3OREF is used as the trigger output.

Bits	Field	Descriptions
[10:8]	SMSEL	Slave Mode Selection

SMSEL [2:0]	Mode	Descriptions
000	Disable mode	The prescaler is clocked directly by the internal clock.
001	Quadrature Decoder mode 1	The counter uses the clock pulse generated from the interact between the TI0 and TI1 signals to drive the counter prescaler. A transition of the TI0 edge is used in this mode depending upon the TI1 level.
010	Quadrature Decoder mode 2	The counter uses the clock pulse generated from the interaction between the TI0 and TI1 signals to drive the counter prescaler. A transition of the TI1 edge is used in this mode depending upon the TI0 level.
011	Quadrature Decoder mode 3	The counter uses the clock pulse generated from the interaction between the TI0 and TI1 signals to drive the counter prescaler. A transition of one channel edge is used in the quadrature decoder mode 3 depending upon the other channel level.
100	Restart Mode	The counter value restarts from 0 or the CRR shadow register value depending upon the counting direction mode on the rising edge of the STI signal. The registers will also be updated.
101	Pause Mode	The counter starts to count when the selected trigger input STI is high. The counter stops counting on the instant, not being reset, when the STI signal changes its state to a low level. Both the counter start and stop control are determined by the STI signal.
110	Trigger Mode	The counter starts to count from the original value in the counter on the rising edge of the selected trigger input STI. Only the counter start control is determined by the STI signal.
111	STIED	The rising edge of the selected trigger signal STI will clock the counter.

[0]	TSE	Timer Synchronization Enable 0: No action 1: Master timer (current timer) will generate a delay to synchronize its slave timer through the MTO signal.

Timer Trigger Configuration Register (TRCFR)

This register specifies the GPTM external clock setting and the trigger source selection.

Offset: 0x008

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							ECME
Type/Reset								RW 0
	23	22	21	20	19	18	17	16
	Reserved							ETIPOL
Type/Reset								RW 0
	15	14	13	12	11	10	9	8
	Reserved		ETIPSC		ETF			
Type/Reset			RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	Reserved				TRSEL			
Type/Reset					RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[24]	ECME	External Clock Mode Enable 0: External clock mode disabled 1: External clock mode enabled The following two settings have the same effect: 1. Setting the ECME bit to 1. 2. Setting SMSEL=0x111 with STI connected to ETIF (TRSEL=0x011)
[16]	ETIPOL	External Trigger Polarity 0: GTn_ETI active at high level or rising edge 1: GTn_ETI active at low level or falling edge
[13:12]	ETIPSC	External Trigger Prescaler A prescaler can be enabled to reduce the ETIP frequency. 00: Prescaler OFF 01: ETIP frequency divided by 2 10: ETIP frequency divided by 4 11: ETIP frequency divided by 8

Bits	Field	Descriptions
[11:8]	ETF	External Trigger Filter These bits define the frequency divided ratio that is used to sample the GTn_ETI signal. The digital filter in the GPTM is an N-event counter where N means how many valid transitions are necessary to output a filtered signal. 0000: No filter, the sampling clock is f_D 0001: $f_{SAMPLING} = f_{CLKIN}$, N = 2 0010: $f_{SAMPLING} = f_{CLKIN}$, N = 4 0011: $f_{SAMPLING} = f_{CLKIN}$, N = 8 0100: $f_{SAMPLING} = f_D / 2$, N = 6 0101: $f_{SAMPLING} = f_D / 2$, N = 8 0110: $f_{SAMPLING} = f_D / 4$, N = 6 0111: $f_{SAMPLING} = f_D / 4$, N = 8 1000: $f_{SAMPLING} = f_D / 8$, N = 6 1001: $f_{SAMPLING} = f_D / 8$, N = 8 1010: $f_{SAMPLING} = f_D / 16$, N = 5 1011: $f_{SAMPLING} = f_D / 16$, N = 6 1100: $f_{SAMPLING} = f_D / 16$, N = 8 1101: $f_{SAMPLING} = f_D / 32$, N = 5 1110: $f_{SAMPLING} = f_D / 32$, N = 6 1111: $f_{SAMPLING} = f_D / 32$, N = 8
[3:0]	TRSEL	Trigger Source Selection These bits are used to select the trigger input (STI) for counter synchronizing 0000: Software Trigger by setting the UEVG bit 0001: Filtered input of channel 0 (TI0S0) 0010: Filtered input of channel 1 (TI1S1) 0011: External Trigger input (ETIF) 1000: Channel 0 Edge Detector (TI0BED) 1001: Internal Timer Module Trigger 0 (ITI0) 1010: Internal Timer Module Trigger 1 (ITI1) 1011: Internal Timer Module Trigger 2 (ITI2) Others: Default 0 **NOTE:** These bits must be updated only when they are not in use, i.e. the slave mode is disabled by setting the SMSEL field to 0x00.

Table 31. GPTM Internal Trigger Connection

Slave Timing Module	ITI0	ITI1	ITI2
GPTM0	GPTM1	Reserved	Reserved
GPTM1	GPTM0	Reserved	Reserved

Timer Control Register (CTR)

This register specifies the timer enable bit (TME) and CRR buffer enable bit (CRBE).

Offset: 0x010

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved						CRBE	TME
Type/Reset							RW 0	RW 0

Bits	Field	Descriptions
[1]	CRBE	Counter-Reload register Buffer Enable 0: Counter reload register can be updated immediately 1: Counter reload register can not be updated until the update event occurs
[0]	TME	Timer Enable bit 0: GPTM off 1: GPTM on - GPTM functions normally When the TME bit is cleared to 0, the counter is stopped and the GPTM consumes no power in any operation mode except for the single pulse mode and the slave trigger mode. In these two modes the TME bit can automatically be set to 1 by hardware which permits all the GPTM registers to function normally.

Channel 0 Input Configuration Register (CH0ICFR)

This register specifies the channel 0 input mode configuration.

Offset: 0x020

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	TI0SRC	Reserved						
Type/Reset	RW 0							
	23	22	21	20	19	18	17	16
	Reserved				CH0PSC		CH0CCS	
Type/Reset					RW 0	RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved				TI0F			
Type/Reset					RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[31]	TI0SRC	Channel 0 Input Source TI0 Selection 0: The GTn_CH0 pin is connected to channel 0 input TI0 1: The XOR operation output of the GTn_CH0, GTn_CH1, and GTn_CH2 pins are connected to the channel 0 input TI0
[19:18]	CH0PSC	Channel 0 Capture Input Source Prescaler Setting These bits define the effective events of the channel 0 capture input. Note that the prescaler is reset once the Channel 0 Capture/Compare Enable bit, CH0E, in the Channel Control register named CHCTR is cleared to 0. 00: No prescaler, channel 0 capture input signal is chosen for each active event 01: Channel 0 Capture input signal is chosen for every 2 events 10: Channel 0 Capture input signal is chosen for every 4 events 11: Channel 0 Capture input signal is chosen for every 8 events
[17:16]	CH0CCS	Channel 0 Capture/Compare Selection 00: Channel 0 is configured as an output 01: Channel 0 is configured as an input derived from the TI0 signal 10: Channel 0 is configured as an input derived from the TI1 signal 11: Channel 0 is configured as an input which comes from the TRCED signal derived from the Trigger Controller **NOTE:** The CH0CCS field can be accessed only when the CH0E bit is cleared to 0.

Bits	Field	Descriptions
[3:0]	TI0F	Channel 0 Input Source TI0 Filter Setting These bits define the frequency divided ratio used to sample the TI0 signal. The Digital filter in the GPTM is an N-event counter where N is defined as how many valid transitions are necessary to output a filtered signal. 0000: No filter, the sampling clock is f_D. 0001: $f_{SAMPLING} = f_{CLKIN}$, N = 2 0010: $f_{SAMPLING} = f_{CLKIN}$, N = 4 0011: $f_{SAMPLING} = f_{CLKIN}$, N = 8 0100: $f_{SAMPLING} = f_D / 2$, N = 6 0101: $f_{SAMPLING} = f_D / 2$, N = 8 0110: $f_{SAMPLING} = f_D / 4$, N = 6 0111: $f_{SAMPLING} = f_D / 4$, N = 8 1000: $f_{SAMPLING} = f_D / 8$, N = 6 1001: $f_{SAMPLING} = f_D / 8$, N = 8 1010: $f_{SAMPLING} = f_D / 16$, N = 5 1011: $f_{SAMPLING} = f_D / 16$, N = 6 1100: $f_{SAMPLING} = f_D / 16$, N = 8 1101: $f_{SAMPLING} = f_D / 32$, N = 5 1110: $f_{SAMPLING} = f_D / 32$, N = 6 1111: $f_{SAMPLING} = f_D / 32$, N = 8

Channel 1 Input Configuration Register (CH1ICFR)

This register specifies the channel 1 input mode configuration.

Offset: 0x024

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved				CH1PSC		CH1CCS	
Type/Reset					RW 0	RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved				TI1F			
Type/Reset					RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[19:18]	CH1PSC	Channel 1 Capture Input Source Prescaler Setting These bits define the effective events of the channel 1 capture input. Note that the prescaler is reset once the Channel 1 Capture/Compare Enable bit, CH1E, in the Channel Control register named CHCTR is cleared to 0. 00: No prescaler, channel 1 capture input signal is chosen for each active event 01: Channel 1 Capture input signal is chosen for every 2 events 10: Channel 1 Capture input signal is chosen for every 4 events 11: Channel 1 Capture input signal is chosen for every 8 events
[17:16]	CH1CCS	Channel 1 Capture/Compare Selection 00: Channel 1 is configured as an output 01: Channel 1 is configured as an input derived from the TI1 signal 10: Channel 1 is configured as an input derived from the TI0 signal 11: Channel 1 is configured as an input which comes from the TRCED signal derived from the Trigger Controller **NOTE:** The CH1CCS field can be accessed only when the CH1E bit is cleared to 0

Bits	Field	Descriptions
[3:0]	TI1F	Channel 1 Input Source TI1 Filter Setting These bits define the frequency divided ratio used to sample the TI1 signal. The Digital filter in the GPTM is an N-event counter where N is defined as how many valid transitions are necessary to output a filtered signal. 0000: No filter, the sampling clock is f_D. 0001: $f_{SAMPLING} = f_{CLKIN}$, N = 2 0010: $f_{SAMPLING} = f_{CLKIN}$, N = 4 0011: $f_{SAMPLING} = f_{CLKIN}$, N = 8 0100: $f_{SAMPLING} = f_D / 2$, N = 6 0101: $f_{SAMPLING} = f_D / 2$, N = 8 0110: $f_{SAMPLING} = f_D / 4$, N = 6 0111: $f_{SAMPLING} = f_D / 4$, N = 8 1000: $f_{SAMPLING} = f_D / 8$, N = 6 1001: $f_{SAMPLING} = f_D / 8$, N = 8 1010: $f_{SAMPLING} = f_D / 16$, N = 5 1011: $f_{SAMPLING} = f_D / 16$, N = 6 1100: $f_{SAMPLING} = f_D / 16$, N = 8 1101: $f_{SAMPLING} = f_D / 32$, N = 5 1110: $f_{SAMPLING} = f_D / 32$, N = 6 1111: $f_{SAMPLING} = f_D / 32$, N = 8

Channel 2 Input Configuration Register (CH2ICFR)

This register specifies the channel 2 input mode configuration.

Offset: 0x028

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved				CH2PSC		CH2CCS	
Type/Reset					RW 0	RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved				TI2F			
Type/Reset					RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[19:18]	CH2PSC	Channel 2 Capture Input Source Prescaler Setting These bits define the effective events of the channel 2 capture input. Note that the prescaler is reset once the Channel 2 Capture/Compare Enable bit, CH2E, in the Channel Control register named CHCTR is cleared to 0. 00: No prescaler, channel 2 capture input signal is chosen for each active event 01: Channel 2 Capture input signal is chosen for every 2 events 10: Channel 2 Capture input signal is chosen for every 4 events 11: Channel 2 Capture input signal is chosen for every 8 events
[17:16]	CH2CCS	Channel 2 Capture/Compare Selection 00: Channel 2 is configured as an output 01: Channel 2 is configured as an input derived from the TI2 signal 10: Channel 2 is configured as an input derived from the TI3 signal 11: Channel 2 is configured as an input which comes from the TRCED signal derived from the Trigger Controller **NOTE:** The CH2CCS field can be accessed only when the CH2E bit is cleared to 0

Bits	Field	Descriptions
[3:0]	TI2F	Channel 2 Input Source TI2 Filter Setting These bits define the frequency divided ratio used to sample the TI2 signal. The Digital filter in the GPTM is an N-event counter where N is defined as how many valid transitions are necessary to output a filtered signal. 0000: No filter, the sampling clock is f_D. 0001: $f_{SAMPLING} = f_{CLKIN}$, N = 2 0010: $f_{SAMPLING} = f_{CLKIN}$, N = 4 0011: $f_{SAMPLING} = f_{CLKIN}$, N = 8 0100: $f_{SAMPLING} = f_D / 2$, N = 6 0101: $f_{SAMPLING} = f_D / 2$, N = 8 0110: $f_{SAMPLING} = f_D / 4$, N = 6 0111: $f_{SAMPLING} = f_D / 4$, N = 8 1000: $f_{SAMPLING} = f_D / 8$, N = 6 1001: $f_{SAMPLING} = f_D / 8$, N = 8 1010: $f_{SAMPLING} = f_D / 16$, N = 5 1011: $f_{SAMPLING} = f_D / 16$, N = 6 1100: $f_{SAMPLING} = f_D / 16$, N = 8 1101: $f_{SAMPLING} = f_D / 32$, N = 5 1110: $f_{SAMPLING} = f_D / 32$, N = 6 1111: $f_{SAMPLING} = f_D / 32$, N = 8

Channel 3 Input Configuration Register (CH3ICFR)

This register specifies the channel 3 input mode configuration.

Offset: 0x02C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved				CH3PSC		CH3CCS	
Type/Reset					RW 0	RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved				TI3F			
Type/Reset					RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[19:18]	CH3PSC	Channel 3 Capture Input Source Prescaler Setting These bits define the effective events of the channel 3 capture input. Note that the prescaler is reset once the Channel 3 Capture/Compare Enable bit, CH3E, in the Channel Control register named CHCTR is cleared to 0. 00: No prescaler, channel 3 capture input signal is chosen for each active event 01: Channel 3 Capture input signal is chosen for every 2 events 10: Channel 3 Capture input signal is chosen for every 4 events 11: Channel 3 Capture input signal is chosen for every 8 events
[17:16]	CH3CCS	Channel 3 Capture/Compare Selection 00: Channel 3 is configured as an output 01: Channel 3 is configured as an input derived from the TI3 signal 10: Channel 3 is configured as an input derived from the TI2 signal 11: Channel 3 is configured as an input which comes from the TRCED signal derived from the Trigger Controller **NOTE:** The CH3CCS field can be accessed only when the CH3E bit is cleared to 0

Bits	Field	Descriptions
[3:0]	TI3F	Channel 3 Input Source TI3 Filter Setting These bits define the frequency divided ratio used to sample the TI3 signal. The Digital filter in the GPTM is an N-event counter where N is defined as how many valid transitions are necessary to output a filtered signal. 0000: No filter, the sampling clock is f_D. 0001: $f_{SAMPLING} = f_{CLKIN}$, N = 2 0010: $f_{SAMPLING} = f_{CLKIN}$, N = 4 0011: $f_{SAMPLING} = f_{CLKIN}$, N = 8 0100: $f_{SAMPLING} = f_D / 2$, N = 6 0101: $f_{SAMPLING} = f_D / 2$, N = 8 0110: $f_{SAMPLING} = f_D / 4$, N = 6 0111: $f_{SAMPLING} = f_D / 4$, N = 8 1000: $f_{SAMPLING} = f_D / 8$, N = 6 1001: $f_{SAMPLING} = f_D / 8$, N = 8 1010: $f_{SAMPLING} = f_D / 16$, N = 5 1011: $f_{SAMPLING} = f_D / 16$, N = 6 1100: $f_{SAMPLING} = f_D / 16$, N = 8 1101: $f_{SAMPLING} = f_D / 32$, N = 5 1110: $f_{SAMPLING} = f_D / 32$, N = 6 1111: $f_{SAMPLING} = f_D / 32$, N = 8

Channel 0 Output Configuration Register (CH0OCFR)

This register specifies the channel 0 output mode configuration.

Offset: 0x040

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
		Reserved	CH0IMAE	CH0PRE	REF0CE	CH0OM		
Type/Reset			RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[5]	CH0IMAE	Channel 0 Immediate Active Enable 0: No action 1: Single pulse Immediate Active Mode is enabled The CH0OREF will be forced to the compare matched level immediately after an available trigger event occurs irrespective of the result of the comparison between the CNTR and the CH0CCR values. The effective duration ends automatically at the next overflow or underflow event. **NOTE:** The CH0IMAE bit is available only if the channel 0 is configured to be operated in the PWM mode 1 or the PWM mode 2.
[4]	CH0PRE	Channel 0 Capture/Compare Register (CH0CCR) Preload Enable 0: CH0CCR preload function is disabled. The CH0CCR register can be immediately assigned a new value when the CH0PRE bit is cleared to 0 and the updated CH0CCR value is used immediately. 1: CH0CCR preload function is enabled. The new CH0CCR value will not be transferred to its shadow register until the update event occurs.
[3]	REF0CE	Channel 0 Reference Output Clear Enable 0: CH0OREF performed normally and is not affected by the ETIF signal 1: CH0OREF is forced to 0 on the high level of the ETIF signal derived from the GTn_ETI pin

Bits	Field	Descriptions
[2:0]	CH0OM	Channel 0 Output Mode Setting These bits define the functional types of the output reference signal CH0OREF 000: No Change 001: Output 0 on compare match 010: Output 1 on compare match 011: Output toggles on compare match 100: Force inactive – CH0OREF is forced to 0 101: Force active – CH0OREF is forced to 1 110: PWM mode 1 - During up-counting, channel 0 is at the active level when CNTR < CH0CCR or else at an inactive level. - During down-counting, channel 0 at the inactive level when CNTR > CH0CCR or else at an active level. 111: PWM mode 2 - During up-counting, channel 0 is at the inactive level when CNTR < CH0CCR or else at an active level. - During down-counting, channel 0 is at the active level when CNTR > CH0CCR or else at an inactive level.

Channel 1 Output Configuration Register (CH1OCFR)

This register specifies the channel 1 output mode configuration.

Offset: 0x044

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
		Reserved	CH1IMAE	CH1PRE	REF1CE	CH1OM		
Type/Reset			RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[5]	CH1IMAE	Channel 1 Immediate Active Enable 0: No action 1: Single pulse Immediate Active Mode is enabled The CH1OREF will be forced to the compare matched level immediately after an available trigger event occurs irrespective of the result of the comparison between the CNTR and the CH1CCR values. The effective duration ends automatically at the next overflow or underflow event. **NOTE:** The CH1IMAE bit is available only if the channel 1 is configured to be operated in the PWM mode 1 or the PWM mode 2.
[4]	CH1PRE	Channel 1 Capture/Compare Register (CH1CCR) Preload Enable 0: CH1CCR preload function is disabled. The CH1CCR register can be immediately assigned a new value when the CH1PRE bit is cleared to 0 and the updated CH1CCR value is used immediately. 1: CH1CCR preload function is enabled The new CH1CCR value will not be transferred to its shadow register until the update event occurs.
[3]	REF1CE	Channel 1 Reference Output Clear Enable 0: CH1OREF performed normally and is not affected by the ETIF signal 1: CH1OREF is forced to 0 on the high level of the ETIF signal derived from the GTn_ETI pin

Bits	Field	Descriptions
[2:0]	CH1OM	Channel 1 Output Mode Setting These bits define the functional types of the output reference signal CH1OREF. 000: No Change 001: Output 0 on compare match 010: Output 1 on compare match 011: Output toggles on compare match 100: Force inactive – CH1OREF is forced to 0 101: Force active – CH1OREF is forced to 1 110: PWM mode 1 - During up-counting, channel 1 is at the active level when CNTR < CH1CCR or else at an inactive level. - During down-counting, channel 1 is at the inactive level when CNTR > CH1CCR or else at an active level. 111: PWM mode 2 - During up-counting, channel 1 is at the inactive level when CNTR < CH1CCR or else at an active level. - During down-counting, channel 1 is at the active level when CNTR > CH1CCR or else at an inactive level.

Channel 2 Output Configuration Register (CH2OCFR)

This register specifies the channel 2 output mode configuration.

Offset: 0x048

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								

	7	6	5	4	3	2	1	0
		Reserved	CH2IMAE	CH2PRE	REF2CE	CH2OM		
Type/Reset			RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[5]	CH2IMAE	Channel 2 Immediate Active Enable 0: No action 1: Single pulse Immediate Active Mode is enabled The CH2OREF will be forced to the compare matched level immediately after an available trigger event occurs irrespective of the result of the comparison between the CNTR and the CH2CCR values. The effective duration ends automatically at the next overflow or underflow event. **NOTE:** The CH2IMAE bit is available only if the channel 2 is configured to be operated in the PWM mode 1 or the PWM mode 2.
[4]	CH2PRE	Channel 2 Capture/Compare Register (CH2CCR) Preload Enable 0: CH2CCR preload function is disabled. The CH2CCR register can be immediately assigned a new value when the CH2PRE bit is cleared to 0 and the updated CH2CCR value is used immediately. 1: CH2CCR preload function is enabled The new CH2CCR value will not be transferred to its shadow register until the update event occurs.
[3]	REF2CE	Channel 2 Reference Output Clear Enable 0: CH2OREF performed normally and is not affected by the ETIF signal 1: CH2OREF is forced to 0 on the high level of the ETIF signal derived from the GTn_ETI pin

Bits	Field	Descriptions
[2:0]	CH2OM	Channel 2 Output Mode Setting These bits define the functional types of the output reference signal CH2OREF. 000: No Change 001: Output 0 on compare match 010: Output 1 on compare match 011: Output toggles on compare match 100: Force inactive – CH2OREF is forced to 0 101: Force active – CH2OREF is forced to 1 110: PWM mode 1 - During up-counting, channel 2 is at the active level when CNTR < CH2CCR or else at an inactive level. - During down-counting, channel 2 is at the inactive level when CNTR > CH2CCR or else at an active level. 111: PWM mode 2 - During up-counting, channel 2 is at the inactive level when CNTR < CH2CCR or else at an active level. - During down-counting, channel 2 is at the active level when CNTR > CH2CCR or else at an inactive level.

Channel 3 Output Configuration Register (CH3OCFR)

This register specifies the channel 3 output mode configuration.

Offset: 0x04C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
		Reserved	CH3IMAE	CH3PRE	REF3CE	CH3OM		
Type/Reset			RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[5]	CH3IMAE	Channel 3 Immediate Active Enable 0: No action 1: Single pulse Immediate Active Mode is enabled The CH3OREF will be forced to the compare matched level immediately after an available trigger event occurs irrespective of the result of the comparison between the CNTR and the CH3CCR values. The effective duration ends automatically at the next overflow or underflow event. **NOTE:** The CH3IMAE bit is available only if the channel 3 is configured to be operated in the PWM mode 1 or the PWM mode 2.
[4]	CH3PRE	Channel 3 Capture/Compare Register (CH3CCR) Preload Enable 0: CH3CCR preload function is disabled. The CH3CCR register can be immediately assigned a new value when the CH3PRE bit is cleared to 0 and the updated CH3CCR value is used immediately. 1: CH3CCR preload function is enabled The new CH3CCR value will not be transferred to its shadow register until the update event occurs.
[3]	REF3CE	Channel 3 Reference Output Clear Enable 0: CH3OREF performed normally and is not affected by the ETIF signal 1: CH3OREF is forced to 0 on the high level of the ETIF signal derived from the GTn_ETI pin

Bits	Field	Descriptions
[2:0]	CH3OM	Channel 3 Output Mode Setting These bits define the functional types of the output reference signal CH3OREF 000: No Change 001: Output 0 on compare match 010: Output 1 on compare match 011: Output toggles on compare match 100: Force inactive – CH3OREF is forced to 0 101: Force active – CH3OREF is forced to 1 110: PWM mode 1 - During up-counting, channel 3 is at the active level when CNTR < CH3CCR or else at an inactive level. - During down-counting, channel 3 is at the inactive level when CNTR > CH3CCR or else at an active level. 111: PWM mode 2 - During up-counting, channel 3 is at the inactive level when CNTR < CH3CCR or else at an active level. - During down-counting, channel 3 is at the active level when CNTR > CH3CCR or else at an inactive level.

Channel Control Register (CHCTR)

This register contains the channel capture input or compare output function enable control bits.

Offset: 0x050

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								

	7	6	5	4	3	2	1	0
	Reserved	CH3E	Reserved	CH2E	Reserved	CH1E	Reserved	CH0E
Type/Reset		RW 0		RW 0	RW 0	RW 0		RW 0

Bits	Field	Descriptions
[6]	CH3E	Channel 3 Capture/Compare Enable - Channel 3 is configured as an input (CH3CCS = 0x01/0x02/0x03) 0: Input Capture Mode disabled 1: Input Capture Mode enabled - Channel 3 is configured as an output (CH3CCS = 0x00) 0: Off – Channel 3 Output signal is not active 1: On – Channel 3 Output signal generated on the corresponding output pin
[4]	CH2E	Channel 2 Capture/Compare Enable - Channel 2 is configured as an input (CH2CCS = 0x01/0x02/0x03) 0: Input Capture Mode disabled 1: Input Capture Mode enabled - Channel 2 is configured as an output (CH2CCS = 0x00) 0: Off – Channel 2 Output signal is not active 1: On – Channel 2 Output signal generated on the corresponding output pin
[2]	CH1E	Channel 1 Capture/Compare Enable - Channel 1 is configured as an input (CH1CCS = 0x01/0x02/0x03) 0: Input Capture Mode disabled 1: Input Capture Mode enabled - Channel 1 is configured as an output (CH1CCS = 0x00) 0: Off – Channel 1 Output signal is not active 1: On – Channel 1 Output signal generated on the corresponding output pin
[0]	CH0E	Channel 0 Capture/Compare Enable - Channel 0 is configured as an input (CH0CCS = 0x01/0x02/0x03) 0: Input Capture Mode disabled 1: Input Capture Mode enabled - Channel 0 is configured as an output (CH0CCS = 0x00) 0: Off – Channel 0 Output signal is not active 1: On – Channel 0 Output signal generated on the corresponding output pin

Channel Polarity Configuration Register (CHPOLR)

This register contains the channel capture input or compare output polarity control.

Offset: 0x054

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved	CH3P	Reserved	CH2P	Reserved	CH1P	Reserved	CH0P
Type/Reset		RW 0		RW 0		RW 0		RW 0

Bits	Field	Descriptions
[6]	CH3P	Channel 3 Capture/Compare Polarity - When Channel 3 is configured as an input 0: capture event occurs on a Channel 3 rising edge 1: capture event occurs on a Channel 3 falling edge - When Channel 3 is configured as an output (CH3CCS = 0x00) 0: Channel 3 Output active high 1: Channel 3 Output active low
[4]	CH2P	Channel 2 Capture/Compare Polarity - When Channel 2 is configured as an input 0: capture event occurs on a Channel 2 rising edge 1: capture event occurs on a Channel 2 falling edge - When Channel 2 is configured as an output (CH2CCS = 0x00) 0: Channel 2 Output active high 1: Channel 2 Output active low
[2]	CH1P	Channel 1 Capture/Compare Polarity - When Channel 1 is configured as an input 0: capture event occurs on a Channel 1 rising edge 1: capture event occurs on a Channel 1 falling edge - Channel 1 is configured as an output (CH1CCS = 0x00) 0: Channel 1 Output active high 1: Channel 1 Output active low
[0]	CH0P	Channel 0 Capture/Compare Polarity - When Channel 0 is configured as an input 0: capture event occurs on a Channel 0 rising edge 1: capture event occurs on a Channel 0 falling edge - When Channel 0 is configured as an output (CH0CCS = 0x00) 0: Channel 0 Output active high 1: Channel 0 Output active low

Timer Interrupt Control Register (ICTR)

This register contains the timer interrupt enable control bits.

Offset: 0x074

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved					TEVIE	Reserved	UEVIE
Type/Reset						RW 0		RW 0
	7	6	5	4	3	2	1	0
	Reserved				CH3CCIE	CH2CCIE	CH1CCIE	CH0CCIE
Type/Reset					RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[10]	TEVIE	Trigger event Interrupt Enable 0: Trigger event interrupt disabled 1: Trigger event interrupt enabled
[8]	UEVIE	Update event Interrupt Enable 0: Update event interrupt disabled 1: Update event interrupt enabled
[3]	CH3CCIE	Channel 3 Capture/Compare Interrupt Enable 0: Channel 3 interrupt disabled 1: Channel 3 interrupt enabled
[2]	CH2CCIE	Channel 2 Capture/Compare Interrupt Enable 0: Channel 2 interrupt disabled 1: Channel 2 interrupt enabled
[1]	CH1CCIE	Channel 1 Capture/Compare Interrupt Enable 0: Channel 1 interrupt disabled 1: Channel 1 interrupt enabled
[0]	CH0CCIE	Channel 0 Capture/Compare Interrupt Enable 0: Channel 0 interrupt disabled 1: Channel 0 interrupt enabled

Timer Event Generator Register (EVGR)

This register contains the software event generation bits.

Offset: 0x078

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved					TEVG	Reserved	UEVG
Type/Reset						RW 0		RW 0
	7	6	5	4	3	2	1	0
	Reserved				CH3CCG	CH2CCG	CH1CCG	CH0CCG
Type/Reset					RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[10]	TEVG	Trigger Event Generation The trigger event TEV can be generated by setting this bit. It is cleared by hardware automatically. 0: No action 1: TEVIF flag is set
[8]	UEVG	Update Event Generation The update event UEV can be generated by setting this bit. It is cleared by hardware automatically. 0: No action 1: Reinitialize the counter The counter value returns to 0 or the CRR preloaed value, depending on the counter mode in which the current timer is being used. An update operation of any related registers will also be performed. For more detail descriptions, refer to the corresponding section.
[3]	CH3CCG	Channel 3 Capture/Compare Generation A Channel 3 capture/compare event can be generated by setting this bit. It is cleared by hardware automatically. 0: No action 1: Capture/compare event is generated on channel 3 If Channel 3 is configured as an input, the counter value is captured into the CH3CCR register and then the CH3CCIF bit is set. If Channel 3 is configured as an output, the CH3CCIF bit is set.
[2]	CH2CCG	Channel 2 Capture/Compare Generation A Channel 2 capture/compare event can be generated by setting this bit. It is cleared by hardware automatically. 0: No action 1: Capture/compare event is generated on channel 2 If Channel 2 is configured as an input, the counter value is captured into the CH2CCR register and then the CH2CCIF bit is set. If Channel 2 is configured as an output, the CH2CCIF bit is set.

Bits	Field	Descriptions
[1]	CH1CCG	Channel 1 Capture/Compare Generation A Channel 1 capture/compare event can be generated by setting this bit. It is cleared by hardware automatically. 0: No action 1: Capture/compare event is generated on channel 1 If Channel 1 is configured as an input, the counter value is captured into the CH1CCR register and then the CH1CCIF bit is set. If Channel 1 is configured as an output, the CH1CCIF bit is set.
[0]	CH0CCG	Channel 0 Capture/Compare Generation A Channel 0 capture/compare event can be generated by setting this bit. It is cleared by hardware automatically. 0: No action 1: Capture/compare event is generated on channel 0 If Channel 0 is configured as an input, the counter value is captured into the CH0CCR register and then the CH0CCIF bit is set. If Channel 0 is configured as an output, the CH0CCIF bit is set.

Timer Interrupt Status Register (INTSR)

This register stores the timer interrupt status.

Offset: 0x07C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved					TEVIF	Reserved	UEVIF
Type/Reset						RW 0		RW 0
	7	6	5	4	3	2	1	0
	CH3OCF	CH2OCF	CH1OCF	CH0OCF	CH3CCIF	CH2CCIF	CH1CCIF	CH0CCIF
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[10]	TEVIF	Trigger Event Interrupt Flag This flag is set by hardware on a trigger event and is cleared by software. 0: No trigger event occurs 1: Trigger event occurs
[8]	UEVIF	Update Event Interrupt Flag. This bit is set by hardware on an update event and is cleared by software. 0: No update event occurs 1: Update event occurs **NOTE:** The update event is derived from the following conditions: - The counter overflows or underflows - The UEVG bit is set with UEVDIS=0 - A STI rising edge is received in slave restart mode with UEVDIS=0.
[7]	CH3OCF	Channel 3 Over-Capture Flag This flag is set by hardware and cleared by writing 0. 0: No over-capture event is detected 1: Capture event occurs again when the CH3CCIF bit is already set and it is not yet cleared by software
[6]	CH2OCF	Channel 2 Over-Capture Flag This flag is set by hardware and cleared by writing 0. 0: No over-capture event is detected 1: Capture event occurs again when the CH2CCIF bit is already set and it is not cleared yet by software
[5]	CH1OCF	Channel 1 Over-Capture Flag This flag is set by hardware and cleared by writing 0. 0: No over-capture event is detected 1: Capture event occurs again when the CH1CCIF bit is already set and it is not cleared yet by software.

Bits	Field	Descriptions
[4]	CH0OCF	Channel 0 Over-Capture Flag This flag is set by hardware and cleared by software writing 0. 0: No over-capture event is detected 1: Capture event occurs again when the CH0CCIF bit is already set and it is not yet cleared by software.
[3]	CH3CCIF	Channel 3 Capture/Compare Interrupt Flag - Channel 3 is configured as an output: 0: No match event occurs 1: The contents of the counter CNTR has matched the contents of the CH3CCR register. This flag is set by hardware when the counter value matches the CH3CCR value with exception in some center-aligned counting mode. It is cleared by software. - Channel 3 is configured as an input: 0: No input capture occurs 1: Input capture occurs This bit is set by hardware on a capture event. It is cleared by software or by reading the CH3CCR register.
[2]	CH2CCIF	Channel 2 Capture/Compare Interrupt Flag - Channel 2 is configured as an output: 0: No match event occurs 1: The contents of the counter CNTR has matched the contents of the CH2CCR register This flag is set by hardware when the counter value matches the CH2CCR value with exception in some center-aligned counting mode. It is cleared by software. - Channel 2 is configured as an input: 0: No input capture occurs 1: Input capture occurs. This bit is set by hardware on a capture event. It is cleared by software or by reading the CH2CCR register.
[1]	CH1CCIF	Channel 1 Capture/Compare Interrupt Flag - Channel 1 is configured as an output: 0: No match event occurs 1: The content of the counter CNTR has matched the contents of the CH1CCR register This flag is set by hardware when the counter value matches the CH1CCR value with exception in some center-aligned counting mode. It is cleared by software. - Channel 1 is configured as an input: 0: No input capture occurs 1: Input capture occurs This bit is set by hardware on a capture event. It is cleared by software or by reading the CH1CCR register.
[0]	CH0CCIF	Channel 0 Capture/Compare Interrupt Flag - Channel 0 is configured as an output: 0: No match event occurs 1: The contents of the counter CNTR has matched the content of the CH0CCR register This flag is set by hardware when the counter value matches the CH0CCR value with exception in some center-aligned counting mode. It is cleared by software. - Channel 0 is configured as an input: 0: No input capture occurs 1: Input capture occurs This bit is set by hardware on a capture event. It is cleared by software or by reading the CH0CCR register.

Timer Counter Register (CNTR)

This register stores the timer counter value.

Offset: 0x080

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	Reserved							
Type/Reset								
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	CNTV							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	CNTV							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	CNTV	Counter Value.

Timer Prescaler Register (PSCR)

This register specifies the timer prescaler value to generate the counter clock.

Offset: 0x084

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	PSCV							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	PSCV							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	PSCV	Prescaler Value These bits are used to specify the prescaler value to generate the counter clock frequency CK_CNT. $f_{CK\_CNT} = \frac{f_{CK\_PSC}}{PSCV[15:0]+1}$, where the f_{CK_PSC} is the prescaler clock source.

Timer Counter Reload Register (CRR)

This register specifies the timer counter reload value.

Offset: 0x088

Reset value: 0x0000_FFFF

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	Reserved							
Type/Reset								
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	CRV							
Type/Reset	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	CRV							
Type/Reset	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1

Bits	Field	Descriptions
[15:0]	CRV	Counter Reload Value The CRV is the reload value which is loaded into the actual counter register.

Channel 0 Capture/Compare Register (CH0CCR)

This register specifies the timer channel 0 capture/compare value.

Offset: 0x090

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	Reserved							
Type/Reset								
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	CH0CCV							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	CH0CCV							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	CH0CCV	Channel 0 Capture/Compare Value - When Channel 0 is configured as an output The CH0CCR value is compared with the counter value and the comparison result is used to trigger the CH0OREF output signal. - When Channel 0 is configured as an input The CH0CCR register stores the counter value captured by the last channel 0 capture event.

Channel 1 Capture/Compare Register (CH1CCR)

This register specifies the timer channel 1 capture/compare value.

Offset: 0x094

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	CH1CCV							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	CH1CCV							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	CH1CCV	Channel 1 Capture/Compare Value - When Channel 1 is configured as an output The CH1CCR value is compared with the counter value and the comparison result is used to trigger the CH1OREF output signal. - When Channel 1 is configured as an input The CH1CCR register stores the counter value captured by the last channel 1 capture event.

Channel 2 Capture/Compare Register (CH2CCR)

This register specifies the timer channel 2 capture/compare value.

Offset: 0x098

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	CH2CCV							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	CH2CCV							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	CH2CCV	Channel 2 Capture/Compare Value - When Channel 2 is configured as an output The CH2CCR value is compared with the counter value and the comparison result is used to trigger the CH2OREF output signal. - When Channel 2 is configured as an input The CH2CCR register stores the counter value captured by the last channel 2 capture event.

Channel 3 Capture/Compare Register (CH3CCR)

This register specifies the timer channel 3 capture/compare value.

Offset: 0x09C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	CH3CCV							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	CH3CCV							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	CH3CCV	Channel 3 Capture/Compare Value - When Channel 3 is configured as an output The CH3CCR value is compared with the counter value and the comparison result is used to trigger the CH3OREF output signal. - When Channel 3 is configured as an input The CH3CCR register stores the counter value captured by the last channel 3 capture event.

15 Real Time Clock (RTC)

Introduction

The Real Time Clock, RTC, circuitry includes the APB interface, a 32-bit up-counter, a control register, a prescaler, a compare register and a status register. Most of the RTC circuits are located in the Backup Domain (as shown shaded in Figure 32) except for the APB interface. The APB interface is located in the V_{DD18} domain. Therefore, it is necessary to be isolated from the ISO signal that comes from the power control unit when the V_{DD18} domain is powered off, i.e., when the device enters the Power-Down mode. The RTC counter is used as a wakeup timer to let the system resume from the Power-Down mode. The detailed RTC function will be described in the following sections.

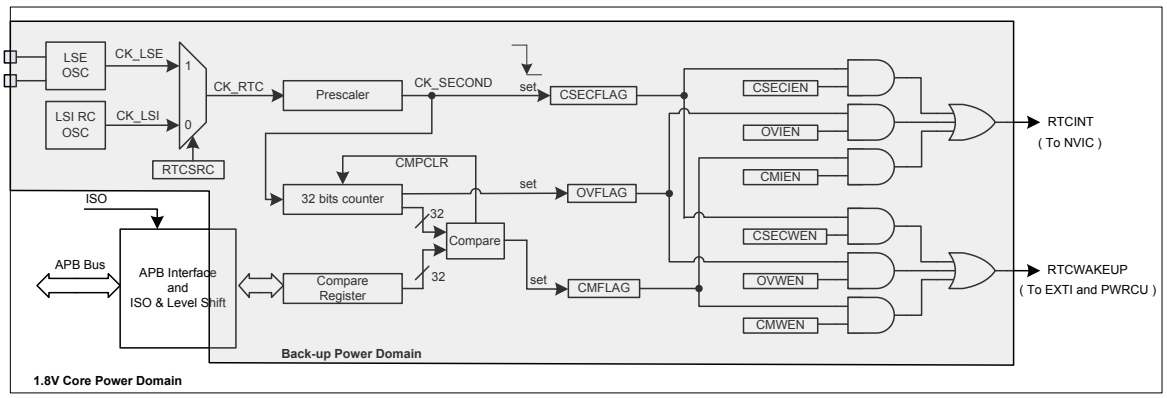


Figure 64. RTC Block Diagram

Features

- 32 bit up-counter for counting elapsed time
- Programmable clock prescaler
  - Division factor: 1, 2, 4, 8…, 32768
- 32 bit compare register for alarm usage
- RTC clock source
  - LSE oscillator clock
  - LSI oscillator clock
- Three RTC Interrupt/Wakeup settings
  - RTC second clock interrupt/wakeup
  - RTC compare match interrupt/wakeup
  - RTC counter overflow interrupt/wakeup
- The RTC interrupt/wakeup event can work together with power management to wake up the chip from the power saving mode

Functional Descriptions

RTC Related Register Reset

The RTC registers can only be reset by either a Backup Domain power on reset, PORB, or by a Backup Domain software reset by setting the BAKRST bit in the BAKCR register. Other reset events have no effect to clear the RTC registers.

Reading RTC Register

The RTC control logic and the related registers are powered by the V_{BAK} supply voltage. Therefore, the RTC circuitry remains operational in the Power-Down mode where V_{DD18} is powered off. Only the APB bus, which is located in the V_{DD18} domain, is interconnected to the circuits located in the V_{BAK} domain using level shift circuitry and isolated by the ISO signals when the V_{DD18} supply voltage is powered off. The isolation function must be disabled by setting the BAKISO bit to 1 in the LPCR register as described in the Clock Control Unit before accessing the RTC registers using the APB bus.

Low Speed Clock Configuration

The default RTC clock source, CK_RTC, is derived from the LSI oscillator. The CK_RTC clock can be derived from either the external 32768 Hz crystal oscillator, named the LSE oscillator, or the internal 32K RC oscillator named the LSI oscillator, by setting the RTCSRC bit in RTCCR register. A prescaler is provided to divide the CK_RTC by a ratio ranged from 2^0 to 2^{15} determined by the RPRE [3:0] field. For instance, setting the prescaler value RPRE[3:0] to 0x0F will generate an exact 1 Hz CK_SECOND clock if the CK_RTC clock frequency is equal to 32,768 Hz. The LSI and LSE oscillators can be enabled by the LSIEN and LSEEN control bits in the RTCCR register respectively. In addition, the LSE oscillator startup mode can be selected by configuring the LSESM bit in the RTCCR register. This enables the LSE oscillator to have either a shorter startup time or a lower power consumption. It is a traded off between startup time and power consumption depending upon specific application requirements. An example of the startup time and the power consumption for different startup modes are shown in Table 32 for reference.

Table 32. LSE Startup Mode Operating Current and Startup Time

Startup mode	LSESM Setting in RTCCR register	Operating Current	Startup time
Normal startup	0	3 uA	Above 200 ms
Fast startup	1	8 uA	Below 200 ms
@ V_{DD} = 3.3 V and LSE clock = 32768 Hz; these values are only for reference, actual values are dependent on the specification of the external 32.768KHz crystal.			

RTC Counter Operation

The RTC provides a 32-bit up-counter which increments at the falling edge of the CK_SECOND clock and whose value can be read from the RTCCNT register asynchronously via the APB bus. A 32-bit compare register, RTCCMP, is provided to store the specific value to be compared with the RTCCNT content. This is used to define a pre-determined time interval. When the RTCCNT content is equal to the RTCCMP value, the match flag CMFLAG in the RTCSR register will be set by hardware and an interrupt or wakeup event can be sent according to the corresponding enable bits in the RTCIWEN register. The RTC counter will be either reset to zero or keep counting when the compare match event occurs upon the CMPCLR bit in the RTCCR register. For example, if the RPRE[3:0] is set to 0x0F the RTCCMP field is set to a decimal value of 60 and the CMPCLR bit is set to 1, then the CMFLAG bit will be set every minute. In addition, the OVFLAG bit in the RTCSR register will be set when the RTC counter overflows. A read operation on the RTCSR register clears the status flags including the CSECFLAG, CMFLAG and OVFLAG bits.

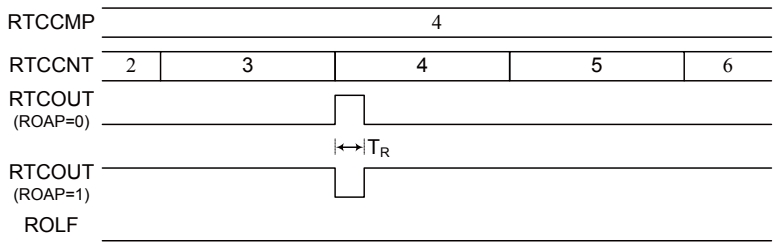
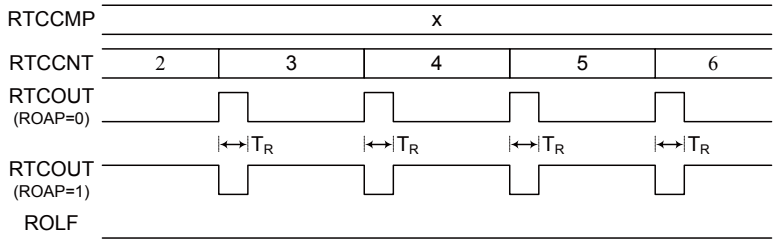
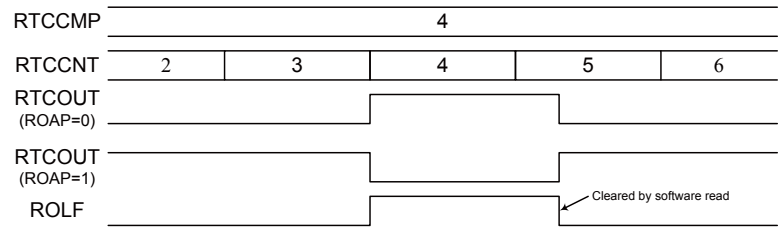
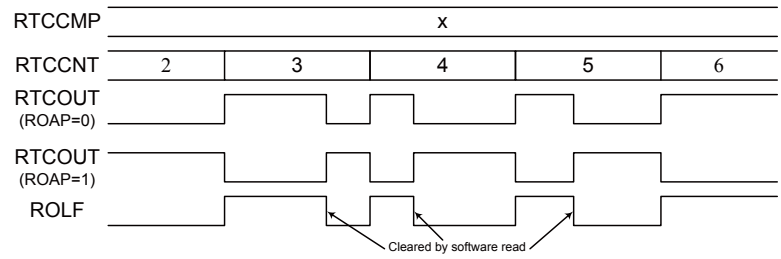
Interrupt and Wakeup Control

The falling edge of the CK_SECOND clock causes the CSECFLAG bit in the RTCSR register to be set and generates an interrupt if the corresponding interrupt enable bit, CSECIEN, in the RTCIWEN register is set. The wakeup event can also be generated to wake up the HSI/HSE oscillators, the PLL circuitry, the LDO and the Cortex™-M3 core if the corresponding wakeup enable bit CSECWEN is set. When the RTC counter overflows or a compare match event occurs, it will generate an interrupt or a wake up event determined by the corresponding interrupt or wakeup enable control bits, OVIEN/OVWEN or CMIEN/CMWEN bits, in the RTCIWEN register. Refer to the related register definitions for more details.

RTCOUT Output Pin Configuration

The following table shows the RTCOUT output format according to the mode, polarity, and event selection setting.

Table 33. RTCOUT Output Mode and Active Level Setting

ROWM	ROES	RTCOUT Output Waveform
0 (Pulse mode)	0 Compare match	
	1 Second clock	
1 (Level mode)	0 Compare match	
	1 Second clock	

T_R: RTCOUT output pulse time = 1 / f_{CK_RTC}

Register Map

The following table shows the RTC registers and reset values. Note all the registers in this unit are located at the V_{BAK} backup power domain.

Table 34. Register Map of RTC

Register	Offset	Description	Reset Value
RTC Base Address = 0x4006_A000			
RTCCNT	0x000	RTC Counter Register	0x0000_0000
RTCCMP	0x004	RTC Compare Register	0x0000_0000
RTCCR	0x008	RTC Control Register	0x0000_0F04
RTCSR	0x00C	RTC Status Register	0x0000_0000
RTCIWEN	0x010	RTC Interrupt and Wakeup Enable Register	0x0000_0000

Register Descriptions

RTC Counter Register (RTCCNT)

This register defines a 32-bit up counter which is increased by the CK_SECOND clock.

Offset: 0x000

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	RTCCNTV							
Type/Reset	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	RTCCNTV							
Type/Reset	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	RTCCNTV							
Type/Reset	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	RTCCNTV							
Type/Reset	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0

Bits	Field	Descriptions
[31:0]	RTCCNTV	RTC Counter Value The current value of the RTC counter is returned when reading the RTCCNT register. The RTCCNT register value is updated during the falling edge of the CK_SECOND. This register is reset by one of the following conditions: - Backup Domain software reset - set the BAKRST bit in the BAKCR register - Backup Domain power on reset - PORB - Compare match (RTCCNTV = RTCCMPV) when CMPCLR = 1 (in the RTCCR register) - RTCEN bit changed from 0 to 1.

RTC Compare Register (RTCCMP)

This register defines a specific value to be compared with the RTC counter value.

Offset: 0x004

Reset value: 0x0000_0000 (Reset by Backup Domain reset only)

	31	30	29	28	27	26	25	24
	RTCCMPV							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	23	22	21	20	19	18	17	16
	RTCCMPV							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
	RTCCMPV							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	RTCCMPV							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[31:0]	RTCCMPV	RTC Compare Match Value A match condition happens when the value in the RTCCNT register is equal to the RTCCMP register value. An interrupt can be generated if the CMIEN bit in the RTCIWEN register is set. When the CMPCLR bit in the RTCCR register is cleared to 0 and a match condition occurs, the CMFLAG bit in the RTCSR register will be set while the value in the RTCCNT register will not be affected and will continue to count until the counter overflows. When the CMPCLR bit is set to 1 and a match condition occurs, the CMFLAG bit in the RTCSR register will be set and the RTCCNT register will be reset to zero and then the counter continues to count.

RTC Control Register (RTCCR)

This register specifies a range of RTC circuitry control bits.

Offset: 0x008

Reset value: 0x0000_0F04 (Reset by Backup Domain reset only)

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved			ROLF	ROAP	ROWM	ROES	ROEN
Type/Reset				RC 0	RW 0	RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
	Reserved				RPRE			
Type/Reset					RW 1	RW 1	RW 1	RW 1
	7	6	5	4	3	2	1	0
		Reserved	LSESM	CMPCLR	LSEEN	LSIEN	RTCSRC	RTCEN
Type/Reset			RW 0	RW 0	RW 0	RW 1	RW 0	RW 0

Bits	Field	Descriptions
[20]	ROLF	RTCOUT Level Mode Flag 0: RTCOUT Output inactive 1: RTCOUT Output held at active level Set by hardware when level mode (ROWM = 1) and a RTCOUT output event occurred. Cleared by software reading this flag. The RTCOUT signal will return to the inactive level after software has read this bit.
[19]	ROAP	RTCOUT Output Active Polarity. 0: Active level is high. 1: Active level is low.
[18]	ROWM	RTCOUT Output Waveform Mode 0: Pulse mode The output pulse duration is one RTC clock (CK_RTC) period. 1: Level mode. The RTCOUT signal will remain at an active level until the ROLF bit is cleared by software reading the ROLF bit.
[17]	ROES	RTCOUT Output Event Selection The ROES bit can be used to select whether the RTCOUT signal is output on the RTCOUT pin when a RTC compare match event or the RTC second clock (CK_SECOND) event occurs. 0: RTC compare match event is selected 1: RTC second clock (CK_SECOND) event is selected
[16]	ROEN	RTCOUT Signal Output Enable 0: Disable RTCOUT signal output 1: Enable RTCOUT signal output When the ROEN bit is set to 1, the RTCOUT signal will be at an active level once a RTC compare match or the RTC second clock (CK_SECOND) event occurs. The active polarity and output waveform mode can be configured by the ROAP and ROWM bits respectively. When the ROEN bit is cleared to 0, the RTCOUT pin will be in a floating state.

Bits	Field	Descriptions
[11:8]	RPRE	RTC Clock Prescaler Select CK_SECOND = CK_RTC / 2^{RPRE} b0000: CK_SECOND = CK_RTC / 2^0 b0001: CK_SECOND = CK_RTC / 2^1 b0010: CK_SECOND = CK_RTC / 2^2 … b1111: CK_SECOND = CK_RTC / 2^{15}
[5]	LSESM	LSE oscillator Startup Mode 0: Normal startup and requires less operating power 1: Fast startup but requires higher operating power
[4]	CMPCLR	Compare Match Counter Clear 0: 32-bit RTC counter not affected when compare match condition occurs 1: 32-bit RTC counter cleared when compare match condition occurs
[3]	LSEEN	LSE oscillator Enable 0: LSE oscillator disabled 1: LSE oscillator enabled
[2]	LSIEN	LSI oscillator Enable 0: LSI oscillator disabled 1: LSI oscillator enabled The LSIEN bit default value is 1 which means the LSI oscillator is enabled automatically after the Backup Domain powered up. **NOTE:** After the backup domain is powered on, the internal LSI RC oscillator will start to oscillate. The frequency range of the LSI oscillator is shown in the LSI oscillator electrical characteristics in the datasheet. The device also provides a production trim value to obtain a more accurate oscillation frequency. The procedure is to disable the LSI oscillator and then enable it again after the backup domain is powered on. After the trimming procedure has completed the system will automatically load the production trim value to the frequency trimming circuit of the LSI RC oscillator.
[1]	RTCSRC	RTC Clock Source Selection 0: LSI oscillator selected as the RTC clock source 1: LSE oscillator selected as the RTC clock source
[0]	RTCEN	RTC Enable Control 0: RTC disabled 1: RTC enabled

RTC Status Register (RTCSR)

This register stores the counter flags.

Offset: 0x00C

Reset value: 0x0000_0000 (Reset by Backup Domain reset and RTCEN bit change from 1 to 0)

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved					OVFLAG	CMFLAG	CSECFLAG
Type/Reset						RC 0	RC 0	RC 0

Bits	Field	Descriptions
[2]	OVFLAG	Counter Overflow Flag 0: Counter overflow has not occurred since the last RTCSR register read operation 1: Counter overflow has occurred since the last RTCSR register read operation This bit is set by hardware when the counter value, RTCCNT, changes from 0xFFFF_ FFFF to 0x0000_0000 and cleared by read operation. This bit is suggested to read in the RTC IRQ handler and should be taken care when software polling is used.
[1]	CMFLAG	Compare Match Condition Flag 0: Compare match condition has not occurred since the last RTCSR register read operation 1: Compare match condition has occurred since the last read of RTCSR register This bit is set by hardware on the CK_SECOND clock falling edge when the RTCCNT register value is equal to the RTCCMP register value. It is cleared by software reading this bit. This bit is suggested for access in the corresponding RTC interrupt routine - do not use software polling during software free running.
[0]	CSECFLAG	CK_SECOND Occurrence Flag 0: CK_SECOND has not occurred since the last RTCSR register read operation 1: CK_SECOND has occurred since the last RTCSR register read operation This bit is set by hardware on the CK_SECOND clock falling edge. It is cleared by software reading this bit. This bit is suggested for access in the corresponding RTC interrupt routine - do not use software polling during software free running.

RTC Interrupt and Wakeup Enable Register (RTCIWEN)

This register contains the interrupt and wakeup enable bits.

Offset: 0x010

Reset value: 0x0000_0000 (Reset by Backup Domain reset only)

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved					OVWEN	CMWEN	CSECWEN
Type/Reset						RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	Reserved					OVIEN	CMIEN	CSECIEN
Type/Reset						RW 0	RW 0	RW 0

Bits	Field	Descriptions
[10]	OVWEN	Counter Overflow Wakeup Enable 0: Counter overflow wakeup disabled 1: Counter overflow wakeup enabled
[9]	CMWEN	Compare Match Wakeup Enable 0: Compare match wakeup disabled 1: Compare match wakeup enabled
[8]	CSECWEN	Counter Clock CK_SECOND Wakeup Enable 0: Counter Clock CK_SECOND wakeup disabled 1: Counter Clock CK_SECOND wakeup enabled
[2]	OVIEN	Counter Overflow Interrupt Enable 0: Counter Overflow Interrupt disabled 1: Counter Overflow Interrupt enabled
[1]	CMIEN	Compare Match Interrupt Enable 0: Compare Match Interrupt disabled 1: Compare Match Interrupt enabled
[0]	CSECIEN	Counter Clock CK_SECOND Interrupt Enable 0: Counter Clock CK_SECOND Interrupt disabled 1: Counter Clock CK_SECOND Interrupt enabled

16 Watchdog Timer (WDT)

Introduction

The Watchdog Timer is a hardware timing circuitry that can be used to detect system failures due to software malfunctions. It includes a 12-bit down-counting counter, a prescaler, a WDT counter value register, a WDT delta value register, interrupt related circuits, WDT operation control circuitry and the WDT protection mechanism. The Watchdog Timer can be operated in an interrupt mode or a reset mode. The Watchdog Timer will generate an interrupt or a reset when the counter counts down and reaches a zero value. If the software does not reload the counter value before the Watchdog Timer underflow occurs, an interrupt or a reset will be generated when the counter underflows. In addition, an interrupt or reset is also generated if the software reloads the counter when the counter value is greater than or equal to the WDT delta value. That means the counter must be reloaded within a limited timing window using a specific method. The Watchdog Timer counter can be stopped while the processor is in the debug mode. The register write protection function can be enabled to prevent it from changing the configuration of the Watchdog Timer unexpectedly.

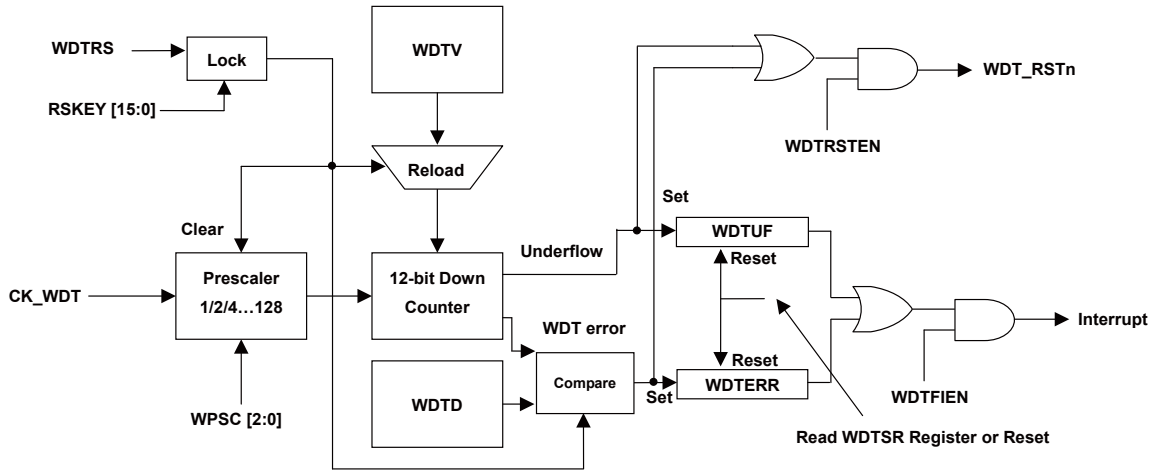


Figure 65. Watchdog Timer Block Diagram

Features

- 12-bit down counter with 3-bit prescaler
- Clock source from either internal 32 kHz RC oscillator (LSI) or external 32,768 Hz oscillator (LSE)
- Provides reset or interrupt signals to the system
- Limited reload window setting to prevent unsuitable Watchdog Timer reloads
- Watchdog Timer stopped while the processor is in the debug state
- Reload lock key to prevent unexpected operation
- Write protection function for register configuration (counter value, interrupt enable, reset enable, delta value, and prescaler)

Functional Descriptions

The Watchdog Timer consists of a 7-stage prescaler and a 12-bit down-counter. The largest time-out period is 16 seconds using the maximum prescaler value of 1/128.

The configurations of the counter reload value, the interrupt enable, the reset enable, the Delta value, and the prescaler selection in the WDTMR0 and WDTMR1 registers must be set properly before the Watchdog Timer starts to count. In order to prevent an unexpected write operation to these configurations, a register write protection function should be enabled by writing any value except the value 0x35CA to the PROTECT [15:0] bits in the WDTPR register. The value 0x35CA can be written into the PROTECT [15:0] bits to disable the register write protection function before accessing the configuration register. The read operation of the PROTECT [0] bit can obtain the enable/disable status of the register write protection function.

During normal operation, the Watchdog Timer counter should be reloaded before the counter underflows to avoid generating an interrupt or a reset. The 12-bit down counter can be reloaded with the Watchdog Timer Counter Value (WDTV) by setting WDTRS to 1 together with correct lock key 0x5FA0 specified in the WDTCR register.

If a software deadlock situation occurs in a task or a subroutine is contained within a WDT reload operation, then the reload operation will continue to function and a Watchdog Timer underflow reset or interrupt will not be generated. This will result in the software deadlock remaining undetected. To prevent this situation, the reload operation is designated to be executed when the WDT counter value is less than the WDT delta value, WDTD. A reload operation is only executed when the WDT counter value is greater than or equal to the WDT delta value which will then cause a Watchdog Timer error which generates an interrupt or reset depending on the related setting. With a proper WDT delta value being specified, if a software deadlock occurs in a task or if a subroutine is contained within a WDT reload operation, the WDT reload operation will not be executed and a WDT error interrupt or a WDT error reset will be generated to obtain CPU attention. However, the delta value feature described can be disabled by programming the WDTD to have a value greater than or equal to the WDTV value.

The WDTERR flag and the WDTUF flag in the WDTSR register will be set respectively when the Watchdog Timer underflows or the Watchdog Timer error occurs. A system reset or the read operation of the WDTSR register clears the WDTERR flag and the WDTUF flag.

When the processor enters the debug mode, the Watchdog Timer counter will either continue to count or stop, depending on the DB_WDT bit configuration in the MCUDBGCR register in the Clock Control Unit.

The following method shows how the Watchdog Timer is setup and used:

- Configure the Watchdog Timer reload value WDTV and the reset or interrupt control in the WDTMR0 register.
- Configure the Watchdog Timer delta value WDTD and the prescaler selection in the WDTMR1 register.
- Reload the Watchdog Timer by setting the RSKEY field to 0x5FA0 and the WDTRS bit to 1 in the WDTCR register.
- Write any value except 0x35CA into the WDTPR register to lock all Watchdog Timer registers except the WDTCR and the WDTPR registers.
- The Watchdog Timer counter should be reloaded again within the delta value (WDTD).

NOTE: The WDT will stop counting if APB clock is stopped or WDTEN bit in APBCCR1 register is disabled.

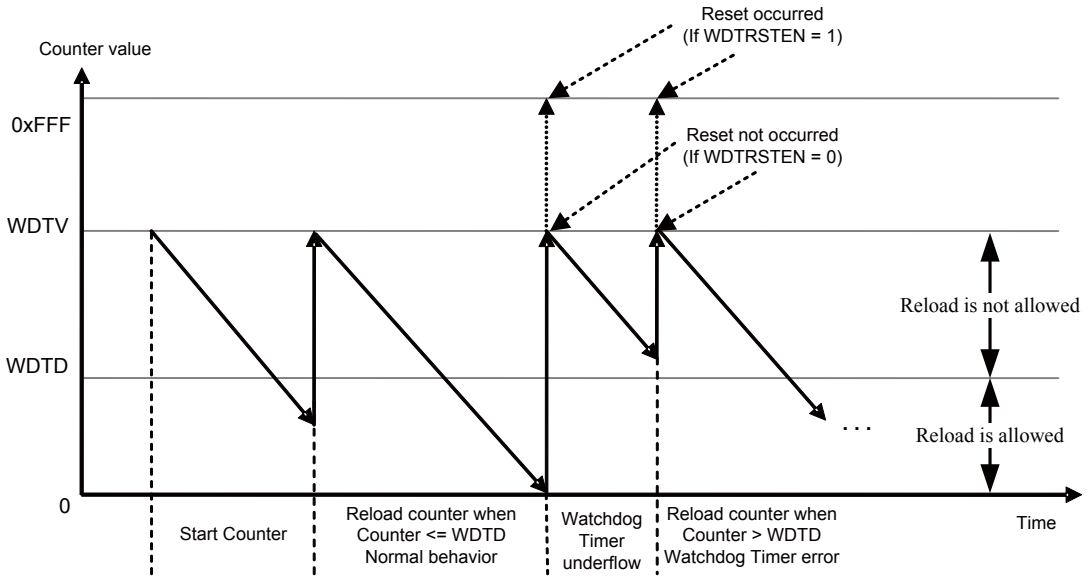


Figure 66. Watchdog Timer Behavior

Register Map

The following table shows the Watchdog Timer registers and reset values.

Table 35. Register Map of WDT

Register	Offset	Description	Reset Value
Watchdog Timer Base Address = 0x4006_8000			
WDTCR	0x000	Watchdog Timer Control Register	0x0000_0000
WDTMR0	0x004	Watchdog Timer Mode Register 0	0x0000_0FFF
WDTMR1	0x008	Watchdog Timer Mode Register 1	0x0000_7FFF
WDTSR	0x00C	Watchdog Timer Status Register	0x0000_0000
WDTPR	0x010	Watchdog Timer Protection Register	0x0000_0000

Register Descriptions

Watchdog Timer Control Register (WDTCR)

This register is used to reload the Watchdog Timer.

Offset: 0x000

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	RSKEY							
Type/Reset	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	RSKEY							
Type/Reset	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	Reserved							
Type/Reset								
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	Reserved							WDTRS
Type/Reset								WO 0

Bits	Field	Descriptions
[31:16]	RSKEY	Watchdog Timer Reload Lock Key The RSKEY [15:0] bits should be written with a value of 0x5FA0 to enable the WDT reload operation function. Writing any other value except 0x5FA0 in this field will abort the write operation.
[0]	WDTRS	Watchdog Timer Reload 0: No operation 1: Reload Watchdog Timer. This bit is used to reload the Watchdog Timer Counter with a WDTV value stored in the WDTMR0 register. It is set to 1 by software and cleared to 0 by hardware automatically.

Watchdog Timer Mode Register 0 (WDTMR0)

This register specifies the Watchdog Timer counter reload value, interrupt enable and reset enable control.

Offset: 0x004

Reset value: 0x0000_0FFF

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved		WDTRSTEN	WDTFIEN	WDTV			
Type/Reset			RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	WDTV							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[13]	WDTRSTEN	Watchdog Timer Reset Enable 0: A Watchdog Timer underflow or error event has no effect on the reset operation. 1: A Watchdog Timer underflow or error event triggers a Watchdog Timer reset.
[12]	WDTFIEN	Watchdog Timer Fault Interrupt Enable 0: A Watchdog Timer underflow or error has no effect on interrupt. 1: A Watchdog Timer underflow or error asserts an interrupt.
[11:0]	WDTV	Watchdog Timer Counter Value WDTV defines the value loaded into the 12-bit Watchdog down Counter.

Watchdog Timer Mode Register 1 (WDTMR1)

This register specifies the Watchdog delta value and the prescaler selection.

Offset: 0x008

Reset value: 0x0000_7FFF

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved	WPSC			WDTD			
Type/Reset		RW 1	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1
	7	6	5	4	3	2	1	0
	WDTD							
Type/Reset	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1

Bits	Field	Descriptions
[14:12]	WPSC	Watchdog Timer Prescaler Selection 000: 1/1 001: 1/2 010: 1/4 011: 1/8 100: 1/16 101: 1/32 110: 1/64 111: 1/128
[11:0]	WDTD	Watchdog Timer Delta Value WDTD is used to define the permitted range to reload the Watchdog Timer. If the Watchdog Timer counter value is less than the WDTD value, writing the WDTCR register with the setting including WDTRS = 1 and RSKEY = 0x5FA0 to execute a WDT reload operation will successfully reload the timer. If the Watchdog Timer value is greater than or equal to the WDTD value, writing the WDTCR register with the setting including WDTRS = 1 and RSKEY = 0x5FA0 to execute a WDT reload operation will cause a Watchdog Timer error. This feature can be disabled by programming the WDTD value to be greater than or equal to the WDTV value.

Watchdog Timer Status Register (WDTSR)

This register specifies Watchdog Timer status.

Offset: 0x00C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved						WDTERR	WDTUF
Type/Reset							RC 1	RC 1

Bits	Field	Descriptions
[1]	WDTERR	Watchdog Timer Error 0: No Watchdog Timer error occurs since the last read operation of this register 1: Watchdog Timer error occurs since last the read operation of this register **NOTE:** A reload operation will cause a Watchdog Timer error when the Watchdog Timer counter value is greater than or equal to the WDTD value.
[0]	WDTUF	Watchdog Timer Underflow 0: No Watchdog Timer underflow since the last read operation of this register 1: The Watchdog Timer underflows since the last read operation of this register

Watchdog Timer Protection Register (WDTPR)

This register specifies the Watchdog Timer write protection key configuration.

Offset: 0x010

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	PROTECT							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	PROTECT							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	PROTECT	Watchdog Timer Register Write Protection For write operation: 0x35CA: Disable the Watchdog Timer register write protection Other values: Enable the Watchdog Timer register write protection For read operation: 0x0000: Watchdog Timer register write protection is disabled 0x0001: Watchdog Timer register write protection is enabled This register is used to enable or disable the write protection of WDTMR0 and WDTMR1 registers. Enable write protection will make WDTMR0 and WDTMR1 registers become read only to prevent any unexpected write operation. Read the WDTPR register to check if the write protection is enabled or not.

17 Inter-integrated Circuit (I²C)

Introduction

The I²C Module is an internal circuit allowing communication with an external I²C interface which is an industry standard two line serial interface used for connection to external hardware. These two serial lines are known as a serial data line, SDA, and a serial clock line, SCL. The I²C module provides two data transfer rates: (1) 100 kHz in the Standard mode or (2) 400 kHz in the Fast mode. The SCL period generation register is used to setup different kinds of duty cycle implementation for the SCL pulse.

The SDA line which is connected to the whole I²C bus is a bi-directional data line between the master and slave devices used for the transmission and reception of data. The I²C module also has an arbitration detect function to prevent the situation where more than one master attempts to transmit data to the I²C bus at the same time.

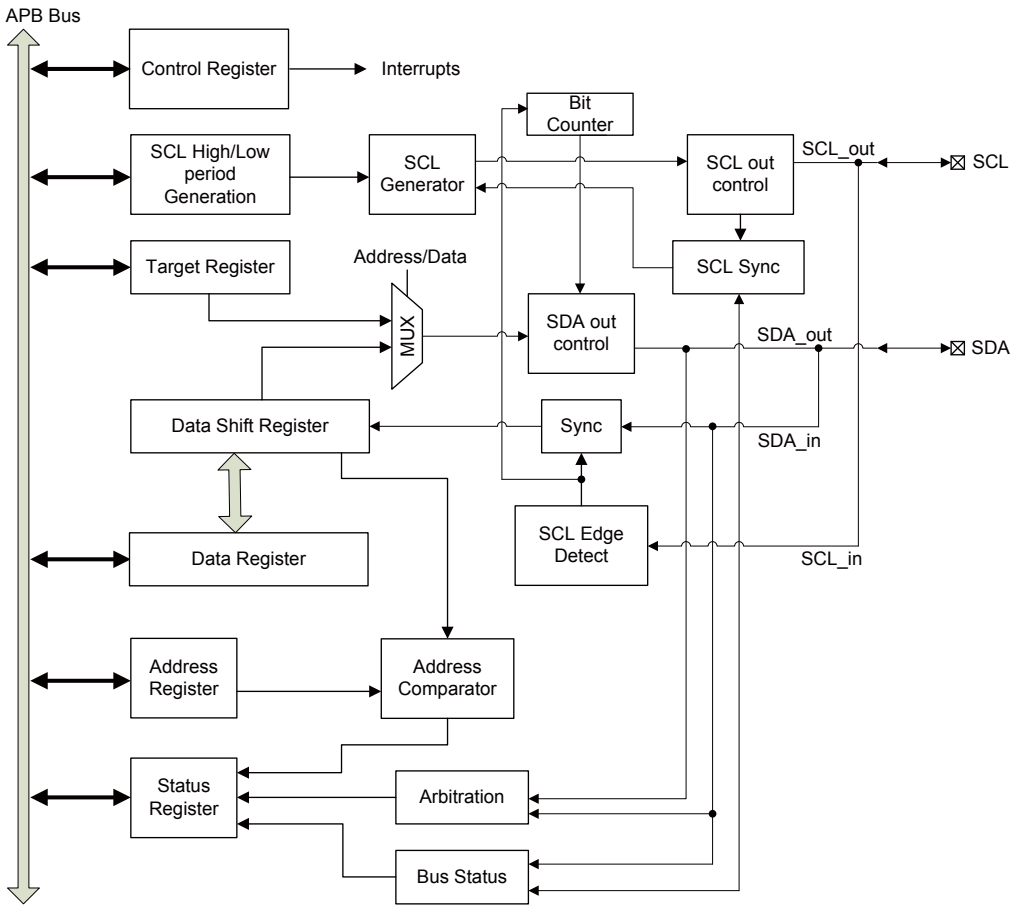


Figure 67. I²C Module Block Diagram

Features

- Two-wire I²C serial interface
  - Serial data line (SDA) and serial clock (SCL)
- Multiple speed modes
  - Standard mode - 100 kHz
  - Fast mode - 400 kHz
- Bi-directional data transfer between master and slave
- Multi-master bus - no central master
  - The same interface can act as Master or Slave
- Arbitration among simultaneously transmitting masters without corruption of serial data on the bus.
- Clock synchronization
  - Allow devices with different bit rates to communicate via one serial bus
- Supports 7-bit and 10-bit addressing mode and general call addressing

Functional Descriptions

Two Wire Serial Interface

The I²C module has two external lines, the serial data SDA and serial clock SCL lines, to carry information between the interconnected devices connected to the bus. The SCL and SDA lines are both bidirectional and must be connected to a pull-high resistor. When the I²C bus is in the free or idle state, both pins are at a high level to perform the required wired-AND function for multiple connected devices.

START and STOP Conditions

A master device can initialize a transfer by sending a START signal and terminate the transfer with a STOP signal. A START signal is usually referred to as the “S” bit, which is defined as a High to Low transition on the SDA line while the SCL line is high. A STOP signal is usually referred to as the “P” bit, which is defined as a Low to High transition on the SDA line while the SCL line is high.

A repeated START, which is denoted as the “Sr” bit, is functionally identical to the normal START condition. A repeated START signal allows the I²C interface to communicate with another slave device or with the same device but in a different transfer direction without releasing the I²C bus control.

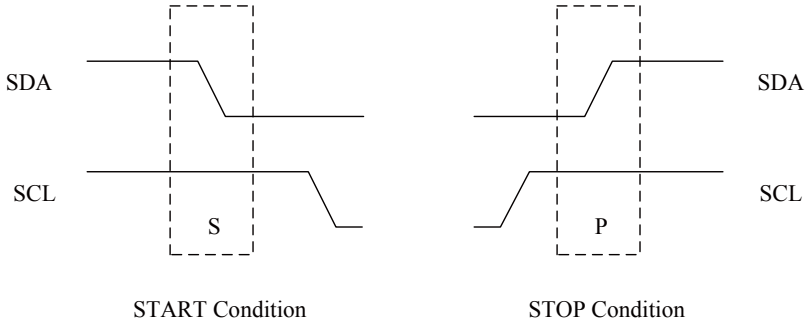


Figure 68. START and STOP Condition

Data Validity

The data on the SDA line must be stable during the high period of the SCL clock. The SDA data state can only be changed when the clock signal on the SCL line is in a low state.

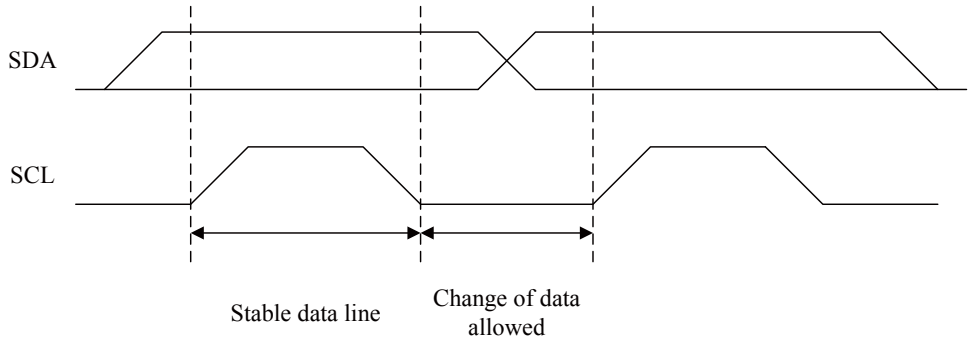


Figure 69. Data Validity

Addressing Format

The I²C interface starts to transfer data after the master device has sent the address to confirm the targeted slave device. The address frame is sent just after the START signal by master device. The addressing mode selection bit named ADRM in the I2CCR register should be defined to choose either the 7-bit or 10-bit addressing mode.

7-bit Address Format

The 7-bit address format is composed of the seven-bit length slave address, which the master device wants to communicate with, a R/$\overline{W}$ bit and an ACK bit. The R/$\overline{W}$ bit defines the direction of the data transfer.

R/$\overline{W}$ =0 (Write): The master transmits data to the addressed slave.

R/$\overline{W}$ =1 (Read): The master receives data from the addressed slave.

The slave address can be assigned through the ADDR field in the I2CADDR register. The slave device sends back the acknowledge bit (ACK) if its slave address matches the transmitted address sent by master.

Note that it is forbidden to have the same address for two slave devices.

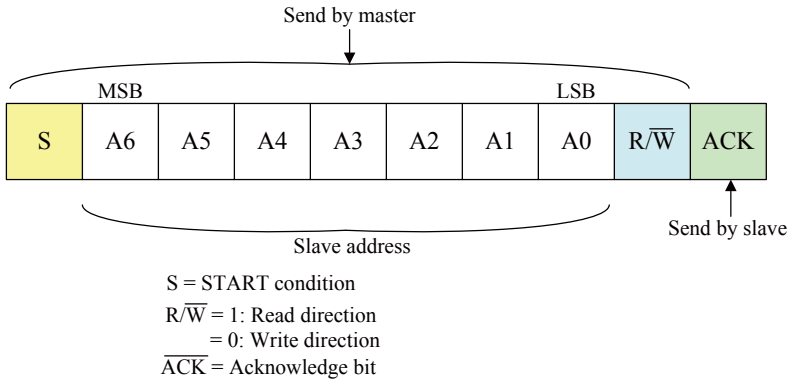


Figure 70. 7-bit Addressing Mode

10-bit Address Format

In order to prevent address clashes, due to the limited range of the 7-bit addresses, a new 10-bit address scheme has been introduced. This enhancement can be mixed with the 7-bit addressing mode which increases the available address range about ten times. For the 10-bit addressing mode, the first two bytes after a START signal include a header byte and an address byte that usually determines which slave will be selected by the master. The header byte is composed of a leading "11110", 10th and 9th bits of the slave address. The second byte is the remaining 8 bit address of the slave device.

Note that devices which use the 7-bit address format should avoid configuring the address (A6 ~ A0) as "11110xx". Otherwise, the slave will not send an ACK to the master.

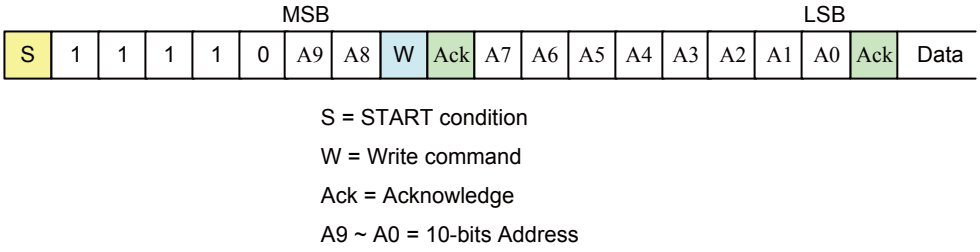


Figure 71. 10-bit Addressing Write Transmit Mode

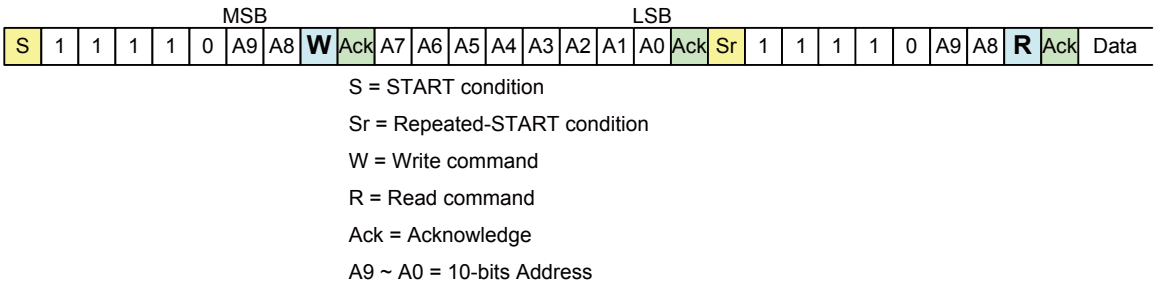


Figure 72. 10-bit Addressing Read Receive Mode

Data Transfer and Acknowledge

Once the slave device address has been matched, the data can be transmitted to or received from the slave device according to the transfer direction specified by the R/$\overline{W}$ bit. Each byte is followed by an acknowledge bit on the 9th SCL clock.

If the slave device returns a Not Acknowledge (NACK) signal to the master device, the master device can generate a STOP signal to terminate the data transfer or generate a repeated START signal to restart the transfer.

If the master device sends a Not Acknowledge (NACK) signal to the slave device, the slave device should release the SDA line for the master device to generate a STOP signal to terminate the transfer.

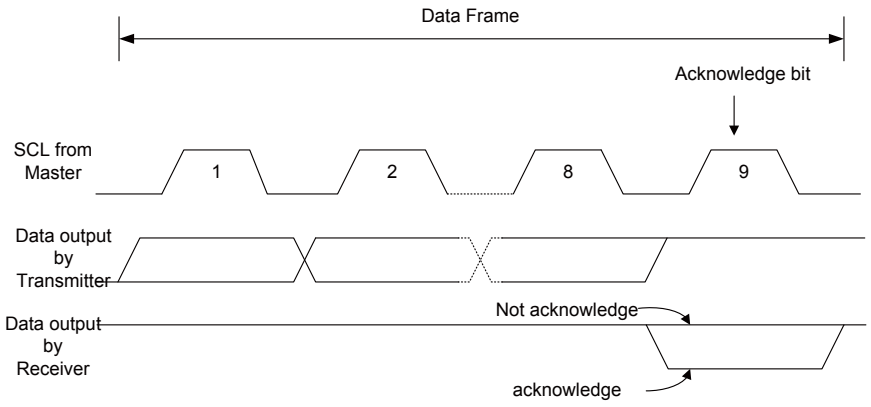


Figure 73. I²C Bus Acknowledge

Clock Synchronization

Only one master device can generate the SCL clock under normal operation. However when there is more than one master trying to generate the SCL clock, the clock should be synchronized so that the data output can be compared. Clock synchronization is performed using the wired-AND connection of the I^2C interface to the SCL line.

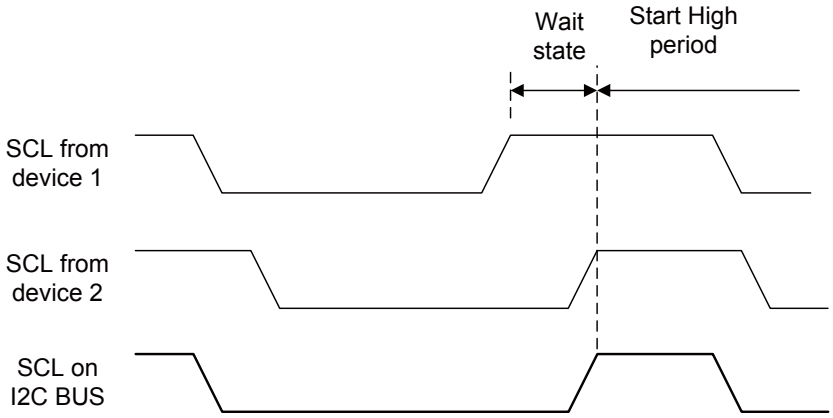


Figure 74. Clock Synchronization during Arbitration

Arbitration

A master may start a transfer only if the I²C bus line is in the free or idle mode. If two or more masters generate a START signal at approximately the same time, an arbitration procedure will occur.

Arbitration takes place on the SDA line and can continue for many bits. The arbitration procedure gives a higher priority to the device that transmits serial data with a binary low bit (logic low). Other master devices which want to transmit binary high bits (logic high) will lose the arbitration. As soon as a master loses the arbitration, the I²C module will set the ARBLOS bit in the I2CSR register and generate an interrupt if the interrupt enable bit, ARBLSIEN, in the I2CIER register is set to 1. Meanwhile, it stops sending data and listens to the bus in order to detect an I²C stop signal. When the stop signal is detected, the master which has lost the arbitration may try to access the bus again.

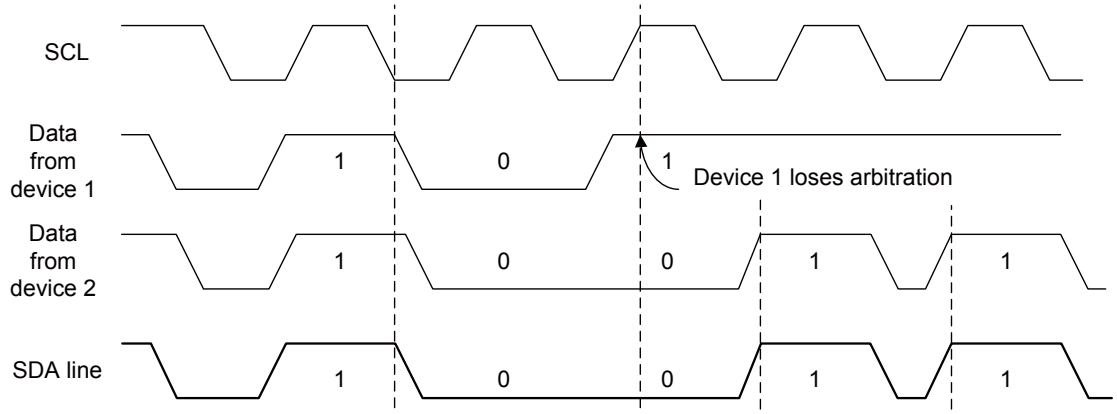


Figure 75. Two Master Arbitration Procedure

General Call Addressing

The general call addressing function can be used to address all the devices connected to the I²C bus. The master device can activate the general call function by writing 00 into the TAR and setting the RWD bit to 0 in the I2CTAR register on the addressing frame.

The device can support the general call addressing function by setting the corresponding enable control bit GCEN to 1. If the GCEN bit is set to 1 to support the general call addressing, the AA bit in the I2CCR register should also be set to 1 to send an acknowledge signal back when the device receives an address frame with a value of 00H. When this condition occurs, the general call flag, GCS, will be set to 1, but the ADRS flag will not be set.

Bus Error

If an unpredictable START or STOP condition occurs when data is being transferred on the I²C bus, it will be considered as a bus error and the transferring data will be aborted. When a bus error event occurs, the relevant bus error flag BUSERR in the I2CSR register will be set to 1 and both the SDA and SCL lines are released. The BUSERR flag should be cleared by writing 1 to it to initiate the I²C module to an idle state.

Operation Mode

The I²C module can operate in one of the following modes:

- Master Transmitter
- Master Receiver
- Slave Transmitter
- Slave Receiver

The I²C module operates in the slave mode by default. The interface will switch to the master mode automatically after generating a START signal.

Master Transmitter Mode

Start condition

Users write the target slave device address and communication direction into the I2CTAR register after setting the I2CEN bit in the I2CCR register. The STA flag in the I2CSR register is set by hardware after a start condition occurs. In order to send the following Address Frame, the STA flag must be cleared to 0 if it has been set to 1. The STA flag is cleared by reading the I2CSR register.

Address Frame

The ADRS flag in the I2CSR register will be set after the address frame is sent by the master device and the acknowledge signal from the address matched slave device is received. In order to send the following Data Frame, the ADRS flag must be cleared to 0 if it has been set to 1. The ADRS bit is cleared by reading the I2CSR register.

Data Frame

The data to be transmitted to the slave device must be transferred to the I2CDR register.

The TXDE bit in the I2CSR register is set to indicate that the I2CDR register is empty, which results in the SCL line being held at a logic low state. New data must then be transferred to the I2CDR register to continue with data transfer. Writing data into the I2CDR register will clear the TXDE flag.

Close / Continue Transmission

After transmitting the last data byte, the STOP bit in the I2CCR register can be set to terminate the transmission or re-assign another slave device by configuring the I2CTAR register to restart a new transfer.

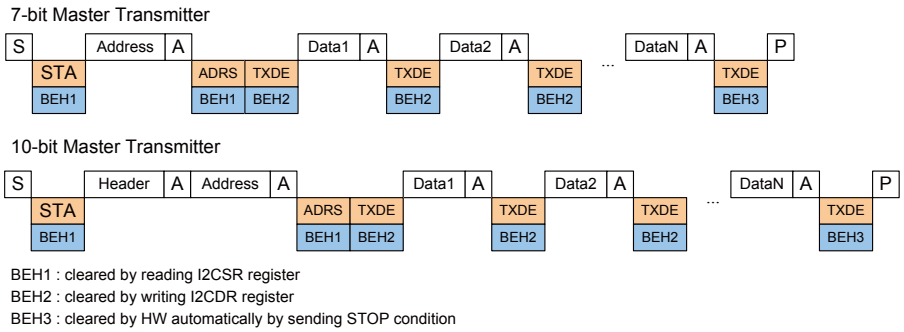


Figure 76. Master Transmitter Timing Diagram

Master Receiver Mode

Start condition

The target slave device address and communication direction must be written into the I2CTAR register. The STA flag in the I2CSR register is set by hardware after a start condition occurs. In order to send the following Address Frame, the STA flag must be cleared to 0 if it has been set to 1.The STA flag is cleared by reading the I2CSR register.

Address Frame

In the 7-bit addressing mode: The ADRS flag is set after the address frame is sent by the master device and the acknowledge signal from the address matched slave device is received. In order to receive the following Data Frame, the ADRS bit must be cleared to 0 if it has been set to 1. The ADRS bit is cleared after reading the I2CSR register.

In the 10-bit addressing mode: The ADRS bit in the I2CSR register will be set twice in the 10-bit addressing mode. The first time the ADRS bit is set is when the 10-bit address is sent and the acknowledge signal from the slave device is received. The second time the ADRS bit is set is when the header byte is sent and the slave acknowledge signal is received. In order to receive the following Data Frame, the ADRS bit must be cleared to 0 if it has been set to 1. The ADRS bit is cleared after reading the I2CSR register. The detailed master receiver mode timing diagram is shown in the following figure.

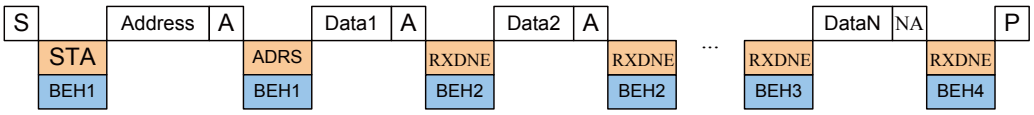
Data Frame

In the master receiver mode, data is transmitted from the slave device. Once a data is received by the master device, the RXDNE flag in the I2CSR register is set but it will not hold the SCL line. However, if the device receives a complete new data byte and the RXDNE flag has already been set to 1, the RXBF bit in the I2CSR register will be set to 1 and the SCL line will be held at a logic low state. When this situation occurs, data from the I2CDR register should be read to continue the data transfer. The RXDNE flag can be cleared after reading the I2CDR register.

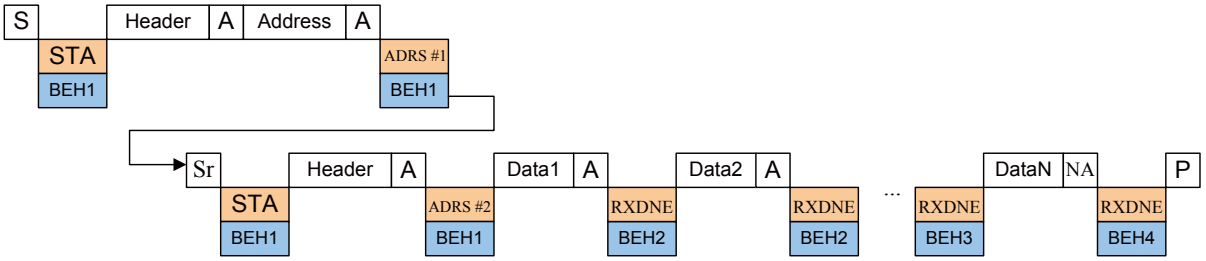
Close / Continue Transmission

The master device needs to reset the AA bit in the I2CCR register to send a NACK signal to the slave device before the last data byte transfer has been completed. After the last data byte has been received from the slave device, the master device will hold the SCL line at a logic low state following after a NACK signal sent by the master device to the slave device. The STOP bit can be set to terminate the data transfer or re-assign the I2CTAR register to restart a new transfer.

7-bit Master Receiver



10-bit Master Receiver



BEH1 : cleared by reading I2CSR register
BEH2 : cleared by reading I2CDR register
BEH3 : cleared by reading I2CDR register, set AA=0 to send NACK signal
BEH4 : cleared by reading I2CDR register, set STOP=1 to send STOP signal

Figure 77. Master Receiver Timing Diagram

Slave Transmitter Mode

Address Frame

In the 7-bit addressing mode, the ADRS bit in the I2CSR register is set after the slave device receives the calling address which matches with the slave device address. In the 10-bit addressing mode, the ADRS bit is set when the first header byte is matched and the second address byte is matched respectively. After the ADRS bit has been set to 1, it must be cleared to 0 to continue the data transfer. The ADRS bit is cleared after reading the I2CSR register.

Data Frame

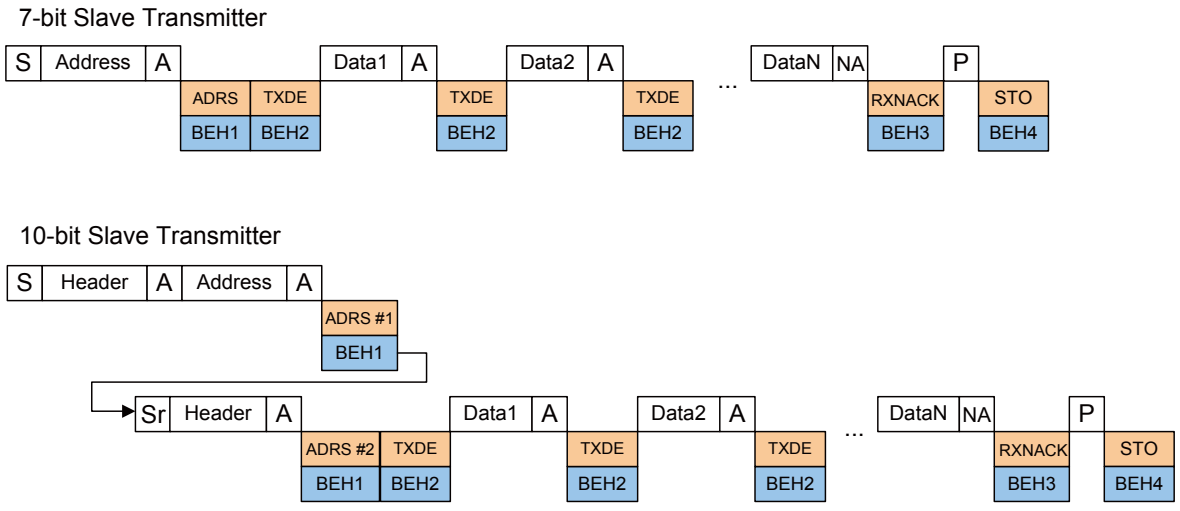
In the Slave transmitter mode, the TXDE bit is set to indicate that the I2CDR is empty, which results in the SCL line being held at a logic low state. New transmission data must then be written into the I2CDR register to continue the data transfer. Writing a data into the I2CDR register will clear the TXDE bit.

Receive Not-Acknowledge

When the slave device receives a Not-Acknowledge signal, the RXNACK bit in the I2CSR Register is set but it will not hold the SCL line. Writing 1 to RXNACK will clear the RXNACK flag.

STOP condition

When the slave device detects a STOP condition, the STO bit in the I2CSR register is set to indicate that the I^2C interface transmission is terminated. Reading the I2CSR register can clear the STO flag.



BEH1 : cleared by reading I2CSR register
BEH2 : cleared by writing I2CDR register
BEH3 : cleared by writing 1 to RXNACK flag, TXDE is not set when NACK is received.
BEH4 : cleared by reading I2CSR register

Figure 78. Slave Transmitter Timing Diagram

Slave Receiver Mode

Address Frame

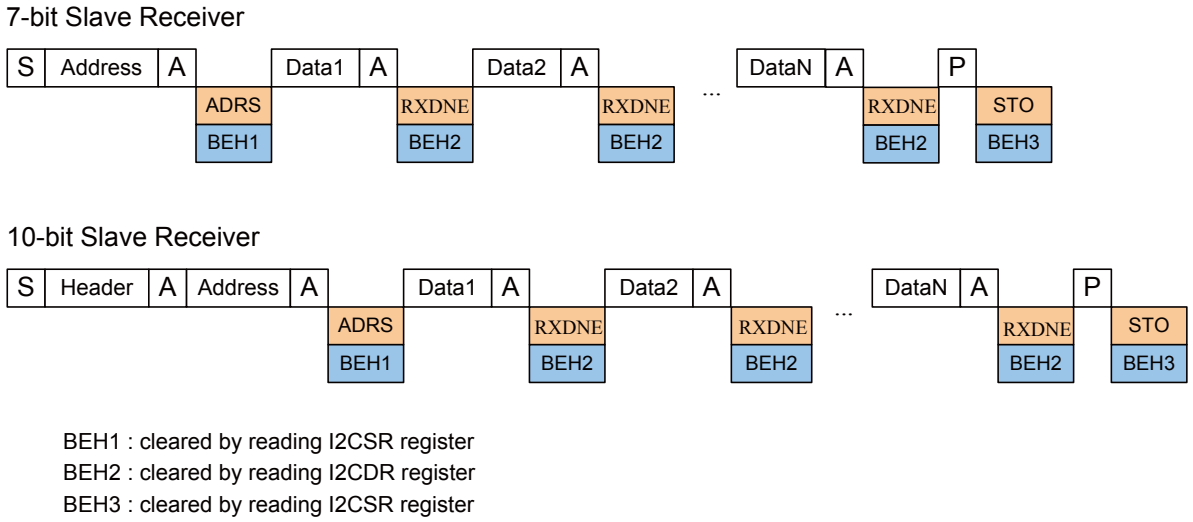
The ADRS bit in the I2CSR register is set after the slave device receives the calling address which matches with the slave device address. After the ADRS bit has been set to 1, it must be cleared to 0 to continue the data transfer. The ADRS flag is cleared after reading the I2CSR register.

Data Frame

In the slave receiver mode, the data is transmitted from the master device. Once a data byte is received by the slave device, the RXDNE flag in the I2CSR register is set but it will not hold the SCL line. However, if the device receives a complete new data byte and the RXDNE bit has been set to 1, the RXBF bit in the I2CSR register will be set to 1 and the SCL line will be held at a logic low state. When this situation occurs, data from the I2CDR register should be read to continue the data transfer. The RXDNE flag bit can be cleared after reading the I2CDR register.

STOP condition

When the slave device detects a STOP condition, the STO flag bit in the I2CSR register is set to indicate that the I²C interface transmission is terminated. Reading the I2CSR register can clear the STO flag bit.



BEH1 : cleared by reading I2CSR register
BEH2 : cleared by reading I2CDR register
BEH3 : cleared by reading I2CSR register

Figure 79. Slave Receiver Timing Diagram

Holding SCL Line Conditions

The following conditions will cause the SCL line to be held at a logic low state by hardware resulting in all I²C transfers being stopped. Data transfer will continue after the creating conditions are eliminated.

Table 36. Conditions of Holding SCL Line

Type	Condition	Description	Elimination
Flag	STA	Master device sends a START signal	Reading I2CSR register
	ADRS	Master: The I²C module sends the address frame and receives an ACK signal from the slave device (**NOTE:** Refer to *Figure 76. Master Transmitter Timing Diagram on page 280* and *Figure 77. Master Receiver Timing Diagram on page 282*. Slave: The I²C module is addressed as a slave device **NOTE:** Refer to *Figure 78. Slave Transmitter Timing Diagram on page 283* and *Figure 79. Slave Receiver Timing Diagram on page 284*.	Reading the I2CSR register
	TXDE	The I²C module is used in the transmitter mode and a new data byte to be transmitted is necessary to be loaded into the I2CDR register. **NOTE:** The TXDE bit will not be asserted after receiving a NACK signal.	Master case: Writing data to I2CDR register Set TAR Set STOP Slave case: Writing data to the I2CDR register
	RXBF	The device received complete new data and the RXDNE flag has been set already.	Reading the I2CDR register
	GCS	The I²C module is addressed as a slave device through a general call.	Reading the I2CSR register
Event	Master receives NACK	No matter whether address or data frame, when the I²C module operating in the master mode receives a NACK signal, the SCL line will be held at a logic low state.	Set TAR Set STOP
	Master sends a NACK used in received mode	When the I²C module operating in the master receiver mode receives the last data byte, the SCL line will be held at a logic low state. **NOTE:** Refer to *Figure 77. Master Receiver Timing Diagram on page 282* and the RXNACK flag will not be asserted in this case	Set TAR Set STOP

Register Map

The following table shows the I²C registers and reset values.

Table 37. Register Map of I²C

Register	Offset	Description	Reset Value
I²C Base Address = 0x4004_8000			
I2CCR	0x000	I²C Control Register	0x0000_0000
I2CIER	0x004	I²C Interrupt Enable Register	0x0000_0000
I2CADDR	0x008	I²C Device Address Register	0x0000_0000
I2CSR	0x00C	I²C Status Register	0x0000_0000
I2CSHPGR	0x010	I²C SCL High Period Generation Register	0x0000_0000
I2CSLPGR	0x014	I²C SCL Low Period Generation Register	0x0000_0000
I2CDR	0x018	I²C Data Register	0x0000_0000
I2CTAR	0x01C	I²C Target Address Register	0x0000_0000

Register Descriptions

I²C Control Register (I2CCR)

This register specifies the corresponding I²C function enable control.

Offset: 0x000

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	ADRM	Reserved			I2CEN	GCEN	STOP	AA
Type/Reset	RW 0				RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[7]	ADRM	Addressing Mode 0: 7-bit addressing mode 1: 10-bit addressing mode When I²C master/slave operates in the 7-bit addressing mode, it can only send out and respond to 7-bit address and vice versa. When I2CEN is disabled, the ADRM bit is cleared to 0 by hardware.
[3]	I2CEN	I²C Interface Enable 0: Disable I²C interface 1: Enable I²C interface
[2]	GCEN	General Call Enable 0: Disable general call function 1: Enable general call function When the device receives the calling address with a value of 0x00 and if both the GCEN and the AA bits are set to 1, then the I²C interface is addressed as a slave and the GCS bit in the I2CSR register is set to 1. When the I2CEN bit is cleared to 0 to disable the I²C interface, the GCEN bit is also cleared to 0 by hardware.
[1]	STOP	STOP Condition control 0: No action 1: Send a STOP condition in master mode This bit is set to 1 by software to generate a STOP condition and automatically cleared to 0 by hardware. The STOP bit is only available for the master device.
[0]	AA	Acknowledge Bit 0: Send a Not Acknowledge (NACK) signal after a byte is received 1: Send an Acknowledge (ACK) signal after a byte is received When the I2CEN bit is cleared to 0, the AA bit is automatically cleared to 0 by hardware.

I²C Interrupt Enable Register (I2CIER)

This register specifies the corresponding I²C interrupt enable bits.

Offset: 0x004

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved					RXBFIE	TXDEIE	RXDNEIE
Type/Reset						RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
	Reserved					BUSERRIE	RXNACKIE	ARBLOSIE
Type/Reset						RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	Reserved				GCSIE	ADRSIE	STOIE	STAIE
Type/Reset					RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[18]	RXBFIE	RX Buffer Full Interrupt Enable Bit 0: Interrupt disabled 1: Interrupt enabled When the I2CEN bit in the I2CCR register is cleared to 0, this bit is cleared to 0 by hardware.
[17]	TXDEIE	Data Register Empty Interrupt Enable Bit in Transmitter Mode 0: Interrupt disabled 1: Interrupt enabled When the I2CEN bit in the I2CCR register is cleared to 0, this bit is cleared to 0 by hardware
[16]	RXDNEIE	Data Register Not Empty Interrupt Enable Bit in Receiver Mode 0: Interrupt disabled 1: Interrupt enabled When the I2CEN bit in the I2CCR register is cleared to 0, this bit is cleared to 0 by hardware.
[10]	BUSERRIE	Bus Error Interrupt Enable Bit 0: Interrupt disabled 1: Interrupt enabled When the I2CEN bit in the I2CCR register is cleared to 0, this bit is cleared to 0 by hardware.
[9]	RXNACKIE	Received Not Acknowledge Interrupt Enable Bit 0: Interrupt disabled 1: Interrupt enabled When the I2CEN bit in the I2CCR register is cleared to 0, this bit is cleared to 0 by hardware.
[8]	ARBLOSIE	Arbitration Loss Interrupt Enable Bit in I²C multi-master mode 0: Interrupt disabled 1: Interrupt enabled When the I2CEN bit in the I2CCR register is cleared to 0, this bit is cleared to 0 by hardware.

Bits	Field	Descriptions
[3]	GCSIE	General Call Slave Interrupt Enable Bit 0: Interrupt disabled 1: Interrupt enabled When the I2CEN bit in the I2CCR register is cleared to 0, this bit is cleared to 0 by hardware.
[2]	ADRSIE	Slave Address Match Interrupt Enable Bit 1: Interrupt enabled 0: Interrupt disabled When the I2CEN bit in the I2CCR register is cleared to 0, this bit is cleared to 0 by hardware.
[1]	STOIE	STOP Condition Detected Interrupt Enable Bit 0: Interrupt disabled 1: Interrupt enabled When the I2CEN bit is cleared to 0, this bit is cleared to 0 by hardware. The bit is used for the I^2C slave mode only.
[0]	STAIE	START Condition Transmit Interrupt Enable Bit 0: Interrupt disabled 1: Interrupt enabled When the I2CEN bit in the I2CCR register is cleared to 0, this bit is cleared to 0 by hardware. The bit is used for the I^2C master mode only.

I²C Device Address Register (I2CADDR)

This register specifies the I²C device address.

Offset: 0x008

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved						ADDR	
Type/Reset							RW 0	RW 0
	7	6	5	4	3	2	1	0
	ADDR							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[9:0]	ADDR	Device Address The register indicates the I²C device address. When the I²C device is used in the 7-bit addressing mode, only the ADDR[6:0] bits will be compared with the received address sent from the I²C master device.

I²C Status Register (I2CSR)

This register contains the I²C operation status.

Offset: 0x00C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved		TXNRX	MASTER	BUSBUSY	RXBF	TXDE	RXDNE
Type/Reset			RO 0	RO 0	RO 0	RO 0	RO 0	RO 0
	15	14	13	12	11	10	9	8
	Reserved					BUSERR	RXNACK	ARBLOS
Type/Reset						WC 0	WC 0	WC 0
	7	6	5	4	3	2	1	0
	Reserved				GCS	ADRS	STO	STA
Type/Reset					RC 0	RC 0	RC 0	RC 0

Bits	Field	Descriptions
[21]	TXNRX	Transmitter / Receiver Mode 0: Receiver mode 1: Transmitter mode Read only bit.
[20]	MASTER	Master Mode 0: I²C is in the slave mode or idle 1: I²C is in the master mode The I²C interface is switched as a master device on the I²C bus when the I2CTAR register is assigned and the I²C bus is idle. The MASTER bit is cleared by hardware when software disables the I²C bus by clearing the I2CEN bit to 0 or sends a STOP condition to the I²C bus or the bus error is detected. This bit is set and cleared by hardware and is a read only bit.
[19]	BUSBUSY	Bus Busy 0: I²C bus idle 1: I²C bus busy The I²C interface hardware starts to detect the I²C bus status if the interface is enabled by setting the I2CEN bit to 1. It is set to 1 when the SDA or SCL signal is detected to have a logic low state and cleared when a STOP condition is detected.
[18]	RXBF	Buffer Full Flag in Receiver Mode 0: Data buffer not full 1: Data buffer full This bit is set when the data register I2CDR has already stored a data byte and meanwhile the data shift register also has been received a complete new data byte. The RXBF bit is cleared by software reading the I2CDR register.

Bits	Field	Descriptions
[17]	TXDE	Data Register Empty in Transmitter Mode 0: Data register I2CDR not empty 1: Data register I2CDR empty This bit is set when the I2CDR register is empty in the Transmitter mode. Note that the TXDE bit will be set after the address frame is being transmitted to inform that the data to be transmitted should be loaded into the I2CDR register. The TXDE bit is cleared by software writing data to the I2CDR register in both the master and slave modes or cleared automatically by hardware after setting the STOP signal to terminate the data transfer or setting the I2CTAR register to restart a new data transfer in the master mode.
[16]	RXDNE	Data Register Not Empty in Receiver Mode 0: Data register I2CDR empty 1: Data register I2CDR not empty This bit is set when the I2CDR register is not empty in the Receiver mode. The RXDNE bit is cleared by software reading the data byte from the I2CDR register.
[10]	BUSERR	Bus Error Flag 0: No bus error occurs 1: Bus error has occurred This bit is set by hardware when the I^2C interface detects a misplaced START or STOP condition in a transfer process. Writing 1 value to this bit will clear the BUSERR flag. In Master Mode: Once the Bus Error event occurs, both the SDA and SCL lines are released by hardware and the BUSERR flag is asserted. The application software has to clear the BUSERR flag before the next address byte is transmitted. In Slave Mode: Once a misplaced START or STOP condition has been detected by the slave device, the software must clear the BUSERR flag before the next address byte is received.
[9]	RXNACK	Received Not Acknowledge Flag 0: Acknowledge is returned from receiver 1: Not Acknowledge is returned from receiver The RXNACK bit indicates that the Not Acknowledge signal is received in master or slave transmitter mode. Writing 1 to this bit will clear the RXNACK flag.
[8]	ARBLOS	Arbitration Loss Flag 0: No arbitration loss is detected 1: Bit arbitration loss is detected This bit is set by hardware on the 9^{th} clock in the data frame when the I^2C interface loses the bus arbitration to another master during the address frame transmission. Writing 1 to this bit will clear the ARBLOS flag. Once the ARBLOS flag is asserted by hardware, the ARBLOS flag must be cleared before the next transmission.
[3]	GCS	General Call Slave Flag 0: No general call slave occurs 1: I^2C interface is addressed by a general call command When the I^2C interface receives an address with a value of 0x00 or 0x000 in the 7-bit or 10-bit addressing mode, if both the GCEN and the AA bit are set to 1, then it is switched as a general call slave. This flag is cleared automatically after being read.

Bits	Field	Descriptions
[2]	ADRS	Address Transmit (master mode) / Address Receive (slave mode) Flag Address Sent in Master mode 0: Address frame has not been transmitted 1: Address frame has been transmitted For the 7-bit addressing mode, this bit is set after the master device receives the address frame acknowledge bit sent from the slave device. For the 10-bit addressing mode, this bit is set after receiving the acknowledge bit of the first header byte and the second address. Address Matched in Slave mode 0: I^2C interface is not addressed 1: I^2C interface is addressed as slave When the I^2C interface has received the calling address that matches the address defined in the I2CADDR register together with the AA bit being set to 1 in the I2CCR register, it will be switched to a slave mode. This flag is cleared automatically after the I2CSR register has been read.
[1]	STO	STOP Condition Detected Flag 0: No STOP condition detected 1: STOP condition detected in slave mode This bit is only available for the slave mode and is cleared automatically after the I2CSR register is read.
[0]	STA	START Condition Transmit 0: No START condition detected 1: START condition is transmitted in master mode This bit is only available for the master mode and is cleared automatically after the I2CSR register is read.

I²C SCL High Period Generation Register (I2CSHPGR)

This register specifies the I²C SCL clock high period interval.

Offset: 0x010

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	SHPG							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	SHPG							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	SHPG	SCL Clock High Period Generation High period duration setting $SCL_{HIGH} = T_{PCLK} \times (SHPG + d)$ where d = 7 and T_{PCLK} is the APB bus peripheral clock (PCLK) period.

I²C SCL Low Period Generation Register (I2CSLPGR)

This register specifies the I²C SCL clock low period interval.

Offset: 0x014

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	SLPG							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	SLPG							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	SLPG	SCL Clock Low Period Generation High period duration setting SCL_{LOW} = T_{PCLK} x (SLPG + d) where d = 7 and T_{PCLK} is the APB bus peripheral clock (PCLK) period.

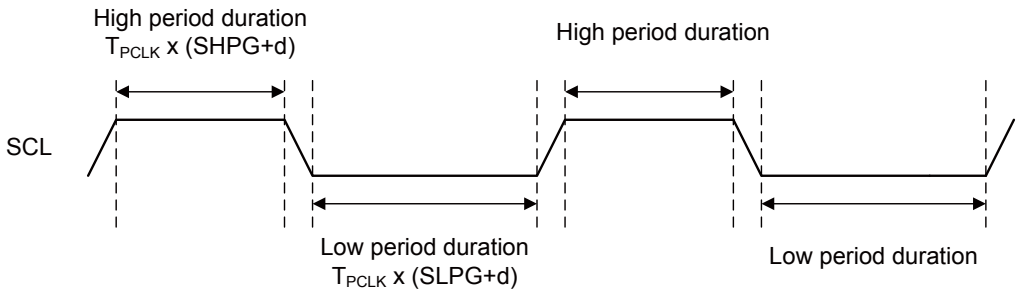


Figure 80. SCL Timing Diagram

Table 38. I²C Clock Setting Example

I²C Clock	T_{SCL} = T_{PCLK} x [(SHPG + d) + (SLPG + d)] (where d = 7) SHPG + SLPG value at PCLK			
	8MHz	24MHz	48MHz	72MHz
100 kHz (Standard Mode)	66	226	466	706
400 kHz (Fast Mode)	6	46	106	166

I²C Data Register (I2CDR)

This register specifies the data to be transmitted or received by the I²C module.

Offset: 0x018

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	DATA							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[7:0]	DATA	I²C Data Register For the transmitter mode, a data byte which is transmitted to a slave device can be assigned to these bits. The TXDE flag is cleared if the application software assigns new data to the I2CDR register. For the receiver mode, a data byte is received bit by bit from MSB to LSB through the I²C interface and stored in the data shift register. Once the acknowledge bit is given, the data shift register value is delivered into the I2CDR register if the RXDNE flag is equal to 0.

I²C Target Address Register (I2CTAR)

This register specifies the target device address to be communicated.

Offset: 0x01C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved					RWD	TAR	
Type/Reset						RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	TAR							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[10]	RWD	Read or Write Direction 0: Write direction to target slave address 1: Read direction from target slave address If this bit is set to 1 in the 10-bit master receiver mode, the I²C interface will initiate a byte with a value of 11110xx0B in the first header frame and then continue to deliver a byte with a value of 11110xx1B in the second header frame by hardware automatically.
[9:0]	TAR	Target Slave Address The I²C interface will assign a START signal and sent a target slave address automatically once data is written to this register. When the system wants to send a repeated START signal to the I²C bus, the timing is suggested to set I2CTAR register after a byte transfer is completed. It is not allowed to set TAR in the address frame. I2CTAR[9:7] will not be available under the 7-bit addressing mode.

18 Serial Peripheral Interface (SPI)

Introduction

The Serial Peripheral Interface, SPI, provides SPI protocol data transmit and receive functions in both master and slave modes. The SPI interface uses 4 pins, which are the serial data input and output lines MISO and MOSI, the clock line, SCK, and the slave select line, SEL. One SPI device acts as a master which controls the data flow using the SEL and SCK signals to indicate the start of the data communication and the data sampling rate. To receive a data byte, the streamed data bits are latched on a specific clock edge and stored in the data register or in the RX FIFO. Data transmission is carried in a similar way but with a reverse sequence. The mode fault detection provides a capability for multi-master applications.

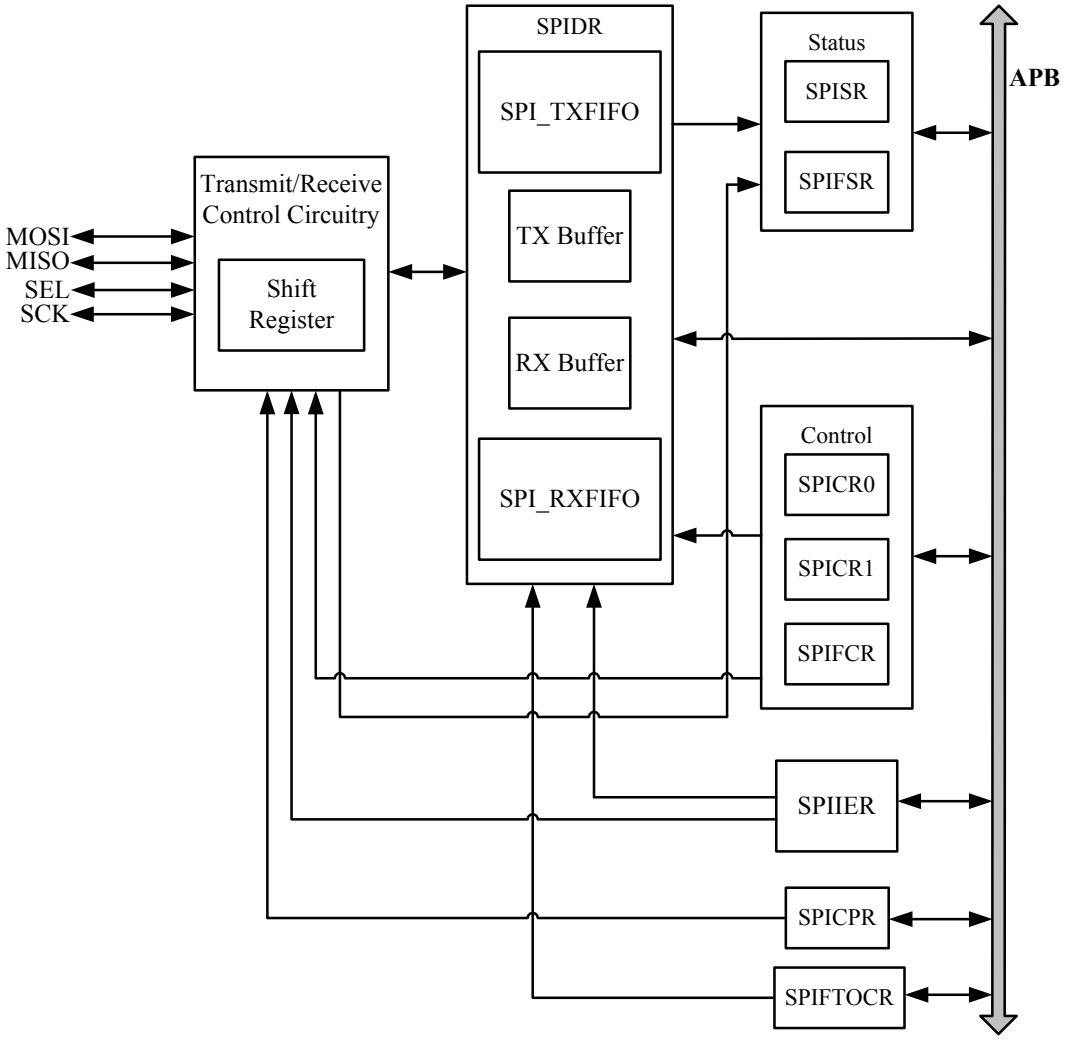


Figure 81. SPI Block Diagram

Features

- Speed up to 18 MHz
- Master or slave mode
- Programmable data frame length up to 16 bits
- FIFO Depth: 8 levels
- MSB or LSB first shift selection
- Programmable slave select high or low active polarity
- Multi-master and multi-slave operation
- Four error flags with individual interrupts
  - Read overrun
  - Write collision
  - Mode fault
  - Slave abort

Functional Descriptions

Master Mode

Each data frame can range from 1 to 16 bits in data length. The first bit of the transmitted data can be either an MSB or LSB determined by the FIRSTBIT bit in the SPICR1 register. The SPI module is configured as a master or a slave by setting the MODE bit in the SPICR1 register. When the MODE bit is set, the SPI module is configured as a master and the serial clock is generated on the SCK pin. The data byte will transmit data in the shift register to the MOSI pin on the serial clock edge. The SEL pin is active during the full data transmission. When the SELAP bit in the SPICR1 register is set, the SEL pin is active high during the complete data transactions. When the SELM bit in the SPICR1 register is set, the SEL pin will be driven by the hardware automatically and the time interval between the active SEL edge and the first edge of SCK is equal to one half an SCK period.

Slave Mode

In the slave mode, the SCK pin acts as an input pin and the serial clock will be derived from the external master device. The SEL pin also acts as an input. When the SELAP bit is cleared to 0, the SEL signal is active low during the full data byte reception. When the SELAP bit is set to 1, the SEL signal will be active high during the full data byte reception.

NOTE: For the slave mode, the APB clock, known as f_{PCLK}, must be at least 4 times faster than the external SCK clock input frequency.

SPI Serial Frame Format

The SPI Interface format is based on the Clock Polarity, CPOL, and the Clock Phase, CPHA, configurations.

■ Clock Polarity Bit - CPOL

When the Clock Polarity bit is cleared to 0, the SCK line idle state is LOW. When the Clock Polarity bit is set to 1, the SCK line idle state is HIGH.

■ Clock Phase Bit - CPHA

When the Clock Phase bit is cleared to 0, the data is sampled on the first SCK clock transition. When the Clock Phase is set to 1, the data is sampled on the second SCK clock transition.

There are four formats contained in the SPI interface. Table 39 shows how to configure these formats by setting the FORMAT field in the SPICR1 register.

Table 39. SPI Interface Format Setup

FORMAT [2:0]	CPOL	CPHA
001	0	0
010	0	1
110	1	0
101	1	1
Others	Reserved	

CPOL = 0, CPHA = 0

In this format, the received data is sampled on the SCK line rising edge while the transmitted data is changed on the SCK line falling edge. In the master mode, the first bit is driven when data is written into the SPIDR Register. In the slave mode, the first bit is driven when the SEL signal goes to an active level.

Figure 82 shows the single byte data transfer timing of this format.

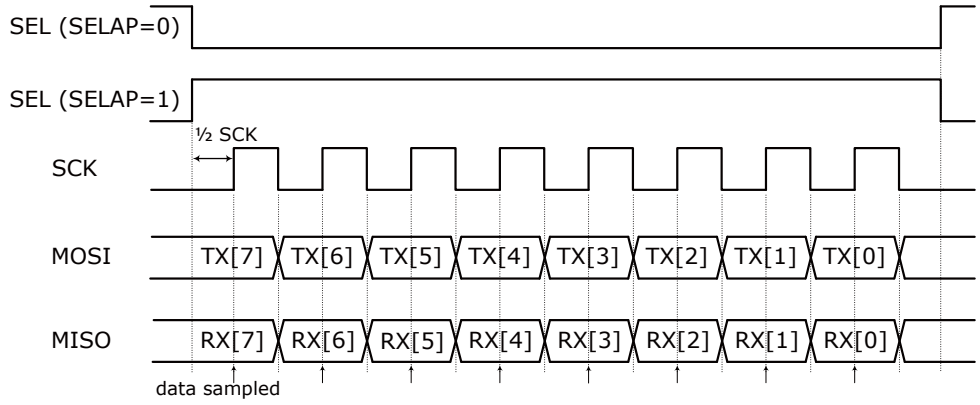


Figure 82. SPI Single Byte Transfer Timing Diagram - CPOL = 0, CPHA = 0

Figure 83 shows the continuous data transfer timing diagram of this format. Note that the SEL signal must change to an inactive level between each data frame.

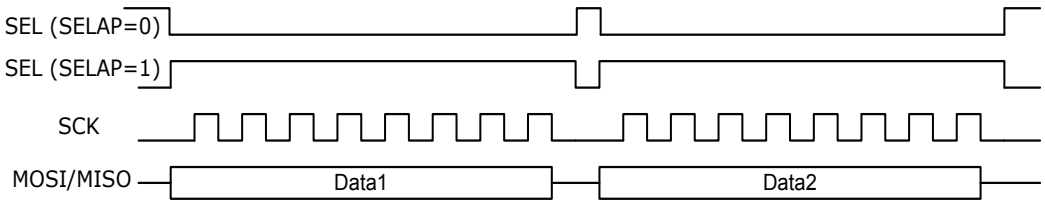


Figure 83. SPI Continuous Data Transfer Timing Diagram - CPOL = 0, CPHA = 0

CPOL = 0, CPHA = 1

In this format, the received data is sampled on the SCK line falling edge while the transmitted data is changed on the SCK line rising edge. In the master mode, the first bit is driven when data is written into the SPIDR Register. In the slave mode, the first bit is driven at the first SCK clock rising edge. Figure 84 shows the single data byte transfer timing.

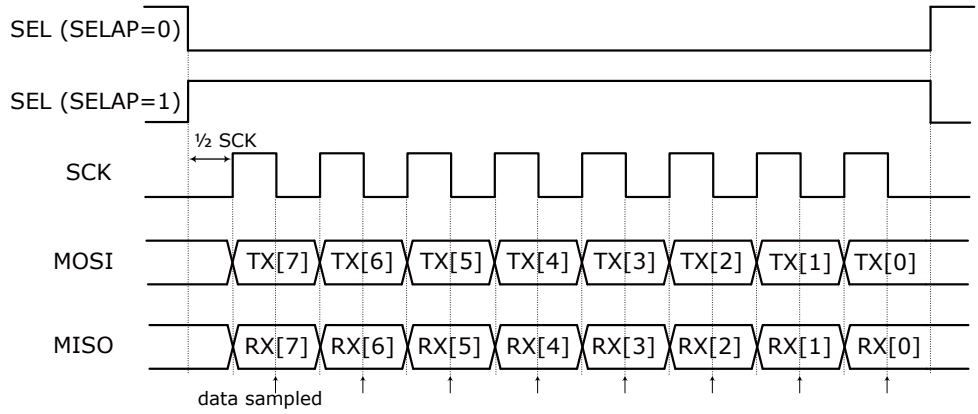


Figure 84. SPI Single Byte Transfer Timing Diagram - CPOL = 0, CPHA = 1

Figure 85 shows the continuous data transfer diagram timing. Note that the SEL signal must remain active until the last data transfer has completed.

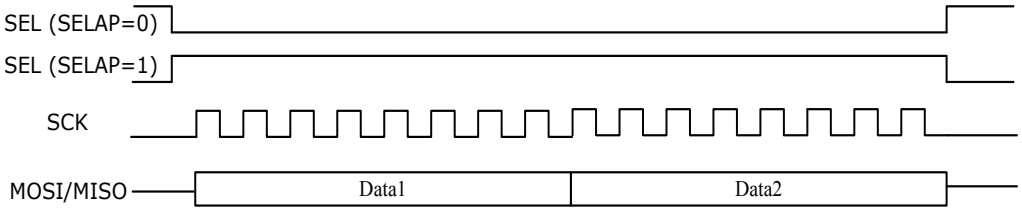


Figure 85. SPI Continuous Transfer Timing Diagram - CPOL = 0, CPHA = 1

CPOL = 1, CPHA = 0

In this format, the received data is sampled on the SCK line falling edge while the transmitted data is changed on the SCK line rising edge. In the master mode, the first bit is driven when data is written into the SPIDR Register. In the slave mode, the first bit is driven when the SEL signal changes to an active level.

Figure 86 shows the single byte data transfer timing of this format.

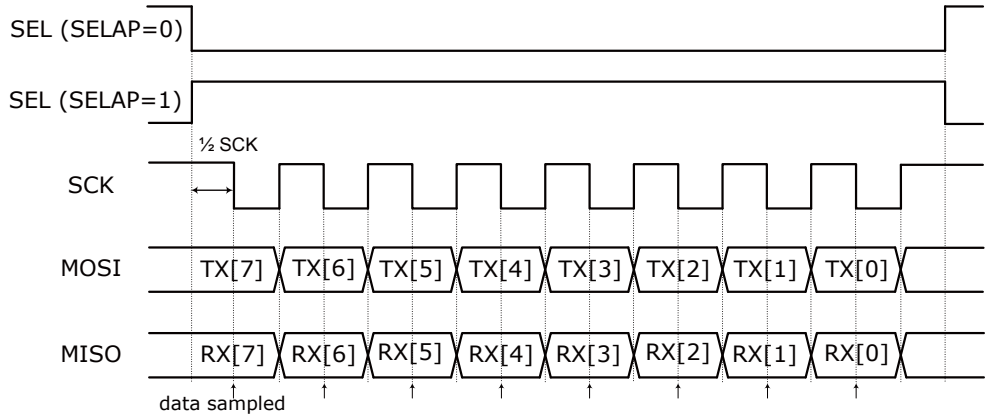


Figure 86. SPI Single Byte Transfer Timing Diagram - CPOL = 1, CPHA = 0

Figure 87 shows the continuous data transfer timing of this format. Note that the SEL signal must change to an inactive level between each data frame.

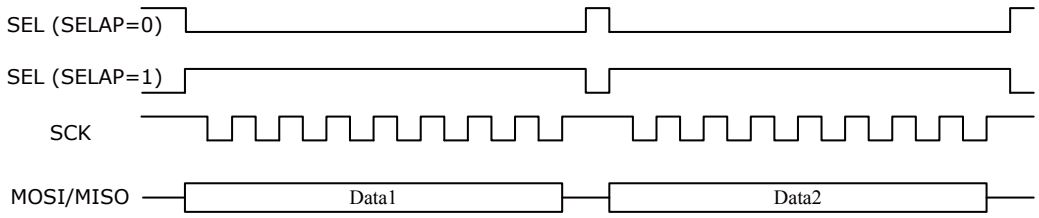


Figure 87. SPI Continuous Data Transfer Timing Diagram - CPOL = 1, CPHA = 0

CPOL = 1, CPHA = 1

In this format, the received data is sampled on the SCK line rising edge while the transmitted data is changed on the SCK line falling edge. In the master mode, the first bit is driven when data is written into the SPIDR Register. In the slave mode, the first bit is driven at the first SCK clock falling edge. Figure 88 shows the timing of this format for a single byte transfer.

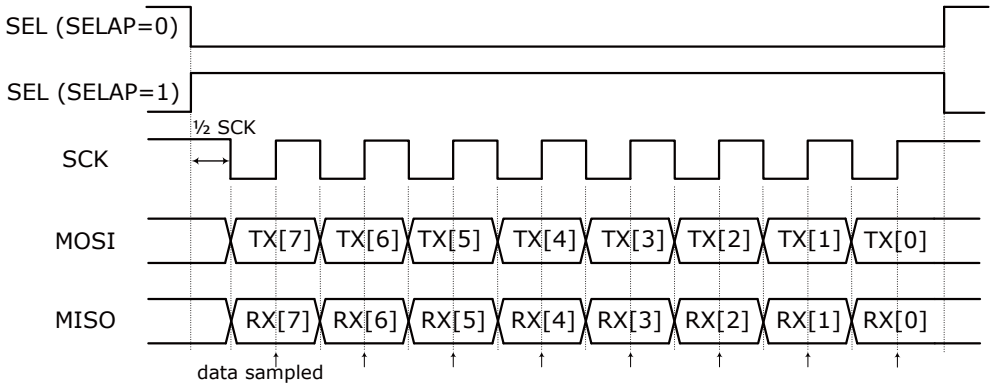


Figure 88. SPI Single Byte Transfer Timing Diagram - CPOL = 1, CPHA = 1

Figure 89 shows the continuous data transfer timing of this format. Note that the SEL signal must remain active until the last data transfer has completed.

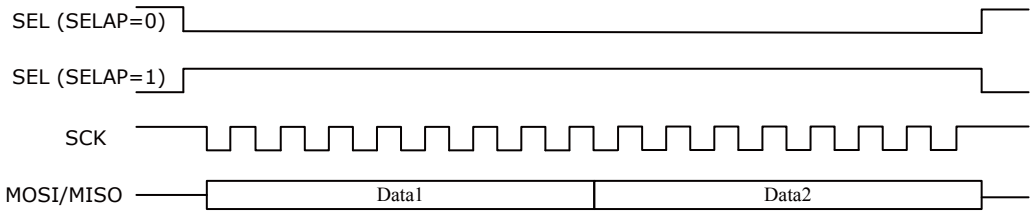


Figure 89. SPI Continuous Data Transfer Timing Diagram - CPOL = 1, CPHA = 1

Status Flags

Tx Buffer Empty - TXBE

The TXBE flag is set when the TX buffer is empty in the non-FIFO mode or when the TX FIFO data length is equal to or less than the TX FIFO threshold level as defined by the TXFTLS field in the SPIFCR register in the FIFO mode. The following data to be transmitted data can then be loaded into the buffer again. After this the TXBE flag will be reset when the TX buffer already contains new data in the non-FIFO mode or the TX FIFO data length is greater than the TX FIFO threshold level determined by the TXFTLS bits in the FIFO mode.

Transmission Register Empty - TXE

The TXE flag is set when both the TX buffer and the TX shift registers are empty. It will be reset when the TX buffer or the TX shift register contains new transmitted data.

Rx Buffer Not Empty - RXBNE

The RXBNE flag is set when there is valid received data in the RX Buffer in the non-FIFO mode or the RX FIFO data length is equal to or greater than the RX FIFO threshold level as defined by the RXFTLS field in the SPIFCR register in the SPI FIFO mode. This flag will be automatically cleared by hardware when the received data is read from the RX buffer or the RX FIFO which results in an empty RX buffer in the non-FIFO mode, or when the RX FIFO data length is less than the RX FIFO threshold level as determined by the RXFTLS bits.

Time Out Flag - TO

The time out function is only available in the SPI FIFO mode and is disabled by loading a zero value into the TOC field in the Time Out Counter register. If data is read from the SPIDR register or if new data is received, and if the SPI RX FIFO is not empty, then the time out counter will be reset to 0 and then start to count. When the time out counter value is equal to the value specified by the TOC field in the SPIFTOCR register, the TO flag will be set. The flag is cleared by writing 1 to this bit.

Mode Fault Flag - MF

The mode fault flag can be used to detect SPI bus usage in the SPI multi-master mode. For the multi-master mode, the SPI module is configured as a master device and the SEL signal is setup as an input signal. The mode fault flag is set when the SPI SEL pin is suddenly changed to an active level by another SPI master. This means that another SPI master is requesting use of the SPI bus. Therefore, when an SPI mode fault occurs, it will force the SPI module to operate in the slave mode and also disable all of the SPI interface signals to avoid SPI bus signal collisions. For the same reason, if the SPI master wants to transfer data, it also needs to inform other SPI masters by driving its SEL signal to an active state. The detailed configuration diagram for the SPI multi-master mode is shown in the following figure.

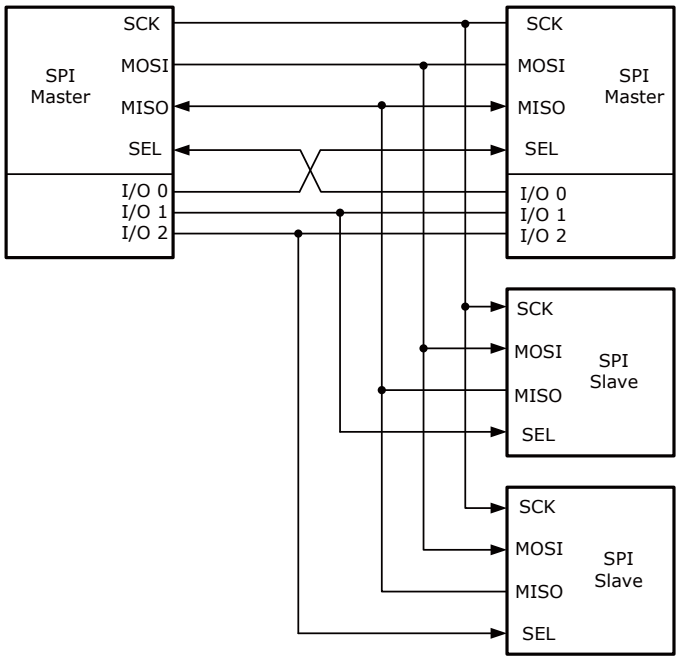


Figure 90. SPI Multi-Master Slave Environment

Table 40. SPI Mode Faulf Trigger Conditions

Mode fault	Descriptions
Trigger condition	1. SPI Master mode 2. SELOEN = 0 - SEL pin is configured in the input mode in the SPICR0 register 3. SEL signal changes to an active level when driven by the external SPI master
SPI behavior	Mode fault flag is set. The SPIEN bit in the SPICR0 register is reset. This disables the SPI interface and blocks all output signals from the device. The MODE bit in the SPICR1 register is reset. This forces the device into the slave mode.

Table 41. SPI Master Mode SEL Pin Status

	SEL as Input - SELOEN = 0		SEL as Output - SELOEN = 1	
Multi-master	Support		Not support	
SPI SEL control signal	Use another GPIO to replace the SEL pin function.		SEL pin in hardware or software mode - using SELM setting	
Continuous transfer	Case 1	Case 2	Case 1	Case 2
	Not supported	Supported	Using hardware control	Hardware or software control

CASE 1: SEL signal must be inactive between each data transfer.
CASE 2: SEL signal will not be inactive until the last data frame has finished.
NOTE: When the SPI module is in the slave mode, the SEL signal is always an input and not affected by the SELOEN bit in the SPICR0 register.

Write Collision Flag – WC

The following conditions will assert the Write Collision Flag:

1. The FIFOEN bit in the SPIFCR register is cleared.
   The write collision flag is asserted when new data is written into the SPIDR register while both the TX buffer and the shift register are already full. Any new data written into the TX buffer will be lost.
2. The FIFOEN bit in the SPIFCR register is set.
   The write collision flag is asserted to indicate that new data has been written into the SPIDR register, when the TX FIFO is already full. Any new data written into the TX FIFO will be lost.

Read Overrun Flag – RO

1. The FIFOEN bit in the SPIFCR register is cleared.
   The read overrun flag is asserted to indicate that both the RX shift register and the RX buffer are already full, when new data is received. This will result in the newly received data not being shifted into the SPI shift register. As a result the latest received data will be lost.
2. The FIFOEN bit in the SPIFCR register is set.
   The read overrun flag is set to indicate that the RX shift register and the Rx FIFO are both full, while latest data is being received. This means that the latest received data can not be shifted into the SPI shift register. As a result the latest received data will be lost.

Slave Abort Flag – SA

In the SPI slave mode, the slave abort flag is set to indicate that the SEL pin has suddenly changed to an inactive state during the reception of a data frame transfer. The data frame length is set by the DFL field in the SPICR1 register.

Register Map

The following table shows the SPI registers and their reset values.

Table 42. Register Map of SPI

Register	Offset	Description	Reset Value
SPI Base Address = 0x4000_4000			
SPICR0	0x000	SPI Control Register 0	0x0000_0000
SPICR1	0x004	SPI Control Register 1	0x0000_0000
SPIIER	0x008	SPI Interrupt Enable Register	0x0000_0000
SPICPR	0x00C	SPI Clock Prescaler Register	0x0000_0000
SPIDR	0x010	SPI Data Register	0x0000_0000
SPISR	0x014	SPI Status Register	0x0000_0003
SPIFCR	0x018	SPI FIFO Control Register	0x0000_0000
SPIFSR	0x01C	SPI FIFO Status Register	0x0000_0000
SPIFTOCR	0x020	SPI FIFO Time Out Counter Register	0x0000_0000

Register Descriptions

SPI Control Register 0 (SPICR0)

This register specifies the SEL control and the SPI enable bits.

Offset: 0x000

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved			SSELC	SELOEN		Reserved	SPIEN
Type/Reset				RW 0	RW 0			RW 0

Bits	Field	Descriptions
[4]	SSELC	Software Slave Select Control 0: Set the SEL output to an inactive state 1: Set the SEL output to an active state The application Software can setup the SEL output to an active or inactive state by configuring the SSELC bit. The active level is configured by the SELAP bit in the SPICR1 register. Note that the SSELC bit is only available when the SELOEN bit is set to 1 to enable the SEL output and the SELM bit is cleared to 0 to control the SEL signal using software. Otherwise, the SSELC bit has no effect.
[3]	SELOEN	Slave Select Output Enable 0: Set the SEL signal to the input mode for Multi-master mode 1: Set the SEL signal to the output mode for slave select The SELOEN is only available in the master mode to setup the SEL signal as an input or output signal. When the SEL signal is configured to operate in the output mode, it is used as a slave select signal in either the hardware or software mode according to the SELM bit setting in the SPICR1 register. The SEL signal is used for mode fault detection in the multi-master environment when it is configured to operate in the input mode.
[0]	SPIEN	SPI Enable 0: SPI interface disabled 1: SPI interface enabled

SPI Control Register 1 (SPICR1)

This register specifies the SPI parameters including the data length, the transfer format, the SEL active polarity/mode, the LSB/MSB control and the master/slave mode.

Offset: 0x004

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved	MODE	SELM	FIRSTBIT	SELAP	FORMAT		
Type/Reset		RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	Reserved				DFL			
Type/Reset					RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[14]	MODE	Master or Slave Mode 0: Slave mode 1: Master mode
[13]	SELM	Slave Select Mode 0: SEL signal is controlled by software - asserted or de-asserted by the SSELC bit 1: SEL signal is controlled by hardware - generated automatically by the SPI hardware Note that the SELM bit is available for the master mode only - MODE = 1
[12]	FIRSTBIT	LSB or MSB Transmitted First 0: MSB transmitted first 1: LSB transmitted first
[11]	SELAP	Slave Select Active Polarity 0: SEL signal is active low 1: SEL signal is active high

Bits	Field	Descriptions
[10:8]	FORMAT	SPI Data Transfer Format These three bits are used to determine the data transfer format of the SPI interface

FORMAT [2:0]	CPOL	CPHA
001	0	0
010	0	1
110	1	0
101	1	1
Others	Reserved	

CPOL: Clock Polarity
0: SCK Idle state is low
1: SCK Idle state is high
CPHA: Clock Phase
0: Data is captured on the first SCK clock edge
1: Data is captured on the second SCK clock edge

[3:0]	DFL	Data Frame Length Selects the data transfer data frame length from 1 bit to 16 bits. 0x1: 1 bit 0x2: 2 bits … 0xF: 15 bits 0x0: 16 bits

SPI Interrupt Enable Register (SPIIER)

This register contains the corresponding SPI interrupt enable control bits.

Offset: 0x008

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	TOIEN	SAIEN	MFIEN	ROIEN	WCIEN	RXBNEIEN	TXEIEN	TXBEIEN
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[7]	TOIEN	Time Out Interrupt Enable 0: Disable 1: Enable
[6]	SAIEN	Slave Abort Interrupt Enable 0: Disable 1: Enable
[5]	MFIEN	Mode Fault Interrupt Enable 0: Disable 1: Enable
[4]	ROIEN	Read Overrun Interrupt Enable 0: Disable 1: Enable
[3]	WCIEN	Write Collision Interrupt Enable 0: Disable 1: Enable
[2]	RXBNEIEN	RX Buffer Not Empty Interrupt Enable 0: Disable 1: Enable Generates an interrupt request when the RXBNE flag is set and when RXBNEIEN is set. In the FIFO mode, the interrupt request being generated depends upon the RX FIFO trigger level setting.
[1]	TXEIEN	TX Register Empty Interrupt Enable 0: Disable 1: Enable The TX register empty interrupt request will be generated when the TXE flag and the TXEIEN bit are set.
[0]	TXBEIEN	TX Buffer Empty Interrupt Enable 0: Disable 1: Enable The TX buffer empty interrupt request will be generated when the TXBE flag and the TXBEIEN bit are set. In the FIFO mode, the interrupt request being generated depends upon the TX FIFO trigger level setting.

SPI Clock Prescaler Register (SPICPR)

This register specifies the SPI clock prescaler ratio.

Offset: 0x00C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	CP							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	CP							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	CP	SPI Clock Prescaler The SPI clock SCK frequency is determined by the following equation: $f_{SCK} = f_{PCLK} / (2x(CP + 1))$ where the CP range is from 0 to 65535 **NOTE:** For the SPI slave mode, the system clock (f_{PCLK}) must be at least 4 times faster than the external SPI SCK input.

SPI Data Register (SPIDR)

This register stores the SPI received or transmitted Data.

Offset: 0x010

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	DR							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	DR							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	DR	Data Register The SPI data register is used to store the serial bus transmit or received data. In the non-FIFO mode, writing data into the SPI data register will also load the data into the data transmission buffer, known as the TX buffer. Reading data from the SPI data register will return the data held in the data received buffer, namely the RX buffer.

SPI Status Register (SPISR)

This register contains the relevant SPI status.

Offset: 0x014

Reset value: 0x0000_0003

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							BUSY
Type/Reset								RO 0
	7	6	5	4	3	2	1	0
	TO	SA	MF	RO	WC	RXBNE	TXE	TXBE
Type/Reset	WC 0	WC 0	WC 0	WC 0	WC 0	RO 0	RO 1	RO 1

Bits	Field	Descriptions
[8]	BUSY	SPI Busy flag 0: SPI not busy 1: SPI busy In the master mode, this flag is reset when the TX buffer and TX shift register are both empty and is set when the TX buffer or the TX shift register are not empty. In the slave mode, this flag is set when SEL changes to an active level and is reset when SEL changes to an inactive level.
[7]	TO	Time Out flag 0: No RX FIFO time out. 1: RX FIFO time out has occurred. Once the time out counter value is equal to the TOC field content in the SPIFTOCR register, the time out flag will be set and an interrupt generated if the TOIEN bit in the SPIIER register is enabled. This bit is cleared by writing 1. **NOTE:** The Time Out flag function is only available in the SPI FIFO mode.
[6]	SA	Slave Abort flag 0: No Slave Abort 1: Slave abort has occurred. This bit is set by hardware and cleared by writing 1.
[5]	MF	Mode Fault flag 0: No Mode Fault 1: Mode fault has occurred This bit is set by hardware and cleared by writing 1.
[4]	RO	Read Overrun flag 0: No Overrun 1: Read overrun has occurred. This bit is set by hardware and cleared by writing 1.
[3]	WC	Write Collision flag 0: No Write Collision 1: Write Collision has occurred. This bit is set by hardware and cleared by writing 1.

Bits	Field	Descriptions
[2]	RXBNE	Receive Buffer Not Empty flag 0: RX buffer empty 1: RX buffer not empty This bit indicates the RX buffer status in the non-FIFO mode. It is also used to indicate if the RX FIFO trigger level has been reached in the FIFO mode. This bit will be cleared when the SPI RX buffer is empty in the non-FIFO mode or if the FIFO depth is less than the trigger level which is specified by the RXFTLS field in the SPIFCR register in the SPI FIFO mode.
[1]	TXE	Transmission Register Empty flag 0: TX buffer or TX shift register is not empty 1: TX buffer and TX shift register are both empty
[0]	TXBE	Transmit Buffer Empty flag 0: TX buffer not empty 1: TX buffer empty In the FIFO mode, this bit indicates that the TX FIFO depth is equal to or less than the trigger level specified by the TXFTLS field in the SPIFCR register.

SPI FIFO Control Register (SPIFCR)

This register contains the related SPI FIFO control including the FIFO enable control, the FIFO pointer reset control and the FIFO trigger level selections.

Offset: 0x018

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved					FIFOEN	RFPR	TFPR
Type/Reset						RW 0	WO 0	WO 0
	7	6	5	4	3	2	1	0
	RXFTLS				TXFTLS			
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[10]	FIFOEN	FIFO Enable 0: FIFO disable 1: FIFO enable This bit cannot be set or reset when the SPI interface is transmitting.
[9]	RFPR	RX FIFO Pointer Reset Setting this bit will reset the RX FIFO. The RX FIFO will become empty resulting from the RX pointer being reset to 0 after a reset. The bit is returned to 0 automatically after being set.
[8]	TFPR	TX FIFO Pointer Reset Setting this bit will reset the TX FIFO. The TX FIFO will become empty resulting from the TX pointer being reset to 0 after a reset. The bit is returned to 0 automatically after being set.
[7:4]	RXFTLS	RX FIFO Trigger Level Select 0000: Trigger level is 0 0001: Trigger level is 1 ... 1000: Trigger level is 8 Others: Reserved The RXFTLS field is used to specify the RX FIFO trigger level. When the data contained in the RX FIFO is equal to or greater than the level defined by the RXFTLS field, the RXBNE flag will be set.
[3:0]	TXFTLS	TX FIFO Trigger Level Select 0000: Trigger level is 0 0001: Trigger level is 1 ... 1000: Trigger level is 8 Others: Reserved The TXFTLS field is used to specify the TX FIFO trigger level. When the data contained in the TX FIFO is equal to or less than the level defined by the TXFTLS field, the TXBE flag will be set.

SPI FIFO Status Register (SPIFSR)

This register contains the relevant SPI FIFO status.

Offset: 0x01C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	RXFS				TXFS			
Type/Reset	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0

Bits	Field	Descriptions
[7:4]	RXFS	RX FIFO Status 0000: RX FIFO empty 0001: RX FIFO contains 1 data ... 1000: RX FIFO contains 8 data Others: Reserved
[3:0]	TXFS	TX FIFO Status 0000: TX FIFO empty 0001: TX FIFO contains 1 data … 1000: TX FIFO contains 8 data Others: Reserved

SPI FIFO Time Out Counter Register (SPIFTOCR)

The register stores the SPI RX FIFO time out counter value.

Offset: 0x020

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	TOC							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	23	22	21	20	19	18	17	16
	TOC							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
	TOC							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	TOC							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[31:0]	TOC	Time Out Counter The time out counter is reset and then starts to count when the SPI RX FIFO is receiving new data or when data is read from the SPIDR register using software. If the FIFO does not receive new data and if the software does not read data from the SPIDR register, the time out counter value will be continuously increased. When the time out counter value is equal to this TOC setup value, the TO flag in the SPISR register will be set and then an interrupt will be generated if the TOIEN bit in the SPIIEN register is set. The time out counter will be reset and stop when the software continuously reads the data from the SPIDR register and allows the FIFO to become empty. The SPI FIFO time out function can be disabled by setting the TOC field to zero. The time out counter is driven by the system APB clock, named f_{PCLK}.

19 Universal Synchronous Asynchronous Receiver Transmitter (USART)

Introduction

The Universal Synchronous Asynchronous Receiver Transmitter, USART, provides a flexible full duplex data exchange using synchronous or asynchronous transfer. The USART is used to translate data between parallel and serial interfaces, and is also commonly used for RS232 standard communication. The USART peripheral function supports five-types of interrupt:

- Line Status Interrupt
- Transmitter FIFO Empty Interrupt
- Receiver Threshold Level Reaching Interrupt
- Time Out Interrupt
- MODEM Status Interrupt

The USART module includes a 16-byte transmitter FIFO, (TX_FIFO) and a 16-byte receiver FIFO (RX_FIFO).

Software can detect a USART error status by reading the Line Status Register, LSR. The status includes the type and the condition of transfer operations as well as several error conditions resulting from Parity, Overrun, Framing and Break events.

The USART includes a programmable baud rate generator which is capable of dividing the CK_AHB to produce a clock for the USART transmitter and receiver.

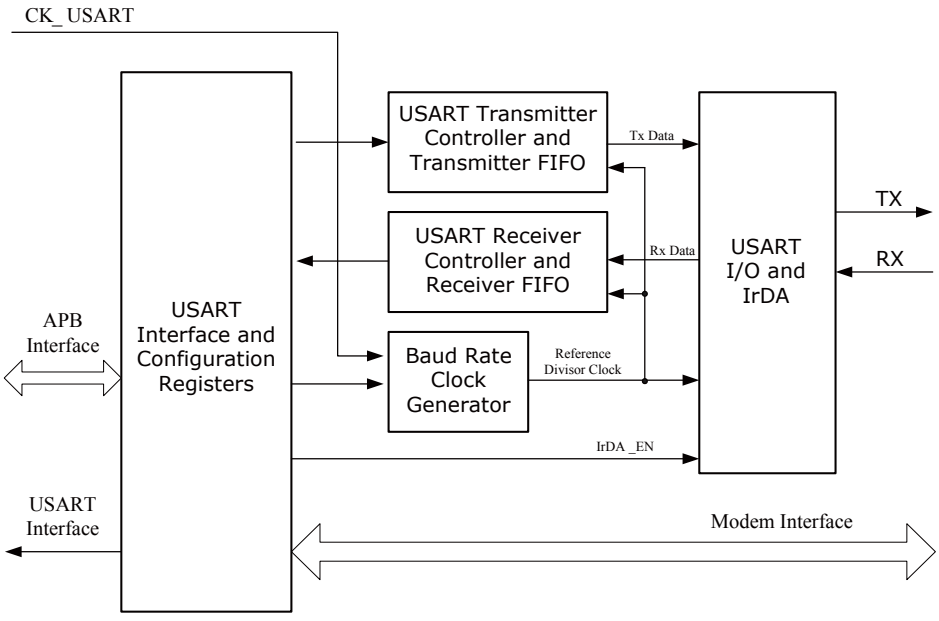


Figure 91. USART Block Diagram

Features

- Supports both asynchronous and clocked synchronous serial communication modes
- Full Duplex Communication Capability
- IrDA SIR encoder and decoder
  - Support normal 3/16 bit duration and low-power (1.41 ~ 2.23 us) duration
- Supports RS485 mode with output enable
- Full Modem function
- Fully programmable serial communication functions including:
  - Word length: 7, 8, or 9-bit character
  - Parity: even, odd, or no-parity bit generation and detection
  - Stop bit: 1 or 2 stop bit generation
  - Bit order: LSB-first or MSB-first transfer
- Error detection: Parity, overrun, and frame error
- FIFO:
  - Receiver FIFO: 16 x 9 bits (max. 9 data bits)
  - Transmitter FIFO: 16 x 9 bits (max. 9 data bits)

Functional Descriptions

Serial Data Format

The USART module performs a parallel-to-serial conversion on data that is read from the Transmitter FIFO and then sends the data with the following format: start bit, 7 ~ 9 LSB first data bits, optional parity bit and finally 1 ~ 2 stop bits. The start bit has the opposite polarity of the data line idle state. The stop bit is the same as the data line idle state and provides a delay before the next start condition. The start and stop bits are both used for data synchronisation during asynchronous data transmission.

The USART module also performs a serial-to-parallel conversion on data that is read in from the Receiver FIFO. It will first check the Parity bit and will then look for a Stop bit. If the Stop bit is not found, the USART module will consider the entire word transmission to have failed and respond with a Framing Error.

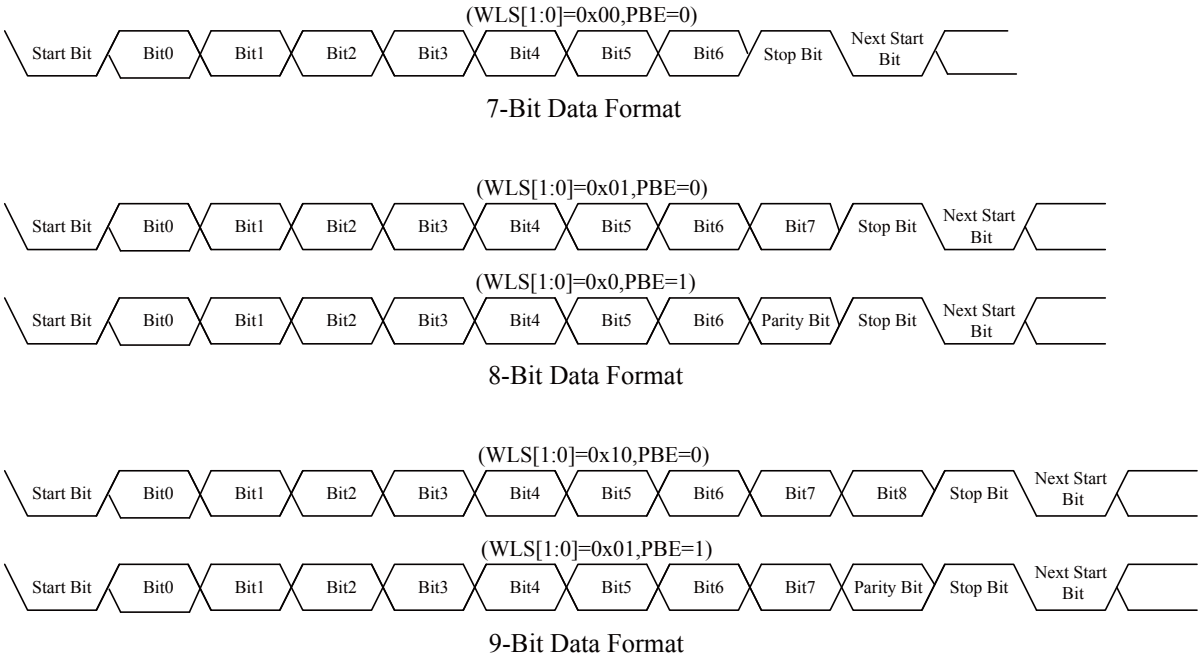


Figure 92. USART Serial Data Format

Baud Rate Generation

The baud rate for the USART receiver and transmitter are both set with the same values. The baud-rate divisor, BRD, has the following relationship with the USART clock which is known as CK_USART.

```
Baud Rate Clock = CK_USART / BRD
```

where the CK_USART clock is the system clock connected to the USART module while the BRD range is from 16 to 65535.

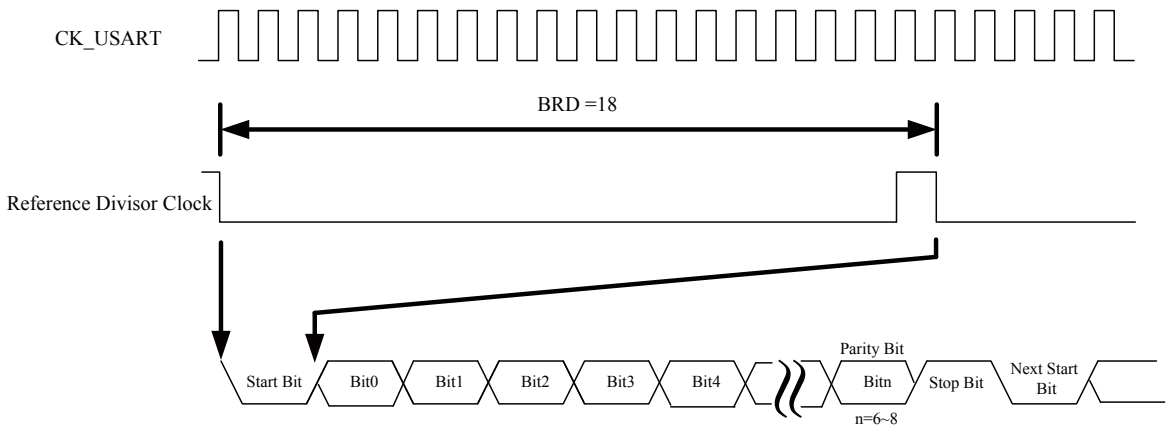


Figure 93. USART Clock CK_USART and Data Frame Timing

Table 43. Baud Rate Error Calculation - CK_USART = 72 MHz

Baud rate		CK_USART = 72 MHz			
No	KBps	Actual	BRD/16	BRD	Error rate
1	2.4	2.4	1875	30000	0%
2	9.6	9.6	468.75	7500	0%
3	19.2	19.2	234.375	3750	0%
4	57.6	57.6	78.125	1250	0%
5	115.2	115.2	39.0625	625	0%
6	230.4	230.769	19.5	312	0.16%
7	460.8	461.538	9.75	156	0.16%
8	921.6	923.076	4.875	78	0.16%
9	2250	2250	2	32	0%
10	4500	4500	1	16	0%

IrDA Mode

The USART IrDA mode is provided for half-duplex point-to-point wireless communication.

The USART module includes an integrated modulator and demodulator which allows for wireless communication using infrared transceivers. The Transmitter specifies a data '0' as a 'high' pulse and a data '1' as a 'low' level while the Receiver specifies a data '0' as a 'low' pulse and a data '1' as a 'high' level in the IrDA mode. The IrDA mode provides two operation modes, one is the normal mode and the other is the low-power mode.

For the IrDA normal mode, the width of each transmitted pulse generated by the transmitter modulator is specified as 3/16 of the baud rate clock period. The received pulse width for the IrDA receiver demodulator is based on the IrDA receive debounce filter which is implemented using an 8-bit down-counting counter. The debounce filter counter value is specified by the IrDAPSC field in the IrDACR register. When a falling edge is detected on the UR_RX pin, the debounce filter counter starts to count down, driven by the CK_USART clock. If a rising edge is detected on the UR_RX pin, the counter stops counting and is reloaded with the IrDAPSC value. When a low pulse falling edge on the UR_RX pin is detected and then before the debounce filter has counted down to zero, a rising edge is also detected, then this low pulse will be considered as glitch noise and will be discarded. If a low pulse falling edge appears on the UR_RX pin but no rising edge is detected before the debounce counter reaches 0, then the input on the USART receiver pin is regarded as a valid data "0" for this bit duration. The IrDAPSC value must be set to be greater than or equal to 0x01, then the IrDA receiver demodulation operation can function properly. The IrDAPSC value can be adjusted to meet the USART baud rate setting to filter the IrDA received glitch noise of which the width is smaller than the prescaler setting duration.

In the IrDA low-power mode, the transmitted pulse width generated by the transmitter modulator is not kept at 3/16 of the baud rate clock period. Instead, the pulse width is fixed and is calculated by the following formula. The transmitted pulse width can be adjusted by the IrDAPSC field to meet the minimum pulse width specification of the external IrDA Receiver device.

$$T_{IrDA\_L} = 3 \times IrDAPSC / CK\_USART$$

NOTE: TIrDA_L is the IrDA transmitted pulse width in the low power mode.
The IrDAPSC field is the IrDA prescaler value in the IrDA Control Register IrDACR.

The debounce behavior in the IrDA low-power receiving mode is similar to the IrDA normal mode. For glitch detection, the low pulse of which the pulse width is shorter than 1 x (IrDAPSC / CK_USART) should be discarded in the IrDA receiver demodulation. A valid low data is accepted if its low pulse width is greater than 2 x (IrDAPSC / CK_USART) duration.

The IrDA physical layer specification specifies a minimum delay with a value of 10 ms between the transmission and reception and this IrDA receiver set-up time should be managed by the software.

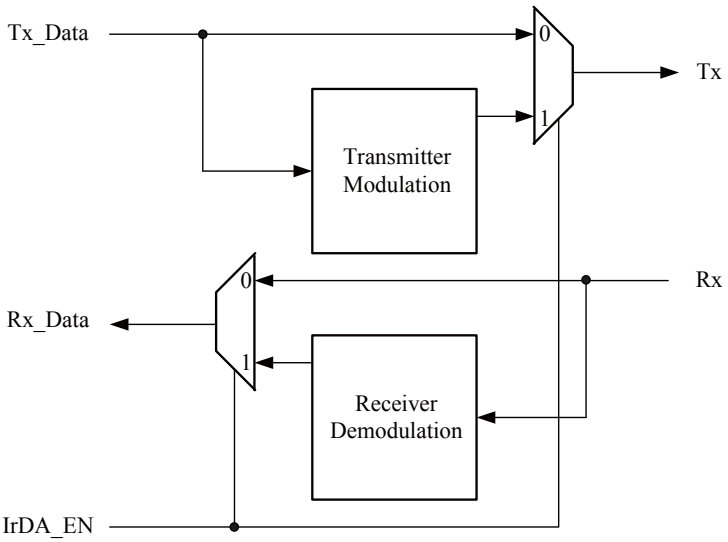


Figure 94. USART I/O and IrDA Block Diagram

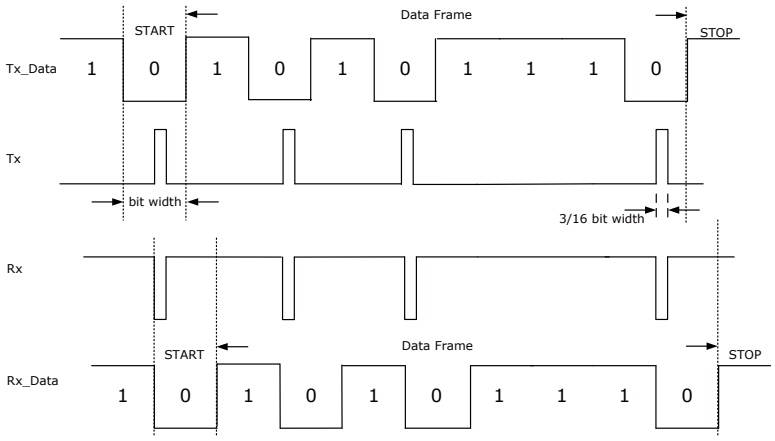


Figure 95. IrDA Modulation and Demodulation

RS485 Mode

The data on the RS485 interface is transmitted over a 2-wire twisted pair bus. The RS485 transceiver interprets the voltage levels of the differential signals with respect to a third common voltage. Without this common reference, the transceiver may interpret the differential signals incorrectly. This enhances the noise rejection capabilities of the RS485 interface. The UR_RTS pin is used to control the external RS485 transceiver whose polarity can be selected by configuring the TXENP bit in the RS485 Control Register, named RS485CR, when the USART module operates in the RS485 mode.

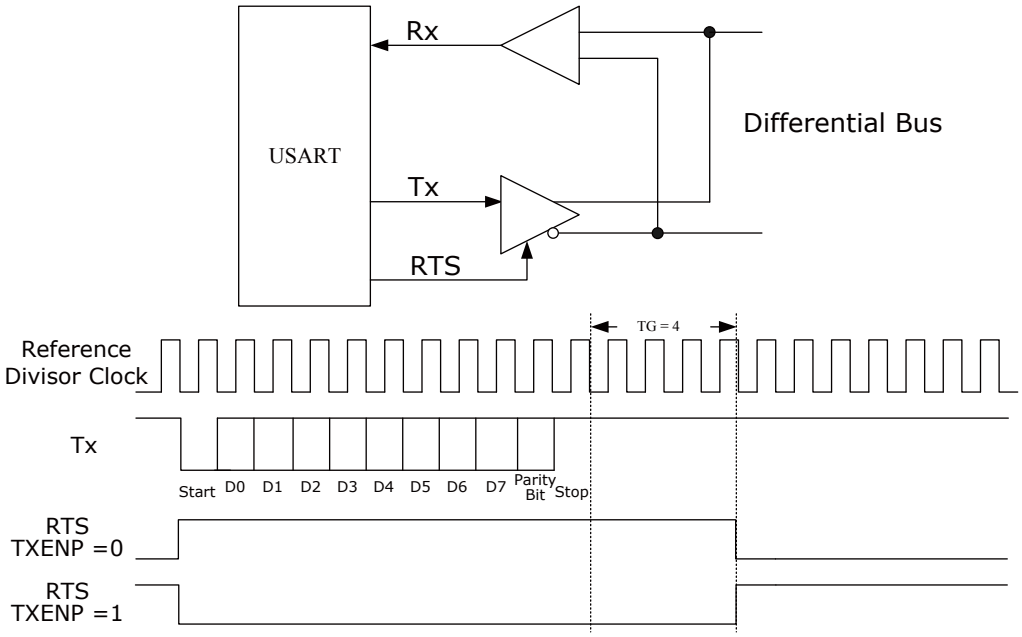
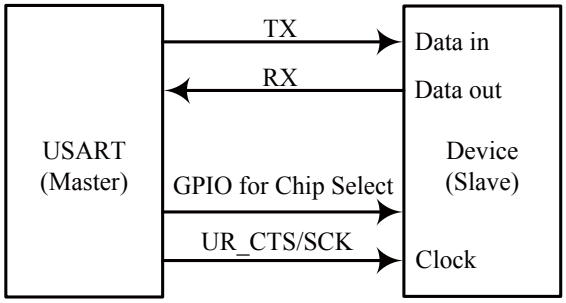


Figure 96. RS485 Interface and Waveform

Synchronous Mode

The data is transmitted in a full-duplex style in the USART Synchronous Master Mode, i.e., data transmission and reception both occur at the same time and only support the master mode. The USART UR_CTS/SCK pin is the synchronous USART transmitter clock output. In this mode, no clock pulses will be sent to the UR_CTS pin during the start bit, parity bit and stop bit duration. The CPS bit in the Synchronous Control Register, SYNCR, can be used to determine whether data is captured on the first or the second clock edge. The CPO bit in the SYNCR Register can be use to configure the clock polarity in the USART Synchronous Mode idle state. Detailed timing information is shown in the accompanying diagram.

In the USART synchronous Mode, the UR_CTS/SCK clock output pin is only used to transmit the data to the slave device. If the transmission data register, TBR, is written with valid data, the USART synchronous mode will automatically transmit this data with the corresponding clock output and the USART receiver will also receive data on the USART_RX pin. Otherwise, the receiver will not obtain synchronous data if no data is transmitted.



NOTE: The USART supports the synchronous master mode only. It can not receive or send data related to an input clock. The USART clock is always an output.

Figure 97. USART Synchronous Transmission Example

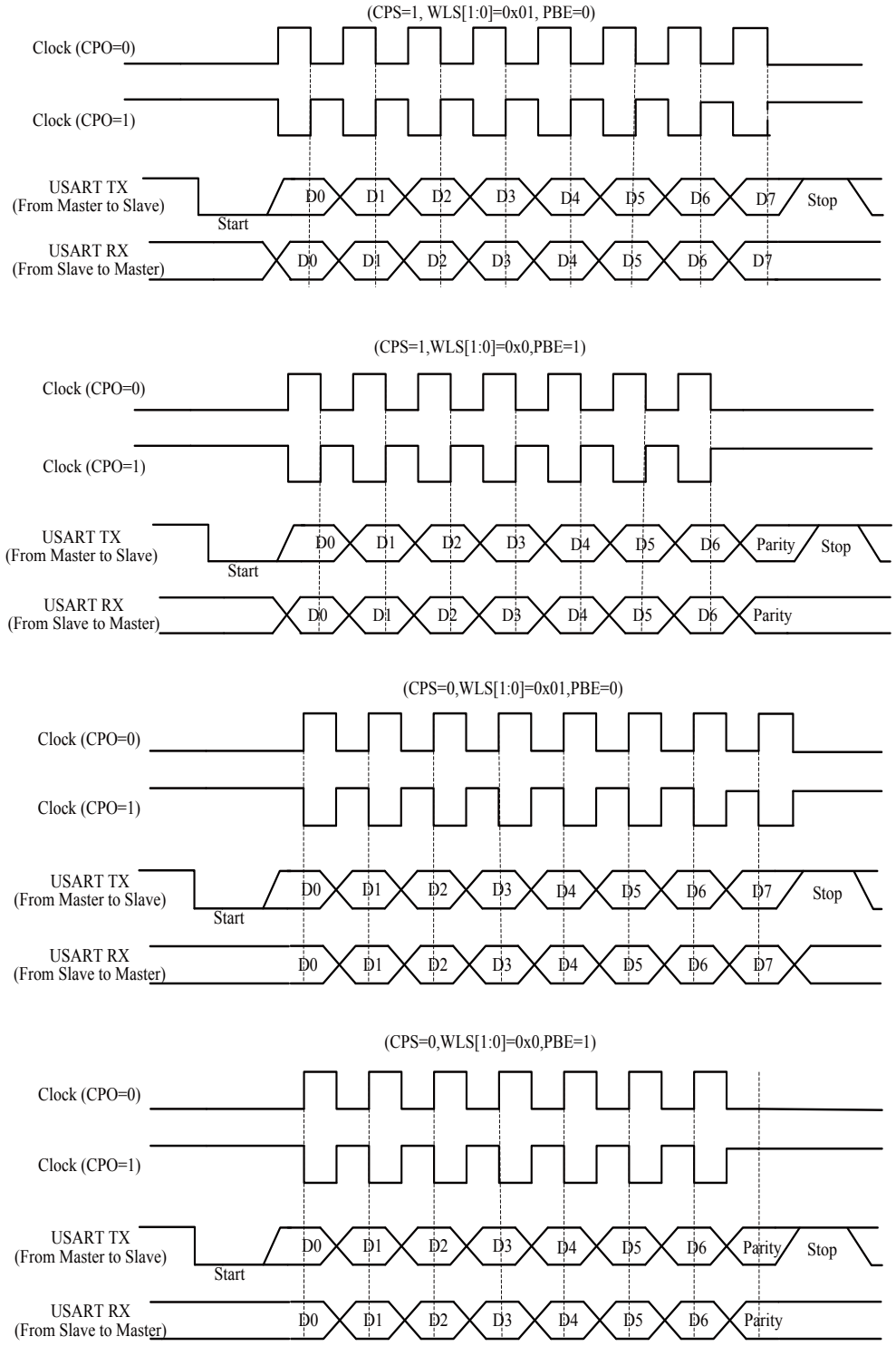


Figure 98. 8-bit Format USART Synchronous Waveform

Interrupts and Status

The USART module can generate an interrupt when the following events occurs.

- Receiver Line Status Interrupt (Irpt_RLSI): Occurrence of USART overrun error, parity error, framing error or break event.
- Receiver FIFO Threshold Level Interrupt (Irpt_RFTLI): When the FIFO received data amount has reached the specified threshold level.
- Receiver FIFO Time-out Interrupt (Irpt_RTOI): When the USART receiver FIFO does not receive a new data package during the specified time-out interval.
- Transmitter FIFO Threshold Level Interrupt (Irpt_TFTLI): When the data to be transmitted in the USART transmitter FIFO is less than the specified threshold level.
- MODEM Status Interrupt (Irpt_MODSI): When the DCD, RI, DSR or CTS bit states in the MODSR register have changed.

Register Map

The following table shows the USART registers and their reset values.

Table 44. Register Map of USART

Register	Offset	Description	Reset Value
USART Base Address = 0x4000_0000			
RBR	0x000	Receiver Buffer Register	0x0000_0000
TBR	0x000	Transmitter Buffer Register	0x0000_0000
IER	0x004	Interrupt Enable Register	0x0000_0000
IIR	0x008	Interrupt Identification Register	0x0000_0001
FCR	0x00C	FIFO Control Register	0x0000_0001
LCR	0x010	Line Control Register	0x0000_0000
MODCR	0x014	Modem Control Register	0x0000_0000
LSR	0x018	Line Status Register	0x0000_0060
MODSR	0x01C	Modem Status Register	0x0000_0000
TPR	0x020	Timing Parameter Register	0x0000_0000
MDR	0x024	Mode Register	0x0000_0000
IrDACR	0x028	IrDA Control Register	0x0000_0000
RS485CR	0x02C	RS485 Control Register	0x0000_0000
SYNCR	0x030	Synchronous Control Register	0x0000_0000
DEGTSTR	0x034	Debug/Test Register	0x0000_0000
DLR	0x038	Divider Latch Register	0x0000_0010

Register Descriptions

Receiver Buffer Register (RBR)

The register is used to store the USART received data.

Offset: 0x000

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							RD
Type/Reset								RO 0
	7	6	5	4	3	2	1	0
	RD							
Type/Reset	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0

Bits	Field	Descriptions
[8:0]	RD	Reading the data via this receiver buffer register will return the data from the receiver FIFO. The receiver FIFO has a capacity of up to 16 x 9 bits. By reading this register, the USART will return 7, 8 or 9-bit received data. The RD field bit 8 is valid for the 9-bit mode only and is fixed at 0 for the 8-bt mode. For the 7-bit mode, the receiver buffer register RD [6:0] contain the available bits.

Transmitter Buffer Register (TBR)

The register is used to specify the USART transmitted data.

Offset: 0x000

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							TD
Type/Reset								WO 0
	7	6	5	4	3	2	1	0
	TD							
Type/Reset	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0

Bits	Field	Descriptions
[8:0]	TD	Writing data to this transmitter buffer register will load data into the transmitter FIFO. The transmitter FIFO has a capacity of up to 16 x 9 bits. By writing to this register, the USART will send out 7, 8 or 9-bit transmitted data. The TD field bit 8 is valid for the 9-bit mode only and will be ignored for the 8-bit mode. For the 7-bit mode, the transmitter buffer register TD [6:0] contains the available bits.

Interrupt Enable Register (IER)

This register is used to enable or disable the related USART interrupt function. The USART module generates interrupts to the controller when the corresponding events occur and the corresponding interrupt enable bits are set.

Offset: 0x004

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved				MODSIE	RLSIE	TFTLIE	RFTLI_RTOIE
Type/Reset					RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[3]	MODSIE	MODEM Status Interrupt Enable (Irpt_MODSI) 0: Mask Irpt_MODSI 1: Enable Irpt_MODSI
[2]	RLSIE	Receiver Line Status Interrupt Enable (Irpt_RLSI) 0: Mask Irpt_RLSI 1: Enable Irpt_RLSI
[1]	TFTLIE	Transmitter FIFO Threshold Level Interrupt (Irpt_TFTLI) Enable 0: Mask Irpt_TFTLI 1: Enable Irpt_TFTLI
[0]	RFTLI_RTOIE	Receiver FIFO Threshold Level Interrupt Enable (Irpt_RFTLI) or receiver FIFO Time-Out Interrupt Enable (Irpt_RTOI) 0: Mask Irpt_RFTLI and Irpt_RTOI 1: Enable Irpt_RFTLI or Irpt_RTOI

Interrupt Identification Register (IIR)

This register is used to identify the interrupt source including the FIFO threshold and USART Receiver/ Transmitter status.

Offset: 0x008

Reset value: 0x0000_0001

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved				IID			NIP
Type/Reset					RO 0	RO 0	RO 0	RO 1

Bits	Field	Descriptions
[3:1]	IID	Interrupt Identification. The detailed Interrupt descriptions are shown in the accompanying table. IID and NIP indicate the current USART interrupt request.
[0]	NIP	No Interrupt Pending 1: No pending USART interrupt. 0: Pending USART interrupts.

Table 45. USART Interrupt Control Function

IID & NIP	Priority	Interrupt Type	Interrupt Source	Interrupt Reset control
xxx1	NA	None	None	NA
0110	Highest	Receiver Line Status Interrupt (Irpt_RLSI)	USART overrun error, parity error, framing error or break event occurs.	Reading the LSR register.
0100	Second	Receiver FIFO Threshold Level Interrupt (Irpt_RFTLI)	Receiver FIFO threshold level has been reached	Read the RBR register to decrease the receiver FIFO level to less than the specified threshold.
1100	Second	Receiver FIFO Time-out Interrupt (Irpt_RTOI)	Receiver FIFO is not empty and no activities have occurred in the receiver FIFO during the RTOIC time-out duration	Reading the RBR register
0010	Third	Transmitter FIFO Threshold Level Interrupt (Irpt_TFTLI)	Transmitter FIFO level is less than the transmitter FIFO threshold level which is set by the TFTL field in the FIFO Control Register named FCR.	Writing data into the TBR register.
0000	Fourth	MODEM Status Interrupt (Irpt_MODSI)	The DCDS, RIS, DSRS, or CTSS bits in the MODSR register have changed state.	Reading the MODSR register. - optional

FIFO Control Register (FCR)

This register specifies the FIFO control and configurations including threshold level and reset function.

Offset: 0x00C

Reset value: 0x0000_0001

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								

	7	6	5	4	3	2	1	0
	RFTL		TFTL		Reserved	TFR	RFR	FME
Type/Reset	RW 0	RW 0	RW 0	RW 0		WO 0	WO 0	RO 1

Bits	Field	Descriptions
[7:6]	RFTL	RX FIFO Threshold Level Setting The RFTL field defines the RX FIFO trigger level. 00: 1 byte 01: 4 bytes 10: 8 bytes 11: 14 bytes
[5:4]	TFTL	TX FIFO Threshold Level Setting The TFTL field determines the TX FIFO trigger level. 00: 0 byte 01: 2 bytes 10: 4 bytes 11: 8 bytes
[2]	TFR	TX FIFO Reset Setting this bit will generate a reset pulse to reset the TX FIFO which will empty the TX FIFO. i.e., the TX pointer will be reset to 0, after a reset signal. This bit returns to 0 automatically after the reset pulse is generated.
[1]	RFR	RX FIFO Reset Setting this bit will generate a reset pulse to reset the RX FIFO which will empty the RX FIFO. i.e., the RX pointer will be reset to 0, after a reset signal. This bit returns to 0 automatically after the reset pulse is generated.
[0]	FME	FIFO Mode Enable Because the USART module is always operated in the FIFO mode, writing to this bit will have no effect.

Line Control Register (LCR)

The line control register specifies the serial parameters such as the data length, parity bit and stop bit for the USART module.

Offset: 0x010

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved	BCB	SPE	EPE	PBE	NSB		WLS
Type/Reset		RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[6]	BCB	Break Control Bit When this bit is set to 1, the serial data output on the UR_TX pin will be forced to the Spacing State (logic 0). This bit acts only on UR_TX output pin and has no effect on the transmitter logic.
[5]	SPE	Stick Parity Enable 0: Disable stick parity 1: Stick Parity bit is transmitted This bit is only available when the PBE bit is set to 1. If both the PBE and SPE bits are set to 1 and the EPE bit is cleared to 0, the transmitted parity bit will be set to 1. However, when the PBE and SPE bits are set to 1 and also the EPE bit is set to 1, the transmitted parity bit will be cleared to 0.
[4]	EPE	Even Parity Enable 0: Odd number of logic 1's are transmitted or checked in the received data word and parity bits. 1: Even number of logic 1's are transmitted or checked in the received data word and parity bits. This bit is only available when the PBE bit is set to 1.
[3]	PBE	Parity Bit Enable 0: Parity bit is not generated (transmitted data) or checked (received data) during transfer. 1: Parity bit is generated or checked during transfer. **NOTE:** When the WLS field is set to "10" to select the 9-bit data format, writing to the PBE bit has no effect.
[2]	NSB	Number of STOP bits 0: One STOP bits is generated for the transmitted data 1: Two STOP bits are generated when either an 8- or 9-bit word length is selected.
[1:0]	WLS	Word Length Select 00: 7 bits 01: 8 bits 10: 9 bits 11: Reserved

Modem Control Register (MODCR)

This register contains a related modem control.

Offset: 0x014

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved						RTS	DTR
Type/Reset							RW 0	RW 0

Bits	Field	Descriptions
[1]	RTS	RTS - Request-To-Send Signal 0: Drive RTS pin to logic 1 1: Drive RTS pin to logic 0
[0]	DTR	DTR - Data-Terminal-Ready Signal 0: Drive DTR pin to logic 1 1: Drive DTR pin to logic 0

Line Status Register (LSR)

This register contains the corresponding USART status.

Offset: 0x018

Reset value: 0x0000_0060

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								

	7	6	5	4	3	2	1	0
	ERRRX	TXEMPT	TXFEMPT	BII	FEI	PEI	OEI	RFDR
Type/Reset	RC 0	RO 1	RO 1	RC 0	RC 0	RC 0	RC 0	RO 1

Bits	Field	Descriptions
[7]	ERRRX	RX FIFO Error 0: RX FIFO operating normally 1: There is at least one parity error (PE), framing error (FE), or break indication (BI) in the receiver FIFO. ERR_RX is cleared when the CPU reads the LSR register and if there are no subsequent errors in the RX FIFO
[6]	TXEMPT	Transmitter Empty 0: Either the Transmitter FIFO (TX FIFO) or the Transmitter Shift Register (TSR) is not empty. 1: Both the TX FIFO and the TSR register are empty.
[5]	TXFEMPT	Transmitter FIFO Empty 0: TX FIFO is not empty. 1: TX FIFO is empty. The TXFEMPT bit is set when the last data package in the TX FIFO is transferred to the Transmitter Shift Register (TSR). This bit is reset when the TBR (or TX FIFO) is loaded with new data. This bit also causes the USART to issue an interrupt (Irpt_TFTLI) to the CPU when the TFTLIE bit in the IER register is set to 1 to enable the relevant interrupt and when the TFTL field in the FCR register is set to the value 0.
[4]	BII	Break Interrupt Indicator This bit is set to 1 whenever the received data input is held in the "spacing state" (logic 0) for longer than a full word transmission time, which is the total time of "start bit" + “data bits” + “parity” + “stop bits” duration, and is reset whenever the CPU reads the contents of this LSR register.
[3]	FEI	Framing Error Indicator This bit is set to 1 whenever the received character does not have a valid "stop bit", which means the stop bit following the last data bit or parity bit is detected as a logic 0, and is reset whenever the CPU reads the contents of this LSR register.
[2]	PEI	Parity Error Indicator This bit is set to 1 whenever the received character does not have a valid "parity bit" and is reset whenever the CPU reads the contents of this LSR register.

Bits	Field	Descriptions
[1]	OEI	Overrun Error Indicator An overrun error will occur only after the RX FIFO is full and when the next character has been completely received into the RX shift register. The character in the shift register is overwritten when an overrun event occurs, but it is not transferred to the RX FIFO. The OEI bit is used to indicate to the CPU as soon as it happens and is reset whenever the CPU reads the contents of this LSR register.
[0]	RFDR	RX FIFO Data Ready 0: RX FIFO is empty 1: RX FIFO contains at least 1 received data word.

Modem Status Register (MODSR)

This register contains the modem status bits.

Offset: 0x01C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								

	7	6	5	4	3	2	1	0
	DCDS	RIS	DSRS	CTSS	DDCD	DRI	DDSR	DCTS
Type/Reset	RO 0	RO 0	RO 0	RO 0	RC 0	RC 0	RC 0	RC 0

Bits	Field	Descriptions
[7]	DCDS	UR_DCD - Data-Carrier-Detect Status 0: UR_DCD pin is inactive 1: UR_DCD pin is active and kept at 0
[6]	RIS	UR_RI Ring-Indicator Status 0: UR_RI pin is inactive 1: UR_RI pin is active and kept at 0
[5]	DSRS	UR_DSR Data-Set-Ready Status 0: UR_DSR pin is inactive 1: UR_DSR pin is active and kept at 0
[4]	CTSS	UR_CTS Clear-To-Send Status 0: UR_CTS pin is inactive 1: UR_CTS pin is active and kept at 0
[3]	DDCD	Detect UR_DCD Status Change This bit is set whenever the UR_DCD input pin status has been changed and will be reset if the CPU reads the MODSR register. When the DDCD bit is set to 1, a modem status Interrupt is generated if the MODSIE bit in the IER register is set to 1.
[2]	DRI	Detect UR_RI Status Change This bit is set whenever the UR_RI input pin status has been changed and will be reset if the CPU reads the MODSR register. When the DIR bit is set to 1, a modem status Interrupt is generated if the MODSIE bit in the IER register is set to 1.
[1]	DDSR	Detect UR_DSR Status Change This bit is set whenever the UR_DSR input pin status has been changed and will be reset if the CPU reads the MODSR register. When the DDSR bit is set to 1, a modem status Interrupt is generated if the MODSIE bit in the IER register is set to 1.
[0]	DCTS	Detect UR_CTS Status Change This bit is set whenever the UR_CTS input pin status has been changed and will be reset if the CPU reads the MODSR register. When the DCTS bit is set to 1, a modem status Interrupt is generated if the MODSIE bit in the IER register is set to 1.

Timing Parameter Register (TPR)

This register contains the USART timing parameters including the transmitter time guard parameters and the receiver FIFO time-out value together with the RX FIFO time-out interrupt enable control.

Offset: 0x020

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	Reserved							
Type/Reset								
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	TG							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	RTOIE	RTOIC						
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:8]	TG	Transmitter Time Guard The transmitter time guard counter is driven by the baud rate clock. When the TX FIFO transmits data, the counter is reset and then starts to count. Only when the counter content is equal to the TG value, are further word transmission transactions allowed.
[7]	RTOIE	Receiver FIFO Time Out Interrupt Enable The receiver FIFO time-out interrupt is enabled only when the RFTLI_RTOIE bit in the IER register is set to 1.
[6:0]	RTOIC	Receiver FIFO Time-Out Interrupt Compare value The RX FIFO time-out counter, TOUT_CNT, is driven by the baud rate clock. When the RX FIFO receives new data, the counter is reset and then starts to count. Once the time-out counter content is equal to the time-out interrupt compare RTOIC value, a receiver FIFO time-out interrupt, Irpt_RTOI, is generated if the RFTLI_RTOIE bit in the IER register is set to 1. New received data or the empty RX FIFO after being read will clear the RX FIFO time-out counter.

Mode Register (MDR)

This register specifies the USART mode and the data transfer mode selections.

Offset: 0x024

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved					TRSM		MODE
Type/Reset						RW 0	RW 0	RW 0

Bits	Field	Descriptions
[2]	TRSM	Transfer Mode Selection This bit is used to select the data transfer protocol. 0: LSB first 1: MSB first
[1:0]	MODE	USART Mode Selection. 00: Normal operation 01: IrDA 10: RS485 11: Synchronous

IrDA Control Register (IrDACR)

This register specifies the corresponding enable control and mode selections for the IrDA mode operation.

Offset: 0x028

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	IrDAPSC							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	Reserved				LB	TXSEL	IrDALP	IrDAEN
Type/Reset					RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:8]	IrDAPSC	IrDA Prescaler value This field contains the 8-bit debounce prescaler value. The debounce count-down counter is driven by the USART clock, named as CK_USART. The counting period is specified by the IrDAPSC field. The IrDAPSC field must be set to a value equal to or greater than 0x01 to for normal debounce counter operation. If the pulse width is less than the duration specified by the IrDAPSC field, the pulse will be considered as glitch noise and discarded. 00000000: Reserved – can not be used. 00000001: CK_USART clock divided by 1 00000010: CK_USART clock divided by 2 00000011: CK_USART clock divided by 3 ...
[3]	LB	IrDA Loop Back Mode 0: Disable IrDA loop back mode 1: Enable IrDA loop back mode for self testing
[2]	TXSEL	Transceiver Select 0: Enable IrDA receiver 1: Enable IrDA transmitter
[1]	IrDALP	IrDA Low Power Mode Select the IrDA operation mode. 0: Normal mode 1: IrDA low power mode
[0]	IrDAEN	IrDA Enable control 0: Disable IrDA mode 1: Enable IrDA mode

RS485 Control Register (RS485CR)

This register contains the UR_RTS/TXE pin polarity for the RS485 mode.

Offset: 0x02C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved							TXENP
Type/Reset								RW 0

Bits	Field	Descriptions
[0]	TXENP	UR_RTS/TXE pin Polarity 0: UR_RTS/TXE is active high inthe RS485 transmission mode 1: UR_RTS/TXE is active low in the RS485 transmission mode.

Synchronous Control Register (SYNCR)

This register is used to control the synchronous clock pin and the clock polarity together with the clock phase for the synchronous mode.

Offset: 0x030

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved				CPO	CPS	Reserved	CLKEN
Type/Reset					RW 0	RW 0		RW 0

Bits	Field	Descriptions
[3]	CPO	Clock Polarity Selects the polarity of the clock output on the UR_CTS/SCK pin in the synchronous mode. Works in conjunction with the CPS bit to specify the desired clock idle state. 0: UR_CTS/SCK pin idle state is low. 1: UR_CTS/SCK pin idle state is high.
[2]	CPS	Clock Phase This bit allows the user to select the phase of the clock output on the UR_CTS/SCK pin in the synchronous mode. Works in conjunction with the CPO bit to determine the data capture edge. 0: Data is captured on the first clock edge. 1: Data is captured on the second clock edge.
[0]	CLKEN	Clock Enable Enable/disable the UR_CTS/SCK pin. 0: UR_CTS/SCK pin disabled 1: UR_CTS/SCK pin enabled

Debug/Test Register (DEGTSTR)

This register controls the USART debug mode.

Offset: 0x034

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved						LBM	
Type/Reset							RW 0	RW 0

Bits	Field	Descriptions
[1:0]	LBM	Loopback Test Mode Select 00: Normal Operation 01: Reserved 10: Automatic Echo Mode 11: Loopback Mode

Divider Latch Register(DLR)

The register is used to determine the USART clock divided ratio to generate the appropriate baud rate.

Offset: 0x038

Reset value: 0x0000_0010

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	BRD							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	BRD							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	BRD	Baud Rate Divider These 16 bits define the USART clock divider ratio. Baud Rate = CK_USART / BRD where the CK_USART clock is the system clock connected to the USART module. The BRD field can be set from 16 to 65535.

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