Holtek 32-bit Microcontroller with ARM® Cortex™-M3 Core

HT32F1755/HT32F1765/HT32F2755
User Manual

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1 Introduction

Overview

This user manual provides detailed information including how to use the HT32F1755/1765/2755 series of devices, system and bus architecture, memory organization and peripheral instructions. The target audiences for this document are software developers, application developers and hardware developers. For more information regarding pin assignment, package and electrical characteristics, please refer to the HT32F1755/1765/2755 series datasheet.

The Holtek HT32F1755/1765/2755 series of devices are high performance, low power consumption 32-bit microcontrollers based on the ARM® Cortex™-M3 processor core. The Cortex™-M3 is a next generation processor core which is tightly coupled with a Nested Vectored Interrupt Controller (NVIC), SysTick timer and advanced debug support.

The HT32F1755/1765/2755 device operates at a frequency of up to 72MHz with a Flash accelerator to obtain maximum efficiency. It provides 128 kbytes of embedded Flash memory for code/data storage and up to 64 kbytes of embedded SRAM memory for system operation and application program usage. A variety of peripherals, such as ADC, I^2C, USART, SPI, PDMA, GPTM, MCTM, SCI, CSIF, USB 2.0 FS, SWJ-DP (Serial Wire/JTAG Debug Port), etc., are also implemented in the device series. Several power saving modes provide the flexibility for maximum optimization between wake-up latency and power consumption, an especially important consideration in low power applications.

The above features make the HT32F1755/1765/2755 device suitable for use in a wide range of applications, especially in areas such as white goods application control, power monitors, alarm systems, consumer products, handheld equipment, data logging applications, motor control, fingerprint recognition and so on.

Features

- Core
  - 32-bit ARM® Cortex™-M3 processor core
  - Up to 72MHz operating frequency
  - 1.25 DMIPS/MHz (Dhrystone 2.1)
  - Single-cycle multiplication and hardware division
  - Integrated Nested Vectored Interrupt Controller (NVIC)
  - 24-bit SysTick timer
- On-chip memory
  - 128KB on-chip Flash memory for instruction/data and options storage
  - Up to 64KB on-chip SRAM
  - Supports multiple boot modes
- Flash Memory Controller
  - Flash accelerator to obtain maximum efficiency
  - 32-bit word programming with ISP and IAP
  - Flash protection capability to prevent illegal access
- Reset and Clock Control Units
  - Supply supervisor: Power On Reset (POR), Brown Out Detector (BOD) and Programmable Low Voltage Detector (LVD)
  - External 4 to 16MHz crystal oscillator
  - External 32,768Hz crystal oscillator
  - Internal 8MHz RC oscillator trimmed to ±2% accuracy at 3.3V operating voltage and 25ºC operating temperature
  - Internal 32kHz RC oscillator
  - Integrated system clock PLL
  - Independent clock gating bits for peripheral clock sources
- Power management
  - Single 3.3V power supply: 2.7V to 3.6V
  - Integrated 1.8V LDO regulator for core and peripheral power supply
  - V_{BAT} battery power supply for RTC and backup registers
  - Three power domains: 3.3V, 1.8V and Backup
  - Four power saving modes: Sleep, Deep-Sleep1, Deep-Sleep2, Power-Down
- Analog to Digital Converter
  - 12-bit SAR ADC engine
  - Up to 1Msps conversion rate – 1μs at 56MHz, 1.17μs at 72MHz
  - 8 external analog input channels
  - Supply voltage range: 2.7V~3.6V
  - Conversion range: V_{REF+}~V_{REF-}
- Analog Operational Amplifier/Comparator
  - Two Operational Amplifiers or Comparator functions which are software configurable
  - Supply voltage range: 2.7V~3.6V

- I/O ports
  - Up to 80 GPIOs
  - Port A , Port B, Port C, Port D and Port E are mapped as 16 external interrupts – EXTI
  - Almost all I/O pins are 5V-tolerant except for pins shared with analog inputs
- PWM Generation and Capture Timers
  - Two 16-bit General-Purpose Timer – GPTM
  - Up to 4 Channels with PWM, compare output or input capture input for each GPTM
  - External trigger input
- Basic Function Timer – BFTM
  - Two 32-bit compare/match count-up counters – no I/O control features
  - One shot mode – counting stops after a match condition
  - Repetitive mode – restart counter after a match condition
- Motor Control Timer – MCTM
  - Single 16-bit up, down, up/down auto-reload counter
  - 16-bit programmable prescaler allowing dividing the counter clock frequency by any factor between 1 and 65536
  - Input Capture Function
  - Compare Match Output
  - PWM waveform generation with Edge-aligned and Center-aligned counting Modes
  - Single Pulse Mode Output
  - Complementary Outputs with programmable dead-time insertion
  - Encoder interface controller with two inputs using quadrature decoder
  - Supports 3-phase motor control and hall sensor interface
  - Break input to force the timer's output signals into a reset or fixed condition
- Watchdog Timer
  - 12-bit down-counting counters with 3-bit prescaler
  - Interrupt or reset event for the system
  - Programmable watchdog timer window function
  - Write protection function
- Real Time Clock
  - 32-bit up-counting counters with a programmable prescaler
  - Alarm function
  - Interrupt and Wake-up event
- Communication Interfaces
  - Two I^2C interfaces which support both master and slave modes with a frequency of up to 1MHz
  - Two SPI interfaces which support both master and slave modes with a frequency of up to 36MHz for the master and a frequency of up to 18MHz for the slave
  - Two USART interfaces operate at a frequency of up to 4.5MHz

- Smart Card Interface – SCI
  - Supports ISO 7816-3 Standard
  - Character transfer mode
  - Single transmit buffer and single receive buffer
  - 11-bit Elementary Time Unit (ETU) counter
  - 9-bit Guard Time counter – GT
  - 24-bit Waiting Time counter – WT
  - Parity generation and checking
  - Automatic character retry on parity error detection in transmission and reception modes
- Peripheral Direct Memory Access – PDMA
  - 12 channels with trigger source grouping
  - Transfer modes: single and block
  - Data Transfer Width: 8, 16, and 32-bit
  - Addressing modes: increment, decrement and fixed
  - 4 levels programmable channel priority
  - Auto reload mode
  - PDMA trigger sources: CSIF, ADC, SPI, USART, I^2C, GPTM, MCTM, SCI and software
- Universal Serial Bus Device Controller – USB
  - Complies with USB 2.0 full-speed (12Mbps) specification
  - On-chip USB full-speed transceiver
  - 1 control endpoint (EP0) for control transfer
  - 3 single-buffered endpoints for bulk and interrupt transfer
  - 4 double-buffered endpoints for bulk, interrupt and isochronous transfer
  - 1KB EP-SRAM used as the endpoint data buffers
- CMOS Sensor Interface – CSIF, HT32F2755 only
  - Up to 2048×2048 input resolution
  - Supports 8-bit YUV422 and Raw RGB formats
  - Up to 24MHz input pixel clock frequency
  - Multi VSYNC and HSYNC setting for image capture
  - Fractional hardware sub-sample function
  - Hardware windowing capture function
  - Dual FIFOs with a capacity of 8×32 bits which can be read by the PDMA or CPU
- Debug support
  - Serial Wire or JTAG Debug Port – SWJ-DP
  - 6 instruction comparator and 2 literal comparator for hardware breakpoint or code/literal patch
  - 4 comparators for hardware watchpoints
  - 1-bit asynchronous trace for serial wire debug mode – TRACESWO
- 48, 64, and 100-pin LQFP packages
- Operation temperature range: -40ºC to +85ºC

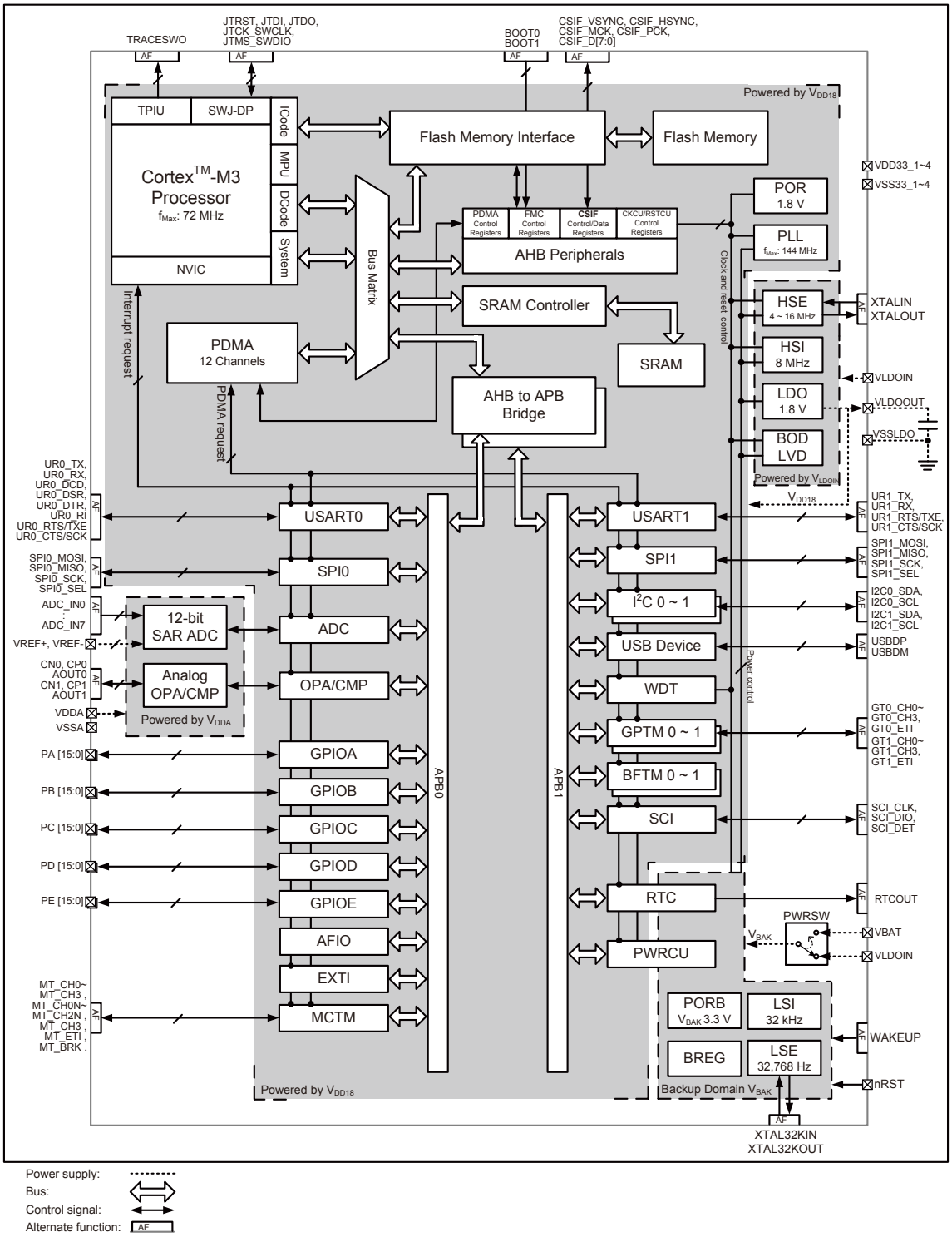
Device Information

Most features are common to all devices while the main features distinguishing them are CSIF, and SRAM memory capacities.

Table 1. HT32F1755/1765/2755 Series Features and Peripheral List

Peripherals		HT32F1755	HT32F1765	HT32F2755
Main Flash (KB)		127	127	127
Option Bytes Flash		1	1	1
SRAM (KB)		32	64	64
Times	MCTM	1		
	GPTM	2		
	BFTM	2		
	RTC	1		
	WDT	1		
Communication	CSIF	—	—	1
	USB	1		
	SCI	1		
	USART	2		
	SPI	2		
	I^2C	2		
GPIO		Up to 80		
EXTI		16		
12-bit ADC Number of channels		1		
		8 Channels		
OPA/Comparator		2		
CPU frequency		Up to 72MHz		
Operating voltage		2.7V~3.6V		
Operating temperature		-40°C ~+85°C		
Package		LQFP 48/64/100		

Block Diagram



Note: The AHB peripheral function, CSIF, only exists in the HT32F2755 device.

Figure 1. HT32F1755/1765/2755 Block Diagram

2 Document Conventions

The conventions used in this document are shown in the following table.

Table 2. Document Conventions

Notation	Example	Description
0x	0x5a05	The number string with a 0x prefix indicates a hexadecimal number.
0xnnnn_nnnn	0x2000_0100	32-bit Hexadecimal address or data.
b	b0101	The number string with a lowercase b prefix indicates a binary number.
NAME [n]	ADDR [5]	Specific bit of NAME. NAME can be a register or field of register. For example, ADDR [5] means bit 5 of ADDR register (field).
NAME [m:n]	ADDR [11:5]	Specific bits of NAME. NAME can be a register or field of register. For example, ADDR [11:5] means bit 11 to 5 of ADDR register (field).
X	b10X1	Don't care notation which means any value is allowed.
RW	19 SERDYIE RW 0 / 18 PLLRDYIE RW 0	Software can read and write to this bit.
RO	3 HSIRDY RO 1 / 2 HSERDY RO 0	Software can only read this bit. A write operation will have no effect.
RC	1 PDF RC 0 / 0 BAK_PORF RC 1	Software can only read this bit. Read operation will clear it to 0 automatically.
WC	3 SERDYF WC 0 / 2 PLLRDYF WC 0	Software can read this bit or clear it by writing 1. Writing 0 will have no effect.
WO	31 / 30 DB_CKSRC WO 0 WO 0	Software can only write to this bit. A read operation always returns 0.
Reserved	1 LLRDY RO 0 / 0 Reserved	Reserved bit(s) for future use. Data read from these bits is not well defined and should be treated as random data. Normally these reserved bits should be set to 0. Note that reserved bit must be kept at reset value.
Word		Data length of a word is 32-bit.
Half-word		Data length of a half-word is 16-bit.
Byte		Data length of a byte is 8-bit.

3 System Architecture

The system architecture of the HT32F1755/1765/2755 series of devices that includes the ARM® Cortex™-M3 processor, bus architecture and memory organization will be described in the following sections. The Cortex™-M3 is a next generation processor core which offers many new features. Integrated and advanced features make the Cortex™-M3 processor suitable for market products that require microcontrollers with high performance and low power consumption. In brief, The Cortex™-M3 processor includes three AHB-Lite buses known as ICode, DCode and System buses. All memory accesses of the Cortex™-M3 processor are executed on the three buses according to the different purposes and the target memory spaces. The memory organization uses a Harvard architecture, pre-defined memory map and up to 4GB of memory space, making the system flexible and extendable.

ARM® Cortex™-M3 Processor

The Cortex™-M3 is a general purpose 32-bit processor core especially suitable for products requiring high performance and low power consumption microcontrollers. It offers many new features such as a Thumb-2 instruction sets, hardware divider, low latency interrupt respond time, atomic bit-band access and multiple buses for simultaneous accesses. The Cortex™-M3 processor is based on the ARMv7 architecture and supports both Thumb and Thumb-2 instruction sets. Some system peripherals listed below are also provided by Cortex™-M3:

- Internal Bus Matrix connected with ICode bus, DCode bus, System bus, Private Peripheral Bus (PPB) and debug accesses (AHB-AP)
- Nested Vectored Interrupt Controller (NVIC)
- Flash Patch and Breakpoint (FPB)
- Data Watchpoint and Trace (DWT)
- Instrument Trace Macrocell (ITM)
- Memory Protection Unit (MPU)
- Serial Wire debug Port (SW-DP)
- Serial Wire JTAG Debug Port (SWJ-DP)
- Embedded Trace Macrocell (ETM)
- Trace Port Interface Unit (TPIU)

The following figure shows the Cortex™-M3 processor block diagram. For more information, refer to the ARM® Cortex™-M3 Technical Reference Manual.

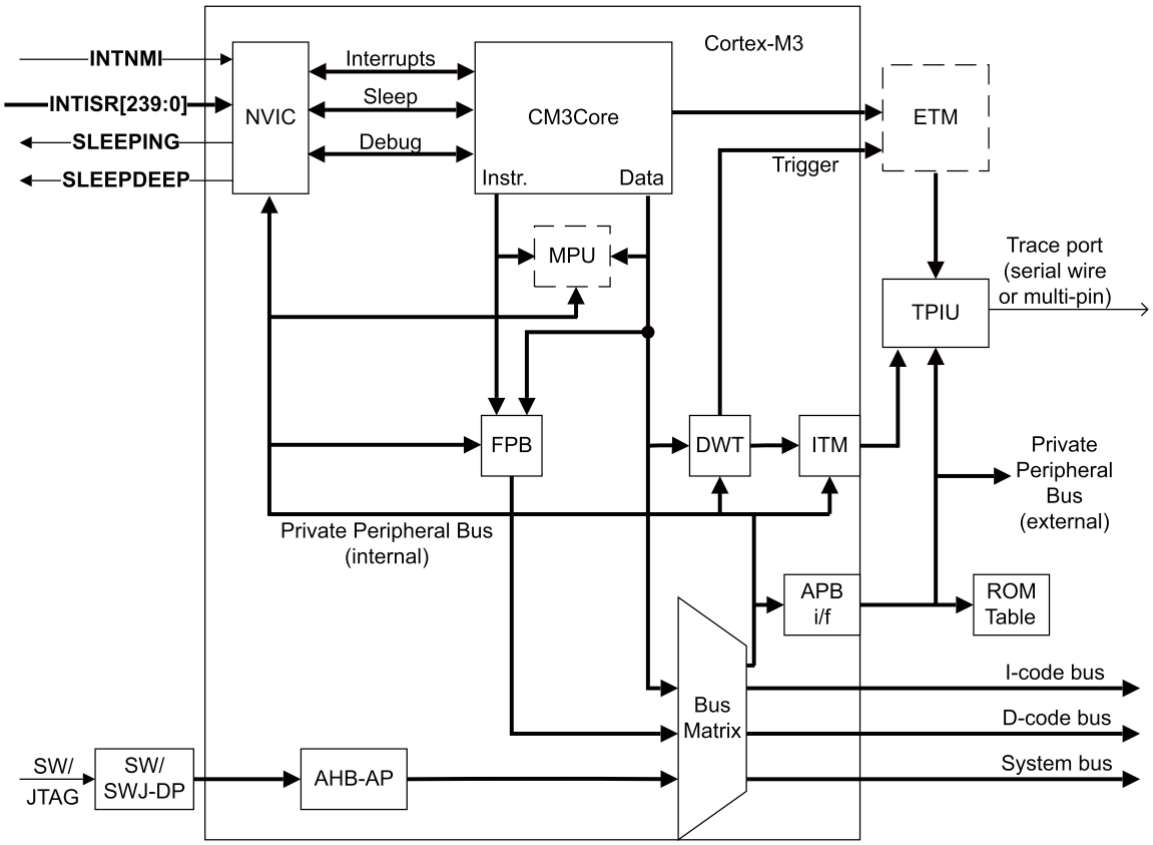


Figure 2. Cortex™-M3 Block Diagram

Bus Architecture

The HT32F1755/1765/2755 series consist of four masters and four slaves in the bus architecture. The Cortex™-M3 ICode, DCode, System bus and Peripheral Direct Memory Access (PDMA) are the masters while the internal SRAM access bus, the internal Flash memory access bus, the AHB peripherals access bus and the AHB to APB bridge are the slaves. The ICode bus is used for instruction and vector fetches from the Code region (0x0000_0000~0x1FFF_FFFF) to the Cortex™-M3 core. The DCode bus is used for loading/storing data and also for debug access of the Code region. Similarly, the System bus is used for instruction/vector fetches, data loading/storing and debugging access of the system regions. The system regions include the internal SRAM region and the peripheral region. All of the four master buses are based on 32-bit Advanced High-performance Bus-Lite (AHB-Lite) protocol. The following figure shows the bus architecture of the HT32F1755/1765/2755 series.

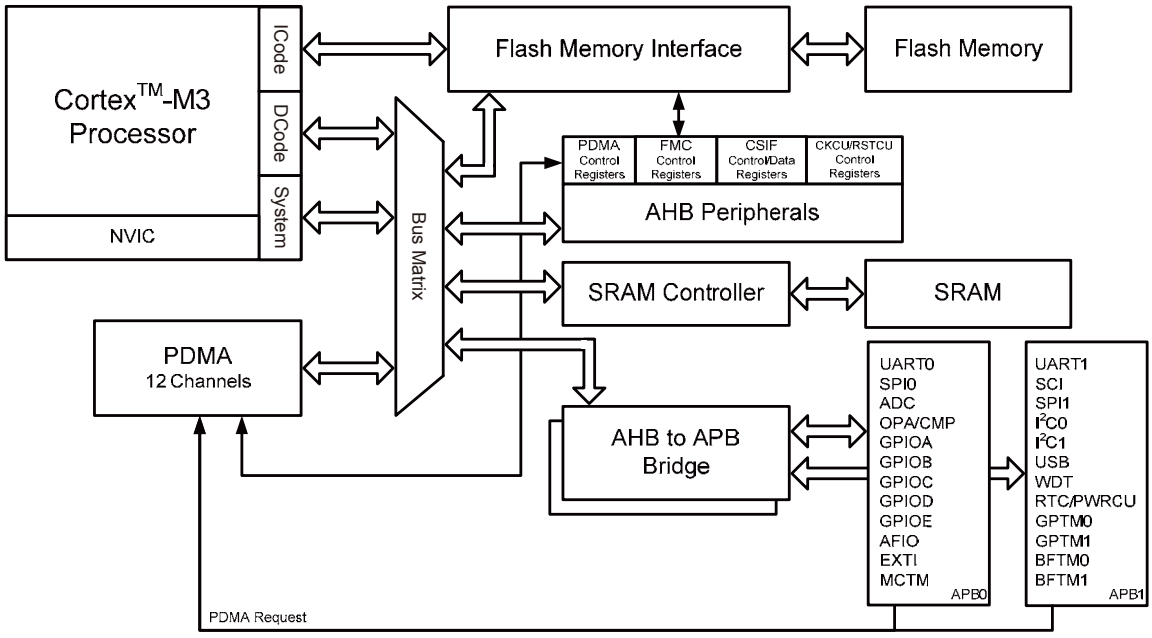
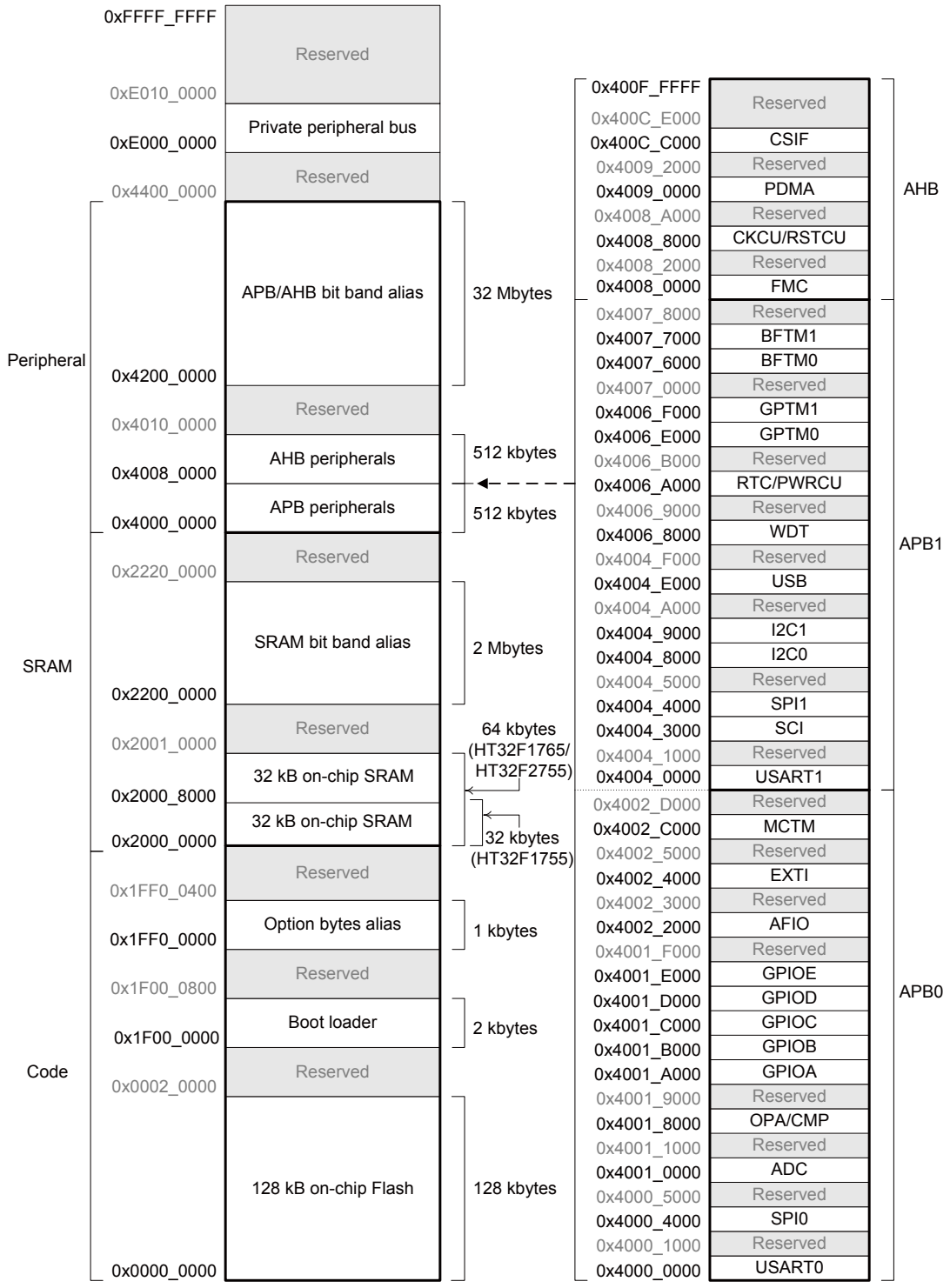


Figure 3. HT32F1755/1765/2755 Bus Architecture

Memory Organization

The ARM® Cortex™-M3 processor is structured in Harvard architecture which can use separate buses to fetch instructions and load/store data. The instruction code and data are both located in the same memory address space but in different address ranges. The maximum address range of the Cortex™-M3 is 4GB since it has 32-bit bus address width. Additionally, a pre-defined memory map is provided by the Cortex™-M3 processor to reduce the software complexity of repeated implementation of different device vendors. However, some regions are used by the ARM® Cortex™-M3 system peripherals. Refer to the ARM® Cortex™-M3 Technical Reference Manual for more information. The following figure shows the memory map of HT32F1755/1765/2755 series of devices, including Code, SRAM, peripheral, and other pre-defined regions.

Memory Map



Note: For HT32F1755, the SRAM memory space at 0x2000_8000 to 0x2000_FFFF is reserved.

Figure 4. HT32F1755/1765/2755 Memory Map

Table 3. HT32F1755/1765/2755 Register Map

Start Address	End Address	Peripheral	Bus	Register map
0x4000_0000	0x4000_0FFF	USART0	APB	
0x4000_1000	0x4000_3FFF	Reserved		
0x4000_4000	0x4000_4FFF	SPI0		
0x4000_5000	0x4001_FFFF	Reserved		
0x4001_0000	0x4001_0FFF	ADC		
0x4001_1000	0x4001_7FFF	Reserved		
0x4001_8000	0x4001_8FFF	OPA/Comparator		
0x4001_9000	0x4001_9FFF	Reserved		
0x4001_A000	0x4001_AFFF	GPIOA		
0x4001_B000	0x4001_BFFF	GPIOB		
0x4001_C000	0x4001_CFFF	GPIOC		
0x4001_D000	0x4002_DFFF	GPIOD		
0x4001_E000	0x4001_EFFF	GPIOE		
0x4001_F000	0x4002_1FFF	Reserved		
0x4002_2000	0x4002_2FFF	AFIO		
0x4002_3000	0x4002_3FFF	Reserved		
0x4002_4000	0x4002_4FFF	EXTI		
0x4002_5000	0x4002_BFFF	Reserved		
0x4002_C000	0x4002_CFFF	MCTM		
0x4002_D000	0x4003_FFFF	Reserved		
0x4004_0000	0x4004_0FFF	USART1		
0x4004_1000	0x4004_2FFF	Reserved		
0x4004_3000	0x4004_3FFF	SCI		
0x4004_4000	0x4004_4FFF	SPI1		
0x4004_5000	0x4004_7FFF	Reserved		
0x4004_8000	0x4004_8FFF	I^2C0		
0x4004_9000	0x4004_9FFF	I^2C1		
0x4004_A000	0x4004_DFFF	Reserved		
0x4004_E000	0x4004_EFFF	USB		
0x4004_F000	0x4006_7FFF	Reserved		
0x4006_8000	0x4006_8FFF	WDT		
0x4006_9000	0x4006_9FFF	Reserved		
0x4006_A000	0x4006_AFFF	RTC/PWRCU		
0x4006_B000	0x4006_DFFF	Reserved		
0x4006_E000	0x4006_EFFF	GPTM0		
0x4006_F000	0x4006_FFFF	GPTM1		
0x4007_0000	0x4007_5FFF	Reserved		
0x4007_6000	0x4007_6FFF	BFTM0		
0x4007_7000	0x4007_7FFF	BFTM1		
0x4007_8000	0x4007_FFFF	Reserved		

Start Address	End Address	Peripheral	Bus	Register map
0x4008_0000	0x4008_1FFF	FMC	AHB	
0x4008_2000	0x4008_7FFF	Reserved		
0x4008_8000	0x4008_9FFF	CKCU/RSTCU		
0x4008_A000	0x4008_FFFF	Reserved		
0x4009_0000	0x4009_1FFF	PDMA		
0x4009_2000	0x400C_BFFF	Reserved		
0x400C_C000	0x400C_DFFF	CSIF		
0x400C_E000	0x400F_FFFF	Reserved		

Embedded Flash Memory

HT32F1755/1765/2755 series of devices provide 128KB of on-chip flash memory which is located at address 0x0000_0000. It supports byte, half-word, and word access operations. Note that the flash memory only supports read operations for the Cortex™-M3 ICode or DCode bus access. Any write operations to the flash memory (via DCode bus) will cause a bus fault exception. The flash memory has a capacity of 128 pages. Each page has a memory capacity of 1KB and can be erased independently. A 32-bit programming interface provides the capability of changing bits from 1 to 0. A data storage or firmware upgrade can be implemented using several method such as In System Programming (ISP), In Application Programming (IAP) or In Circuit Programming (ICP). For more information refer to the Flash Memory Controller section.

Embedded SRAM Memory

The HT32F1765/2755 devices contain 64KB on-chip SRAM while the HT32F1755 device contains 32KB on-chip SRAM, which is located at address 0x2000_0000. They support byte, half-word and word access operations. In order to reduce the time of read-modify-write operations, the Cortex™-M3 provides a bit-band function to perform a single atomic bit operation. Users can modify a single bit in the SRAM bit-band region by accessing the corresponding bit-band alias. For more information about bit-band, refer to the ARM® Cortex™-M3 Technical Reference Manual. The following formulas and examples show how to access a bit in the bit-band region by calculating the bit-band alias.

```
Bit-band alias=Bit-band base+(byte offset*32)+(bit number*4)
```

For example, if you want to access bit 7 of address 0x2000_0200, the bit-band alias is:

```
Bit-band alias=0x2200_0000+(0x200*32)+(7*4)=0x2200_401C
```

Writing to address 0x2200_401C will cause bit 7 of address 0x2000_0200 change while a read to address 0x2200_401C will return 0x01 or 0x00 according to the value of bit 7 at the SRAM address 0x2000_0200.

AHB Peripherals

The address of the AHB peripherals ranges from 0x4008_0000 to 0x400F_FFFF. Some peripherals such as Clock Control Unit, Reset Control Unit and Flash Memory Controller are connected to the AHB bus directly. The AHB peripherals clocks are always enabled after a system reset. Access to registers for these peripherals can be achieved directly via the AHB bus. Note that all peripheral registers in the AHB bus support only word access.

APB Peripherals

The address of APB peripherals ranges from 0x4000_0000 to 0x4007_FFFF. An APB to AHB bridge provides access capability between the Cortex™-M3 and the APB peripherals. Additionally, the APB peripheral clocks are disabled after a system reset. Software must enable the peripheral clock by setting up the APBCCRn register in the Clock Control Unit before accessing the corresponding peripheral register. Note that the APB to AHB bridge will duplicate the half-word or byte data to word width when a half-word or byte access is performed on the APB peripheral registers. In other words, the access result of a half-word or byte access on the APB peripheral register will vary depending on the data bit width of the access operation on the peripheral registers.

4 Flash Memory Controller (FMC)

Introduction

The Flash Memory Controller, FMC, provides all the necessary functions, pre-fetch buffer and branch cache for the embedded on-chip Flash Memory. Since the access speed of the Flash Memory is slower than the CPU, a wide access interface with a pre-fetch buffer is provided for the Flash Memory in order to reduce the CPU waiting time which will cause CPU instruction execution delays. Flash Memory word program/page erase functions are also provided.

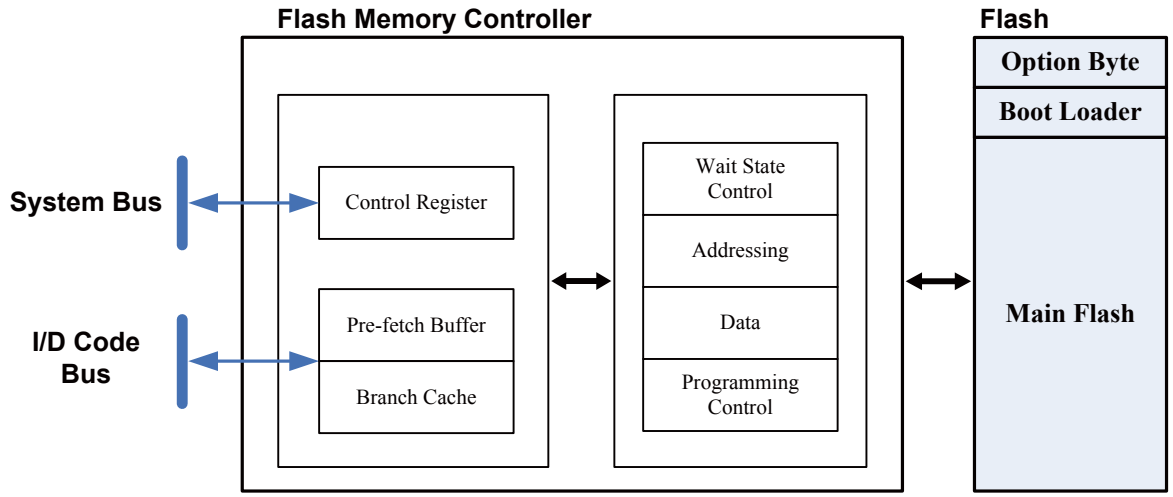


Figure 5. Flash Memory Controller Block Diagram

Features

- 128KB on-chip Flash memory for storing instruction/data and options
  - HT32F1755: 127KB + 1KB (instruction/data + option byte)
  - HT32F1765: 127KB + 1KB (instruction/data + option byte)
  - HT32F2755: 127KB + 1KB (instruction/data + option byte)
- Page size of 1KB – total of 128 pages
- Wide access interface with pre-fetch buffer and branch cache to reduce instruction gaps
- Page erase and mass erase capability
- 32-bit word programming
- Interrupt function to indicate end of Flash memory operations or an error occurs
- Flash read protection to prevent illegal code/data access
- Page erase/program protection to prevent unexpected operation

Functional Descriptions

Flash Memory Map

The following figure is the Flash memory map of the HT32F1755/1765/2755 devices in which the address ranges from 0x0000_0000 to 0x1FFF_FFFF (0.5GB). The address from 0x1F00_0000 to 0x1F00_07FF is mapped to the Boot Loader with a capacity of 2KB. Additionally, the region addressed from 0x1FF0_0000 to 0x1FF0_03FF is the Option Byte Block with a capacity of 1KB. The memory mapping on system view is shown as below.

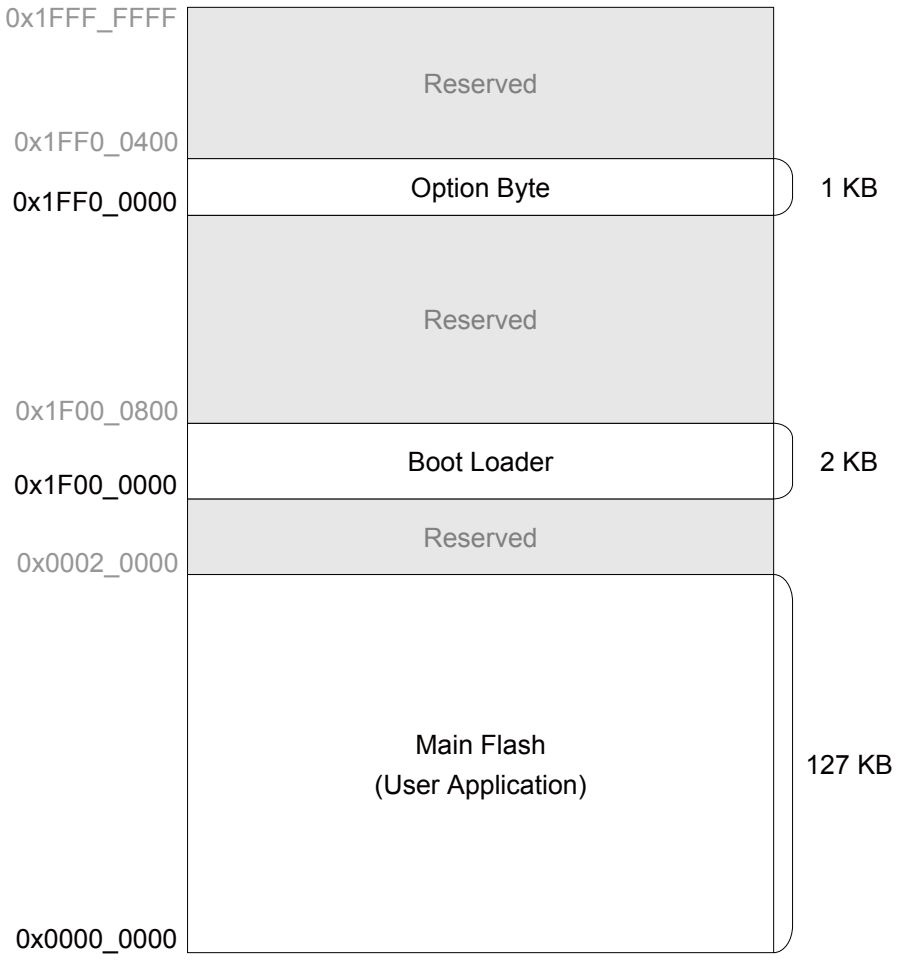


Figure 6. Flash Memory Map

Flash Memory Architecture

The Flash memory consists of 128KB Main Flash organized into 128 pages with 1KB capacity per page and a 2KB Information Block for the Boot Loader. The main Flash memory contains a total of 128 pages which can be erased individually. The following table shows the base address, size and protection setting bit of each page.

Table 4. Flash Memory and Option Byte

Block	Name	Address	Page Protection Bit	Size
Main Flash	Page 0	0x0000_0000~0x0000_03FF	OB_PP [0]	1KB
	Page 1	0x0000_0400~0x0000_07FF	OB_PP [1]	1KB
	Page 2	0x0000_0800~0x0000_0BFF	OB_PP [2]	1KB
	⋮	⋮	⋮	⋮
	Page 126	0x0001_F800~0x0001_FBFF	OB_PP [126]	1KB
	Option Byte	0x1FF0_0000~0x1FF0_03FF	OB_CP [1]	1KB
Information Block	Boot Loader	0x1F00_0000~0x1F00_07FF	NA	2KB

Note: The Information Block stores the boot loader – this block can not be programmed or erased by user.

Wait State Setting

When the CPU clock, HCLK, is greater than the access speed of the Flash memory, then wait state cycles must be inserted during the CPU fetch instructions or load data from Flash memory. The wait state can be changed by setting the WAIT [2:0] bits of the Flash Cache and Pre-fetch Control Register, CFCR. In order to match the wait state requirement, the following two rules should be considered.

- HCLK clock is switched from low to high frequency: Change the wait state setting first and then switch the HCLK clock.
- HCLK clock is switched from high to low frequency: Switch the HCLK clock first and then change the wait state setting.

The following table shows the relationship between the wait state cycle and the CPU clock HCLK. The default wait state is 0 since the High Speed Internal oscillator HSI which operates at a frequency of 8MHz is selected as the HCLK clock source after reset.

Table 5. Relationship between wait state cycle and HCLK

Wait State Cycle	HCLK
0	0MHz < HCLK ≤ 24MHz
1	24MHz < HCLK ≤ 48MHz
2	48MHz < HCLK ≤ 72MHz

Booting Configuration

The HT32F1755/1765/2755 devices provide three kinds of boot modes which can be selected using the BOOT0 and BOOT1 pins. The BOOT0 and BOOT1 pins are sampled during a power-on reset or a system reset. Once the logic value on these pins has been determined, the first 4 words of vector will be remapped to the corresponding source according to the boot mode. The boot modes are shown in the following table.

Table 6. Booting Modes

Booting mode selection pins		Mode	Descriptions
BOOT1	BOOT0		
0	0	SRAM	Vector source is SBVT0~SBVT3
0	1	Boot Loader	Vector source is Boot Loader
1	X	Main Flash	Vector source is Main Flash memory

The Vector Mapping Control Register (VMCR) is provided to change the vector remapping setting temporarily after a device reset. The initial reset value of the VMCR register is determined by the BOOT0 and BOOT1 pins which will be sampled during the reset duration.

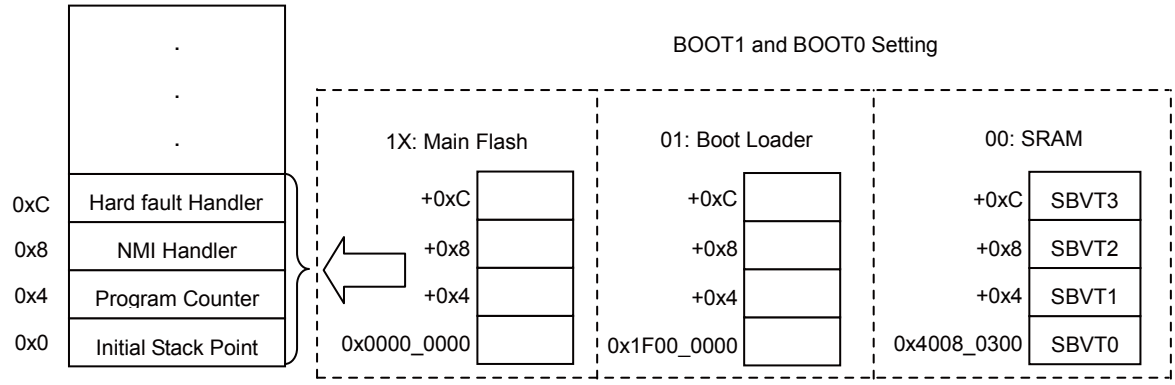


Figure 7. Vector Remapping

Page Erase

The FMC provides a page erase function which is used to initialize the contents of a Flash memory page to a high state. Each page can be erased independently without affecting the contents of other pages. The following steps show the access sequence of the register for a page erase operation.

- Check the OPCR register to confirm that no Flash memory operation is in progress (OPM [3:0] equal to 0xE or 0x6). Otherwise, wait until the previous operation has been finished.
- Write the page address into the TADR register.
- Write the page erase command into the OCMR register (CMD [3:0]=0x8).
- Send the page erase command to the FMC by setting the OPCR register (set OPM [3:0]=0xA).
- Wait until all the operations have been completed by checking the value of the OPCR register (OPM [3:0] equal to 0xE).
- Read and verify the page if required using DCODE access.

Note that a correct target page address must be confirmed. The software may run out of control if the target erase page is being used to fetch codes or to access data. The FMC will not provide any notification when this occurs. Additionally, the page erase operation will be ignored on protected pages. A Flash operation error interrupt will be triggered by the FMC if the OREIEN bit in the OIER register is set. The software can check the PPEF bit in the OISR register to detect this condition in the interrupt handler. The following figure shows the page erase operation flow.

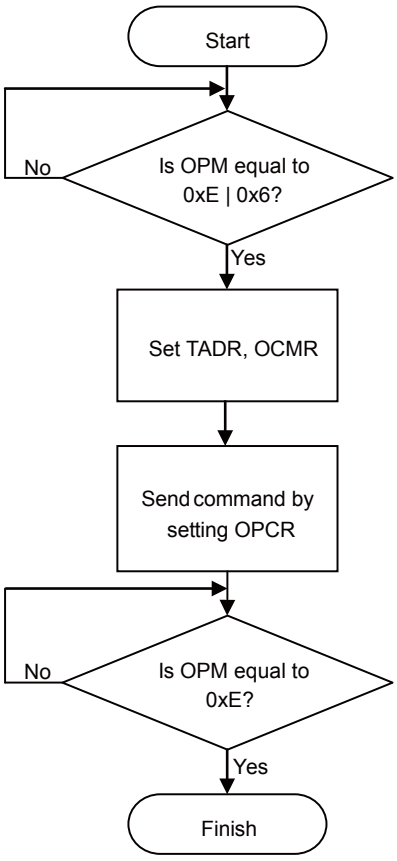


Figure 8. Page Erase Operation Flowchart

Mass Erase

The FMC provides a mass erase function which is used to initialize the complete Flash memory contents to a high state. The following steps show the mass erase operation register access sequence.

- Check the OPCR register to confirm that no Flash memory operation is in progress (OPM [3:0] equal to 0xE or 0x6). Otherwise, wait until the previous operation has been finished.
- Write the mass erase command into the OCMR register (CMD [3:0]=0xA).
- Send the mass erase command to the FMC by setting the OPCR register (set OPM [3:0]=0xA).
- Wait until all operations have been completed by checking the value of the OPCR register (OPM [3:0] equal to 0xE).
- Read and verify the Flash memory if required using DCODE access.

Since all Flash contents will be reset to the value of 0xFFFF_FFFF, the mass erase operation can be implemented by an application that runs in SRAM or by the debug tool that accesses the FMC registers directly. An application executes on the Flash memory will not trigger a mass erase operation. The following figure shows the mass erase operation flow.

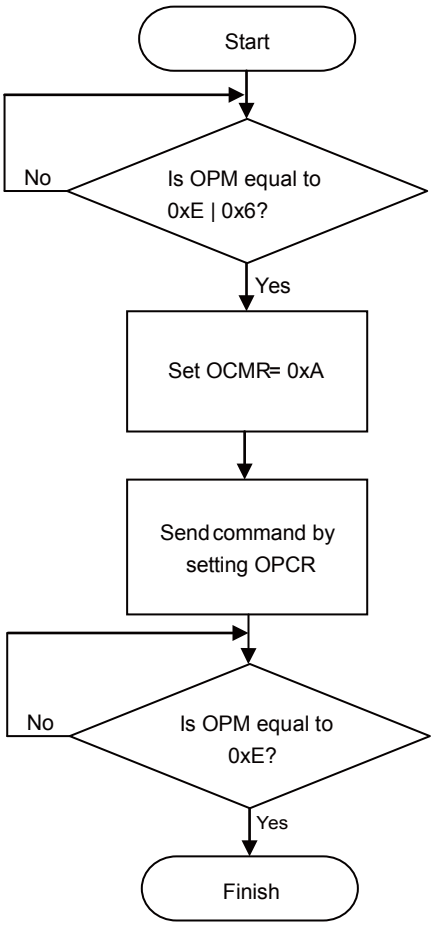


Figure 9. Mass Erase Operation Flowchart

Word Programming

The FMC provides a 32-bit word programming function which is used to modify the Flash memory contents. The following steps show the word programming operation register access sequence.

- Check the OPCR register to confirm that no Flash memory operation is in progress (OPM [3:0] equal to 0xE or 0x6). Otherwise, wait until the previous operation has been finished.
- Write the word address into the TADR register. Write the word data into the WRDR register.
- Write the word programming command into the OCMR register (CMD [3:0]=0x4).
- Send the word programming command to the FMC by setting the OPCR register (set OPM [3:0]=0xA).
- Wait until all operations have been completed by checking the value of the OPCR register (OPM [3:0] equal to 0xE).
- Read and verify the Flash memory if required using DCODE access.

Note that the word programming operation can not be applied to the same address twice. Successive word programming operations to the same address must be separated by a page erase operation. Additionally, the word programming operation will be ignored on protected pages. A Flash operation error interrupt will be triggered by the FMC if the OREIEN bit in the OIER register is set. The software can check the PPEF bit in the OISR register to detect this condition in the interrupt handler. The following figure shows the word programming operation flow.

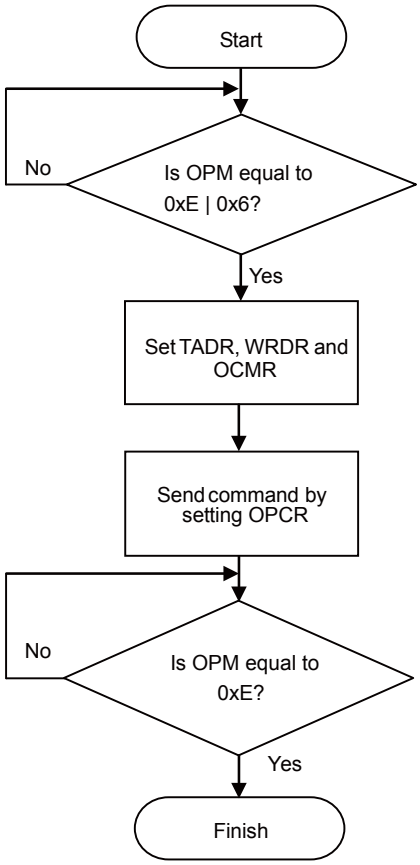


Figure 10. Word Programming Operation Flowchart

Option Byte Description

The Option Byte region can be treated as an independent Flash memory in which the base address is 0x1FF0_0000. The following table shows the functional description and the Option Byte memory map.

Table 7. Option Byte Memory Map

Option Byte	Offset	Description	Reset Value
Option Byte Base Address=0x1FF0_0000			
OB_PP	0x000 0x004 0x008 0x00C	OB_PP [n]: Main Flash Page Erase/Program Protection (n=0~126 for page 0~page 126) 0: Main Flash Page n Erase/Program Protection is enabled 1: Main Flash Page n Erase/Program Protection is disabled OB_PP [127]: Reserved	0xFFFF_FFFF 0xFFFF_FFFF 0xFFFF_FFFF 0xFFFF_FFFF
OB_CP	0x010	OB_CP [0]: Flash Security Protection 0: Flash Security protection is enabled 1: Flash Security protection is disabled OB_CP [1]: Option Byte Erase/Program Protection 0: Option Byte protection is enabled 1: Option Byte protection is disabled OB_CP [31:2]: Reserved	0xFFFF_FFFF
OB_CK	0x020	OB_CK [31:0]: Option Byte Checksum OB_CK should be set as the sum of the 5 words Option Byte content, of which the address offset ranges form 0x000 to 0x010 (0x000 + 0x004 + 0x008 + 0x00C + 0x010), when the content of the OB_PP or OB_CP register is not equal to 0xFFFF_FFFF.	0xFFFF_FFFF

Page Erase/Program Protection

The FMC provides page erase/program protection functions to prevent inadvertent operations on the Flash memory. The page erase or word programming command will not be accepted by the FMC on protected pages. When the page erase or word programming command is sent to the FMC on a protected page, the PPEF bit in the OISR register will then be set by the FMC. If the OREIEN bit in the OIER register is also set to 1 then the Flash operation error interrupt will be triggered by the FMC. The page protection function can be individually enabled for each page by configuring the OB_PP [126:0] bit field in the Option Byte. If a page erase operation is executed on the Option Byte region, all the Flash Memory page protection functions will be disabled. The page protection function of the Option Byte is enabled by clearing the OB_CP [1] bit to 0. Once the Option Byte has been protected, the only way to disable its protection function is to execute a mass erase operation. The following table shows the access permission of the Main Flash page when the page protection is enabled.

Table 8. Access Permission of Protected Main Flash Page

Mode / Operation	ISP/IAP	ICP/Debug mode	Boot from SRAM
DCODE Read	O	O	O
Program	X	X	X
Page Erase	X	X	X
Mass Erase	O	O	O

Notes: 1. The write protection setup is based on specific pages. The above access permission only affects the pages that the protection function has been enabled. Other pages are not affected.

2. The Main Flash page protection is configured by OB_PP [126:0]. The Option Byte page protection is configured by the OB_CP [1] bit.

The following steps show the page erase/program protection procedure register access sequence:

- Check the OPCR register to confirm that no Flash memory operation is in progress (OPM [3:0] equal to 0xE or 0x6). Otherwise, wait until the previous operation has been finished.
- Write the OB_PP address into the TADR register (TADR=0x1FF0_0000~0x1FF0_000C).
- Write the data which indicates the protection function of the corresponding page is enabled or disabled into the WRDR register (0: Enabled, 1: Disabled).
- Write the word programming command into the OCMR register (CMD [3:0]=0x4).
- Send the word programming command to the FMC by setting the OPCR register (set OPM [3:0]=0xA).
- Wait until all operations have been finished by checking the value of the OPCR register (OPM [3:0] equals to 0xE).
- Read and verify the OB_PP if required using DCODE access.
- Before to active the new OB_PP setting, the OB_CK must be updated according to the Option Byte checksum rule.
- Apply a system reset to active the new setting.

Security Protection

The FMC provides a security protection function to prevent illegal code/data access on the Flash memory. This function is useful for protecting the software/firmware from illegal users. The function is activated by configuring the OB_CP [0] bit in the Option Byte. Once the function has been enabled, all the main Flash DCODE access, programming and page erase operations will not be allowed except for the user's application. However, the mass erase operation will still be accepted by the FMC in order to disable this security protection function. The following table shows the access permission of Flash memory when the security protection is enabled.

Table 9. Access Permission When Security Protection Is Enabled

Operation \ Mode	User application(1)	ICP/Debug mode	Boot from SRAM
DCODE Read	O	X(2)	X(2)
Program	O(1)	X	X
Page Erase	O(1)	X	X
Mass Erase	O	O	O

Notes: 1. User application means the software that is executed or booted from the Main Flash memory with the JTAG/SW debugger disconnected. However the Option Byte and the page 0 are still protected in which Programming and Page Erase operations can not be executed.

2. When the JTAG/SW debugger is connected or the executing application is booted from SRAM, all the DCODE read operation to all Flash memory regions will return with the value of 0.

The following steps show the security protection procedure register access sequence:

- Check the OPCR register to confirm that no Flash memory operation is in progress (OPM [3:0] equal to 0xE or 0x6). Otherwise, wait until the pervious operation has been finished.
- Write the OB_CP address to the TADR register (TADR=0x1FF0_0010).
- Write the data into the WRDR register to clear OB_CP [0] bit to 0.
- Write the word programming command into the OCMR register (CMD [3:0]=0x4).
- Send the word programming command to the FMC by setting the OPCR register (set OPM=0xA).
- Wait until all operations have been finished by checking the value of the OPCR register (OPM [3:0] equals to 0xE).
- Read and verify the OB_CP if required using DCODE access.
- Before to activate the security protection function, the OB_CK field must be updated according to the Option Byte checksum rule.
- Apply a system reset to active the new setting.

Register Map

The following table shows the FMC registers and reset values.

Table 10. FMC Register Map

Register	Offset	Description	Reset Value
FMC Base Address=0x4008_0000			
TADR	0x000	Flash Target Address Register	0x0000_0000
WRDR	0x004	Flash Write Data Register	0x0000_0000
OCMR	0x00C	Flash Operation Command Register	0x0000_0000
OPCR	0x010	Flash Operation Control Register	0x0000_000C
OIER	0x014	Flash Operation Interrupt Enable Register	0x0000_0000
OISR	0x018	Flash Operation Interrupt Status Register	0x0001_0000
PPSR	0x020 0x024 0x028 0x02C	Flash Page Erase/Program Protection Status Register	0xXXXX_XXXX 0xXXXX_XXXX 0xXXXX_XXXX 0xXXXX_XXXX
CPSR	0x030	Flash Security Protection Status Register	0xXXXX_XXXX
VMCR	0x100	Flash Vector Mapping Control Register	0x0000_000X
CFCR	0x200	Flash Cache and Pre-fetch Control Register	0x0000_13D1
SBVT0	0x300	SRAM Booting Vector 0 (Stack Point)	0x2000_XX00
SBVT1	0x304	SRAM Booting Vector 1 (Program Counter)	0x2000_0101
SBVT2	0x308	SRAM Booting Vector 2 (NMI Handler)	0x0000_0000
SBVT3	0x30C	SRAM Booting Vector 3 (Hard Fault Handler)	0x0000_0000

Note: "X" means various reset values which depend on the Device, Flash value, option byte value, or power on reset setting.

Register Descriptions

Flash Target Address Register – TADR

This register specifies the target address of the page erase and word programming operations.

Offset: 0x000

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	TADB							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	TADB							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	TADB							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	TADB							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[31:0]	TADB	Flash Target Address Bits For programming operations, the TADR register specifies the address where the data is written. Since the programming length is 32 bits, TADR shall be set as word-aligned (4 bytes). The TADB [1:0] will be ignored during programming operations. For page erase operations, the TADR register contains the page address which is going to be erased. Since the page size is 1KB, TADB [9:0] will be ignored in order to limit the target address as 1KB-aligned. For 127KB Main Flash addressing, TADB [31:17] should be zero. The Option Byte which has a 1KB capacity ranges from 0x1FF0_0000 to 0x1FF0_03FF. This field is used to specify the Flash Memory address which must be within the range from 0x0000_0000 to 0x1FFF_FFFF. Otherwise, an Invalid Target Address interrupt will be generated if the corresponding interrupt enable bit is set.

Flash Write Data Register – WRDR

This register stores the data to be written into the TADR register for programming operations.

Offset: 0x004

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	WRDB							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	WRDB							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	WRDB							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	WRDB							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[31:0]	WRDB	Flash Write Data Bits The data value for programming operation.

Flash Operation Command Register – OCMR

This register is used to specify the Flash operation commands that include word program, page erase and mass erase.

Offset: 0x00C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved				CMD			
Type/Reset					RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[3:0]	CMD	Flash Operation Command The following table shows the definitions of the operation command bits CMD [3:0] which determine the Flash Memory operation. If an invalid command is set and the IOCMIEN bit is equal to 1, an Invalid Operation Command interrupt will occur.

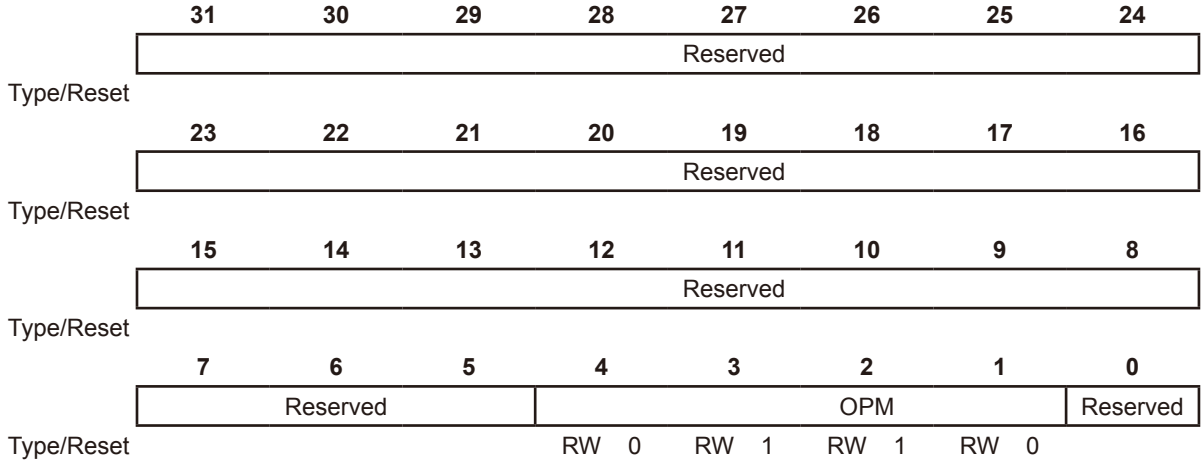
CMD [3:0]	Description
0x0	Idle - default
0x4	Word program
0x8	Page erase
0xA	Mass erase
Others	Reserved

Flash Operation Control Register – OPCR

This register is used for controlling the command commitment and checking the status of the FMC operations.

Offset: 0x010

Reset value: 0x0000_000C



Bits	Field	Descriptions
[4:1]	OPM	Operation Mode The following table shows the operation modes of the FMC. User can commit the command which is set by the OCMR register for the FMC according to the address alias setting in the TADR register. The contents of the TADR, WRDR, and OCMR registers should be prepared before setting this register. After all the operations have been finished, the OPM field will be set as 0xE by the FMC hardware. The Idle mode can be set when all the operations have been finished for power saving purposes. Note that the operation status should be checked before the next operation is executed on the FMC. The contents of the TADR, WRDR, OCMR, and OPCR registers should not be changed until the previous operation has been finished.

OPM [3:0]	Description
0x6	Idle (default)
0xA	Commit command to main Flash
0xE	All operation finished on main Flash
Others	Reserved

Flash Operation Interrupt Enable Register – OIER

This register is used to enable or disable the FMC interrupt function. The FMC generates interrupts to the controller when corresponding interrupt enable bits are set.

Offset: 0x014

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved			OREIEN	IOCMIEN	OBEIEN	ITADIEN	ORFIEN
Type/Reset				RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[4]	OREIEN	Operation Error Interrupt Enable 0: Operation Error interrupt is disabled 1: Operation Error interrupt is enabled
[3]	IOCMIEN	Invalid Operation Command Interrupt Enable 0: Invalid Operation Command interrupt is disabled 1: Invalid Operation Command interrupt is enabled
[2]	OBEIEN	Option Byte Check Sum Error Interrupt Enable 0: Option Byte Check Sum Error interrupt is disabled 1: Option Byte Check Sum Error interrupt is enabled
[1]	ITADIEN	Invalid Target Address Interrupt Enable 0: Invalid Target Address interrupt is disabled 1: Invalid Target Address interrupt is enabled
[0]	ORFIEN	Operation Finished Interrupt Enable 0: Operation Finish interrupt is disabled 1: Operation Finish interrupt is enabled

Flash Operation Interrupt and Status Register – OISR

This register indicates the FMC interrupt status which is used to check if a Flash operation has finished otherwise an error occurs. The status bits are available when the corresponding interrupt enable bits in the OIER register are set.

Offset: 0x018

Reset value: 0x0001_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved						PPEF	RORFF
Type/Reset							RO 0	RO 1
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved			OREF	IOCMF	OBEF	ITADF	ORFF
Type/Reset				WC 0	WC 0	WC 0	WC 0	WC 0

Bits	Field	Descriptions
[17]	PPEF	Page Erase/Program Protected Error Flag 0: Page Erase/Program Protected Error does not occur 1: Operation error occurs due to an invalid page erase/program operation being applied to a protected page This bit is reset by hardware once a new Flash operation command is committed.
[16]	RORFF	Raw Operation Finished Flag 0: The last Flash operation command has not yet finished 1: The last Flash operation command has finished This bit is directly connected to the Flash memory for debugging purpose.
[4]	OREF	Operation Error Flag 0: No Flash operation error occurred 1: The last Flash operation is failed This bit will be set when any Flash operation error occurs such as an invalid command, program error and erase error, etc. The ORE interrupt occurs if the OREIEN bit in the OIER register is set. Reset this bit by writing 1.
[3]	IOCMF	Invalid Operation Command Flag 0: No invalid Flash operation command was set 1: An invalid Flash operation command has been written to the OCMR register The IOCM interrupt will occur if the IOCMIEN bit in the OIER register is set. Reset this bit by writing 1.
[2]	OBEF	Option Byte Checksum Error Flag 0: Option Byte Checksum is correct 1: Option Byte Checksum is incorrect The OBE interrupt will occur if the OBEIEN bit in the OIER register is set. Reset this bit by writing 1.

Bits	Field	Descriptions
[1]	ITADF	Invalid Target Address Flag 0: The target address TADR is valid 1: The target address TADR is invalid The data in the TADR field must have a range from 0x0000_0000 to 0x1FFF_FFFF. An ITAD interrupt will occur if the ITADIEN bit in the OIER register is set. Reset this bit by writing 1.
[0]	ORFF	Operation Finished Flag 0: Flash operation has not finished 1: Last Flash operation has finished The ORF interrupt will occur if the ORFIEN bit in the OIER register is set. Reset this bit by writing 1.

Flash Page Erase/Program Protection Status Register – PPSR

This register indicates the page protection status of the Flash Memory.

Offset: 0x020~0x02C

Reset value: 0xXXXX_XXXX

	31	30	29	28	27	26	25	24
	PPSBn							
Type/Reset	RO X	RO X	RO X	RO X	RO X	RO X	RO X	RO X
	23	22	21	20	19	18	17	16
	PPSBn							
Type/Reset	RO X	RO X	RO X	RO X	RO X	RO X	RO X	RO X
	15	14	13	12	11	10	9	8
	PPSBn							
Type/Reset	RO X	RO X	RO X	RO X	RO X	RO X	RO X	RO X
	7	6	5	4	3	2	1	0
	PPSBn							
Type/Reset	RO X	RO X	RO X	RO X	RO X	RO X	RO X	RO X

Bits	Field	Descriptions
[126:0]	PPSBn	Page n Erase/Program Protection Status Bits (n=0~126) 0: The corresponding page n is protected 1: The corresponding page n is not protected The content of this register is not dynamically updated and will only be reloaded by the Option Byte loader which is activated when any kind of reset occurs. The erase or program function of the specific pages is not allowed when the corresponding bits of the PPSR registers are reset. The reset value of the bits PPSR [126:0] is determined by the Option Byte, OB_PP [126:0]. The other bits of the OB_PP and PPSR registers are reserved for future usage.

Flash Security Protection Status Register – CPSR

This register indicates the Flash Memory Security protection status. The content of this register is not dynamically updated and will only be reloaded by the Option Byte loader which is activated when any kind of reset occurs.

Offset: 0x030

Reset value: 0xXXXX_XXXX

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved						OBPSB	CPSB
Type/Reset							RO X	RO X

Bits	Field	Descriptions
[1]	OBPSB	Option Byte Page Erase/Program Protection Status Bit 0: The Option Byte page is protected 1: The Option Byte page is not protected The reset value of OPBSB is determined by the OB_CP [1] bit in the Option Byte.
[0]	CPSB	Flash Memory Security Protection Status Bit 0: Flash Memory Security protection is enabled 1: Flash Memory Security protection is disabled The reset value of the CPSB bit is determined by the OB_CP [0] bit in the Option Byte.

Flash Vector Mapping Control Register – VMCR

This register is used to control the vector mapping. The reset value of the VMCR register is determined by the status of the external booting pins, BOOT0 and BOOT1 during the power on reset period.

Offset: 0x100

Reset value: 0x0000_000X

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved						VMCB	
Type/Reset							RW X	RW X

Bits	Field	Descriptions
[1:0]	VMCB	Vector Mapping Control Bit The VMCB bits are used to control the mapping source of the first 4-word vectors addressed from 0x0 to 0xC. The following table shows the vector mapping setup.

BOOT1	BOOT0	VMCB [1:0]	Descriptions
Low	Low	00	SRAM booting mode The vector mapping source is SBVT0~3.
Low	High	01	Boot Loader mode The vector mapping source is the Boot Loader area.
High	Low	10	Main Flash mode The vector mapping source is the Main Flash Memory area.
High	High	11	

The reset value of the VMCR register is determined by the pins status of the external booting pins BOOT1 and BOOT0 during a power on reset and system reset. However, when the application program is executed, the vector mapping setting can be temporarily changed by configuring the VMCB bits to correctly access the first 4-word vectors in the Flash memory, especially when the CPU is booted from the Boot Loader or the SRAM region.

Flash Cache and Pre-fetch Control Register – CFCR

This register is used for controlling the FMC cache and pre-fetch module.

Offset: 0x200

Reset value: 0x0000_13D1

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	Reserved							FZWPSEN
Type/Reset								0
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	FHLAEN		Reserved	CE	Reserved			
Type/Reset	RW 0	0	0	RW 1	0	0	1	1
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	DCDB		Reserved	PFBE	Reserved	WAIT		
Type/Reset	RW 1	1	0	RW 1	0	RW 0	RW 0	RW 1

Bits	Field	Descriptions
[16]	FZWPSEN	Flash Zero Wait-state Power Saving Enable Bit 0: Flash zero wait-state power saving is disabled 1: Flash zero wait-state power saving is enabled This bit can only be set to 1 to reduce the Flash memory operating current when the Flash memory is operated in zero wait-state. This bit has no effect when the wait-state setting is changed to non-zero.
[15]	FHLAEN	Flash Memory Half-cycle Access Enable Bit 0: Half-cycle access is disabled 1: Half-cycle access is enabled This bit can only be set when the Flash memory is operated in zero wait-state. Setting this bit to 1 will reduce the Flash memory operation current further when the system frequency HCLK is less than a frequency of 12MHz. This bit has no effect when the wait-state setting is changed to non-zero.
[12]	CE	Branch Cache Enable Bit 0: Branch cache is disabled 1: Branch cache is enabled The branch cache is enabled in default state.
[7]	DCDB	DCODE data Cacheable Enable Bit 0: DCODE data is Cacheable 1: DCODE data is Non-cacheable The DCODE data is non-cacheable in default state.
[4]	PFBE	Pre-fetch Buffer Enable Bit 0: Pre-fetch buffer is disabled 1: Pre-fetch buffer is enabled The pre-fetch buffer is enabled in default state. When the pre-fetch buffer is disabled, the instruction and data are provided directly by the Flash memory.

Bits	Field	Descriptions
[2:0]	WAIT	Flash Wait-state Setting These bits are used to set the HCLK wait clock during a non-sequential Flash access. The actual value of the wait clocks is given by (WAIT [2:0]-1). Since a wide access interface with a pre-fetch buffer and branch cache is provided, the wait-state of sequential Flash access is very close to zero.

WAIT [2:0]	Wait Status	Allowed HCLK Range
001	0	0MHz < HCLK ≤ 24MHz
010	1	24MHz < HCLK ≤ 48MHz
011	2	48MHz < HCLK ≤ 72MHz
Others	Reserved	Reserved

SRAM Booting Vector Register n – SBVTn, n=0~3

These registers specify the initial values of the Stack Point, Program Counter, NMI handler address and Hard Fault handler address for the SRAM Booting mode.

Offset: 0x300~0x30C

Reset value: Various depending on the address offset

	31	30	29	28	27	26	25	24
	SBVTn							
Type/Reset	RW X	RW X	RW X	RW X	RW X	RW X	RW X	RW X
	23	22	21	20	19	18	17	16
	SBVTn							
Type/Reset	RW X	RW X	RW X	RW X	RW X	RW X	RW X	RW X
	15	14	13	12	11	10	9	8
	SBVTn							
Type/Reset	RW X	RW X	RW X	RW X	RW X	RW X	RW X	RW X
	7	6	5	4	3	2	1	0
	SBVTn							
Type/Reset	RW X	RW X	RW X	RW X	RW X	RW X	RW X	RW X

Bits	Field	Descriptions
[31:0]	SBVTn	SRAM Booting Vector n (n=0~3) The SRAM Booting Vector 0~3 provides a SRAM booting capability for application debugging. The contents of the SBVTn registers are re-mapped into the addresses 0x0 to 0xC of the Flash memory CODE area under the SRAM booting mode. Refer to the description of the VMCR register and BOOT1/BOOT0 boot pins. The following table shows the purpose and reset value of the SBVTn register. The reset value provides a fixed setting for program execution during the SRAM booting mode. These registers can be modified by the debugging tool in order to change the program execution setting. The reset values of the SBVTn register will be reloaded only by a power-on reset. Other reset sources will have no effect.

Name	Address Offset	Purpose Descriptions	Reset Value
SBVT0	0x300	Stack point	64KB SRAM: 0x2001_0000 32KB SRAM: 0x2000_8000
SBVT1	0x304	Program counter	0x2000_0151
SBVT2	0x308	NMI handler address	0x0000_0000
SBVT3	0x30C	Hard fault handler address	0x0000_0000

This access width of the registers SBVT0~SBVT3 must be 32-bit (Word access). 8 or 16-bit (Byte or Half-Word) access is not allowed.

5 Power Control Unit (PWRCU)

Introduction

The power consumption can be regarded as one of the most important issues for many embedded system applications. Accordingly the Power Control Unit, PWRCU, provides many types of power saving modes such as Sleep, Deep-Sleep1, Deep-Sleep2, and Power-Down modes. These modes reduce the power consumption and allow the application to achieve the best trade-off between the conflicting demands of CPU operating time, speed and power consumption. The dash line in the Figure 11 indicates the power supply source of three digital power domains.

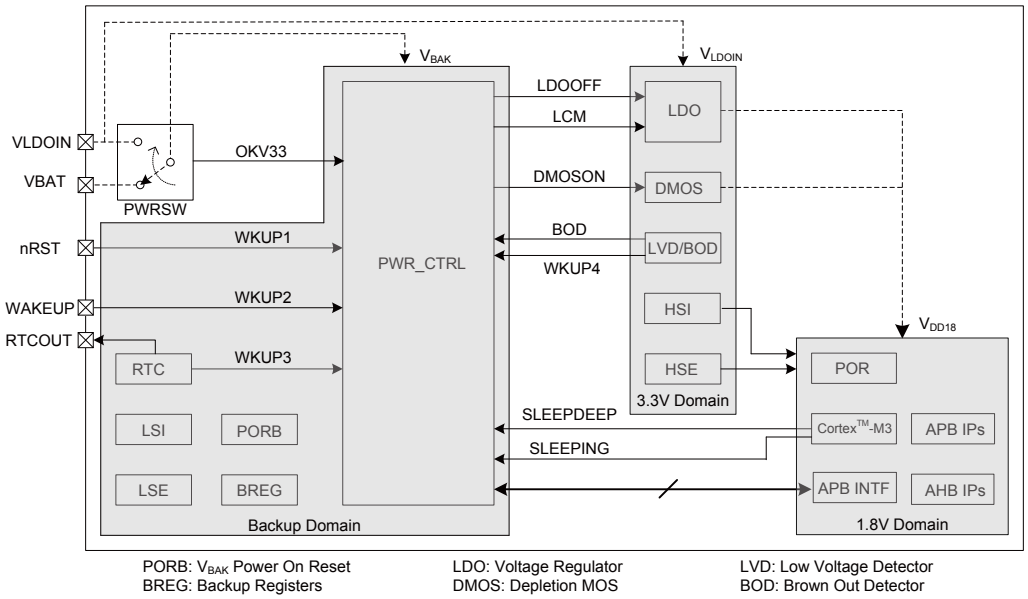


Figure 11. PWRCU Block Diagram

Features

- Three power domains: Backup, 3.3V and 1.8V power domains
- Four power saving modes: Sleep, Deep-Sleep1, Deep-Sleep2 and Power-Down modes
- Internal Voltage regulator supplies 1.8V voltage source
- Additional Depletion MOS supplies 1.8V voltage source with low leakage and low operating current
- Brown Out Detector can issue a system reset or an interrupt when 3.3V power source (V_{LDOIN}) is lower than 2.6V
- Low Voltage Detector can issue an interrupt or wake-up event when V_{LDOIN} is lower than a programmable threshold voltage ranging from 2.7V to 3.0V
- Battery power (V_{BAT}) for backup domain when V_{LDOIN} is shut down
- 40 bytes of backup registers powered by V_{BAK} for data storage of user application data when in the Power-Down mode

Functional Descriptions

Backup Domain

Power Switch

The Backup Domain is powered by the 3.3V power source, V_{LDOIN}, or the battery power source, V_{BAT}, which is selected by the power switch PWRSW. The operating voltage of the power switch ranges from 2.7V to 3.6V. If V_{LDOIN} is lower than V_{BAT}, then the power source will be switched from V_{LDOIN} to V_{BAT}. Therefore, even if V_{LDOIN} is powered down, all the circuitry in the backup domain can operate normally. This means that the backup register contents will be retained, the RTC circuitry will operate normally and the low speed oscillators can keep running.

Backup Domain Reset

The Backup Domain reset sources include the Backup Domain power-on-reset (PORB) and the Backup Domain software reset which is activated by setting the BAKRST bit in the BAKCR register. The PORB signal forces the device to stay in the reset mode until the V_{BAK} is greater than 1.36V. The slew rate of PORB signal is approximately V_{BAK}/100ms. Also the application software can trigger Backup Domain software reset by setting the BAKRST bit in the BAKCR register. All registers of PWRCU and RTC will be reset only by the Backup Domain reset.

LSE, LSI and RTC

The Real Time Clock circuitry clock source can be derived from either the Low Speed Internal RC oscillator, LSI, or the Low Speed External Crystal oscillator, LSE. Before entering the power saving mode by executing WFI/WFE instruction, the Cortex™-M3 needs to setup the compare register with an expected wake-up time and enable the wake-up function to achieve the RTC timer wake-up event. After entering the power saving mode for a certain amount of time, the Compare Match flag, CMFLAG, will be asserted to wake-up the device when the compare match event occurs. The details of the RTC configuration for wake-up timer will be described in the RTC chapter.

Backup Registers and Isolation Cells

Ten 32-bit registers, up to 40 bytes, are located in the Backup Domain for user application data storage. These registers are powered by V_{BAK} which constantly supplies power when the 1.8V power is switched off. The Backup Registers are only reset by the Backup Domain power-on-reset, PORB, or the Backup Domain software reset, BAKRST. When the device resumes operation from the 1.8V power, either by Hardware or Software, access to the Backup registers and the RTC registers are disabled by the isolation cells which protect these registers against possible parasitic write accesses. To resume access operations, users can disable these isolation cells by setting the BKISO bit in the LPCR register of the Clock Control Unit to 1.

LDO Power Control

The LDO will be automatically switched off when one of the following conditions occurs:

- The Power-Down or Deep-Sleep 2 mode is entered
- The control bits BODEN=1, BODRIS=0 and the supply power $V_{LDOIN} \leq 2.6V$

The LDO will be automatically switched on by hardware if any of the following conditions occurs:

- Resume operation from the power saving mode – RTC wake-up, LVD wake-up or WAKEUP pin rising edge
- Detect a falling edge on the external reset pin (nRST)
- The control bit BODEN=1 and the supply power $V_{LDOIN} > 2.6V$

To enter the Deep-Sleep1 mode, the PWRCU will request the LDO to operate in a low current mode, LCM. To enter the Deep-Sleep2 mode, the PWRCU will turn off the LDO and turn on the DMOS to supply an alternative 1.8V power.

3.3V Power Domain

Voltage Regulator

The voltage regulator, LDO, Depletion MOS, DMOS, Low voltage Detector, LVD, the Brown out Detector, BOD and High Speed Internal oscillator, HSI, all operate under the 3.3V power domain. The LDO can be configured to operate in either normal mode (LDOOFF=0, SLEEPDEEP=0, I=200mA) or low current mode (LDOOFF=0, SLEEPDEEP=1, I=100mA) to supply the 1.8V power. An alternative 1.8V power source is the output of the DMOS which has low leakage and drive current characteristics. It is controlled using the DMOSON bit in the BAKCR register. The DMOS output has weak drive current capability and can operate only in the Deep-Sleep2 mode for data retention purposes in the V_{DD18} power domain.

Low Voltage Detector/Brown Out Detector

The Brown Out Detector, BOD, is used to detect if the 3.3V supply voltage is equal to or lower than 2.6V. When the BODEN bit in the LVDCSR register is set to 1 and the 3.3V supply voltage is lower than 2.6V then the BODF flag is active. The PWRCU will regard this as a power down reset situation and then immediately disable the internal LDO regulator when the BODRIS bit is cleared to 0 or issue an interrupt to notify the Cortex™-M3 to execute a power down procedure when the BODRIS bit is set to 1. The Low Voltage Detector, LVD, can also detect whether the 3.3V supply voltage is lower than a programmable threshold voltage ranging from 2.7V to 3.0V. It is selected by the LVDS bits in the LVDCSR register. When a low voltage on the V_{LDOIN} power pin is detected, the LVDF flag will be active and an interrupt will be generated and sent to the Cortex™-M3 if the LVDEN and LVDIWEN bits in the LVDCSR register are set.

High Speed Internal Oscillator

The High Speed Internal Oscillator, HSI, is located in the 3.3V power domain. When exiting from the Deep-Sleep mode, the HSI clock will be configured as the system clock for a certain period by setting the PSRCEN bit to 1. This bit is located in the Global Clock Control Register, GCCR, in the Clock Control Unit, CKCU. The system clock will not be switched back to the original clock source used before entering the Deep-Sleep mode until the original clock source, which may be either sourced from the PLL or HSE, stabilizes. Also the system will force the HSI oscillator to be the system clock after a wake up from Power-Down mode since a 1.8V power on reset will occur.

1.8V Power Domain

The main functions that include the APB interface for the backup domain, 1.8V power on reset (POR), Cortex™-M3 logic, AHB/APB peripherals, and so on are located in this power domain. Once the 1.8V is powered up, the POR will generate a reset sequence (Refer to PORB) on the 1.8V power domain. Subsequently, to enter the expected power saving mode, the associated control bits including the LDOOFF, DMOSON, and SLEEPDEEP bits must be configured. Then, once a WFI or WFE instruction is executed, the device will enter an expected power saving mode which will be discussed in the following section.

Operation Modes

Run Mode

In the Run mode, the system operates with full functions and all power domains are active. There are two ways to reduce the power consumption in this mode. The first is to slow down the system clock by setting the AHBPRE field in the CKCU AHBCFGR register, and the second is to turn off the unused peripherals clock by setting the APBCCR0 and APBCCR1 registers. Reducing the system clock speed before entering the sleep mode will also help to minimize power consumption.

Additionally, there are several power saving modes to provide maximum optimization between device performance and power consumption.

Table 11. Operation Mode Definitions

Mode name	Hardware Action
Run	After system reset, Cortex™-M3 fetches instructions to execute.
Sleep	1. Cortex™-M3 core clock will be stopped. 2. Peripherals, Flash and SRAM clocks can be stopped.
Deep-Sleep	1. Stop all clocks in the 1.8V power domain. 2. Disable HSI, HSE, and PLL. 3. Reduce the 1.8V power domain current by turning on the LDO low current mode or DMOS.
Power-Down	Shut down the 1.8V power domain.

Sleep Mode

By default, only the Cortex™-M3 clock will be stopped in the Sleep mode. Clearing the SRAMEN bit in the CKCU AHBCCR register to 0 will have the effect of stopping the SRAM clock after the system enters the Sleep mode. If it is not necessary for the CPU to access SRAM in the Sleep mode, it is recommended to clear the SRAMEN bit in the AHBCCR register to minimize power consumption. To enter the Sleep mode, it is only necessary to clear the SLEEPDEEP bit to 0 and execute a WFI or WFE instruction. The system will exit from the Sleep mode via any interrupt or event trigger. The accompanying table provides more information about the power saving modes.

Table 12. Enter/Exit Power Saving Modes

Mode	Mode Entry				Mode Exit
	Cortex™-M3 Instruction	Cortex™-M3 SLEEPDEEP	LDOOFF	DMOSON	
Sleep	WFI or WFE (Takes effect)	0	X	X	WFI: Any interrupt WFE: Any wake-up event(1) or Any interrupt (NVIC on) or Any interrupt with SEVONPEND=1 (NVIC off)
Deep-Sleep1		1	0	0	Any EXTI in event mode or RTC wake-up or LVD wake-up(2) or Wake-up pin rising edge
Deep-Sleep2		1	X	1	RTC wake-up or LVD wake-up(2) or WAKEUP pin rising edge
Power-Down		1	1	0	RTC wake-up or LVD wake-up(2) or WAKEUP pin rising edge or External reset (nRST)

Notes: 1. Wake-up event means EXTI line in event mode, RTC, LVD, and WAKEUP pin rising edge.

2. If the system allows the LVD activity to wake it up after the system has entered the power saving mode, the LVDEWEN and LVDEN bits in the LVDCSR register must be set to 1 to make sure that the system can be woken up by a LVD event and then the LDO regulator can be turned on when system is woken up from the Deep-Sleep2 and Power-Down modes.

Deep-Sleep Mode

To enter Deep-Sleep mode, configure the registers as shown in the preceding table and execute the WFI or WFE instruction. In the Deep-Sleep mode, all clocks including PLL and high speed oscillator, known as HSI and HSE, will be stopped. In addition, Deep-Sleep1 turns the LDO into low current mode while Deep-Sleep2 turns off the LDO and uses a DMOS to keep 1.8V power. Once the PWRCU receives a wake-up event or an interrupt as shown in the preceding Mode-Exiting table, the LDO will then operate in normal mode and the high speed oscillator will be enabled. Finally, the Cortex™-M3 will return to Run mode to handle the wake-up interrupt if required. A Low Voltage Detection also can be regarded as a wake-up event if the corresponding wake-up control bit LVDEWEN in the LVDCSR register is enabled. The last wake-up event is a transition from low to high on the external WAKEUP pin sent to the PWRCU to resume from Deep-Sleep mode. During the Deep-Sleep mode, retaining the register and memory contents will shorten the wake-up latency.

Power-Down Mode

The Power-Down mode is derived from the Deep-Sleep mode of the Cortex™-M3 together with the additional control bits LDOOFF and DMOSON. To enter the Power-Down mode, users can configure the registers shown in the preceding Mode-Entering table and execute the WFI or WFE instruction. A RTC wake-up trigger event, a LVD wake-up, a low to high transition on the external WAKEUP pin or an external reset (nRST) signal will force the microcontroller out of the Power-Down mode. In the Power-Down mode, the 1.8V power supply will be turned off. The remaining active power supplies are the 3.3V I/O power (V_{DD33}) and the Backup Domain power (V_{BAK}).

After a system reset, the PORSTF bit in the RSTCU GRSR register, the PDF and BAKPORF bits in the BAKSR register should be checked by software to confirm if the device is being resumed from the Power-Down mode by a backup domain power on reset, an unexpected loss of the 1.8V power or other reset events (nRST, WDT, …). If the device has entered the Power-Down mode under the correct firmware procedure, then the PDF bit will be set. The System information could be saved in the Backup Registers and be retrieved when the 1.8V power domain is powered on again. More information about the PDF and BAKPORF bits in the BAKSR register and PORSTF bit in the RSTCU GRSR register is shown in the following table.

Table 13. Power Status After System Reset

BAKPORF	PDF	PORSTF	Description
1	0	1	Power-up for the first time after the backup domain is reset: Power on reset when V_{BAK} is applied for the first time or executing a software reset command on the backup domain.
0	0	1	Restart from unexpected loss of the 1.8V power or other reset (nRST, WDT, …).
0	1	1	Restart from the Power-Down mode.
1	1	x	Reserved

Register Map

The following table shows the PWRCU registers and reset values. Note all the registers in this unit are located in the V_{BAK} backup power domain.

Table 14. PWRCU Register Map

Register	Offset	Description	Reset Value
PWRCU Base Address=0x4006_A000			
BAKSR	0x100	Backup Domain Status Register	0x0000_0001
BAKCR	0x104	Backup Domain Control Register	0x0000_0000
BAKTEST	0x108	Backup Domain Test Register	0x0000_0027
HSIRCR	0x10C	HSI Ready Counter Control Register	0x0000_0003
LVDCSR	0x110	Low Voltage/Brown Out Detect Control and Status Register	0x0000_0000
BAKREG0	0x200	Backup Register 0	0x0000_0000
BAKREG1	0x204	Backup Register 1	0x0000_0000
BAKREG2	0x208	Backup Register 2	0x0000_0000
BAKREG3	0x20C	Backup Register 3	0x0000_0000
BAKREG4	0x210	Backup Register 4	0x0000_0000
BAKREG5	0x214	Backup Register 5	0x0000_0000
BAKREG6	0x218	Backup Register 6	0x0000_0000
BAKREG7	0x21C	Backup Register 7	0x0000_0000
BAKREG8	0x220	Backup Register 8	0x0000_0000
BAKREG9	0x224	Backup Register 9	0x0000_0000

Register Descriptions

Backup Domain Status Register – BAKSR

This register indicates backup domain status.

Offset: 0x100

Reset value: 0x0000_0001 (Reset only by Backup Domain reset)

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							WUPF
Type/Reset								RC 0
	7	6	5	4	3	2	1	0
	Reserved						PDF	BAKPORF
Type/Reset							RC 0	RC 1

Bits	Field	Descriptions
[8]	WUPF	External WAKEUP Pin Flag 0: The Wakeup pin is not asserted 1: The Wakeup pin is asserted This bit is set by hardware when the WAKEUP pin asserts and is cleared by a software read. Software should read this bit to clear it after a system wakes up from the power saving mode.
[1]	PDF	Power Down Flag 0: Wake-up from abnormal V_{DD18} shutdown (Loss of V_{DD18} is unexpected) 1: Wake-up from Power-Down mode. The loss of V_{DD18} is under expectation This bit is set by hardware when the system has successfully entered the Power-Down mode This bit is cleared by a software read.
[0]	BAKPORF	Backup Domain Reset Flag 0: Backup Domain reset does not occur 1: Backup Domain reset occurs This bit is set by hardware when Backup Domain reset occurs, either a Backup Domain power on reset or Backup Domain software reset. The bit is cleared by a software read. This bit must be cleared after the system is first powered, otherwise it will be impossible to detect when a Backup Domain reset has been triggered. When this bit is read as 1, a read software loop must be implemented until the bit returns again to 0. This software loop is necessary to confirm that the Backup Domain is ready for access. It must be implemented after the Backup Domain is first powered up.

Backup Domain Control Register – BAKCR

This register provides power control bits for the Deep-Sleep and Power-Down modes.

Offset: 0x104

Reset value: 0x0000_0000 (Reset only by Backup Domain reset)

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	DMOSSTS	Reserved		V18RDYSC	Reserved		WUPIEN	WUPEN
Type/Reset	RO 0			RW 0			RW 0	RW 0
	7	6	5	4	3	2	1	0
	DMOSON	Reserved			LDOOFF	Reserved		BAKRST
Type/Reset	RW 0				RW 0			WO 0

Bits	Field	Descriptions
[15]	DMOSSTS	Depletion MOS Status This bit is set to 1 if the DMOSON bit in this register has been set to 1. This bit is cleared to 0 if the DMOSON bit has been set to 0 or if a BOD reset occurred.
[12]	V18RDYSC	V_{DD18} Ready Source Selection Setting this bit to determine what control signal of isolation cells is used to disable the isolation function of the V_{18} to V_{33} power domain level shifter. 0: BKISO bit in the LPCR register located in the CKCU 1: V_{DD18} POR
[9]	WUPIEN	External WAKEUP Pin Interrupt Enable 0: Disable WAKEUP pin interrupt function 1: Enable WAKEUP pin interrupt function The software can set the WUPIEN bit to 1 to assert the LPWUP interrupt in the NVIC unit when both the WUPEN and WUPF bits are set to1.
[8]	WUPEN	External WAKEUP Pin Enable 0: Disable WAKEUP pin function 1: Enable WAKEUP pin function The software can set the WUPEN bit as 1 to enable the WAKEUP pin function before entering the power saving mode. When WUPEN=1, a rising edge on the WAKEUP pin wakes up the system from the power saving mode. For the WAKEUP pin is active high, the pin should be set as input pull down mode. The corresponding registers which should be properly set are the PBPD [6] to 1 in the PBPDR register, the PBPU [6] to 0 in the PBPUR register and the PBCFG6 field to 0x01 in the GPBCFGR register. **Note:** This bit is reset by a system reset or a Backup Domain reset. Because this bit is located in the Backup Domain, after reset activity there will be a delay until the bit is active. The bit will not be active until the system reset finished and the Backup Domain ISO signal has been disabled. This means that the bit can not be immediately set by software after a system reset finished and the Backup domain ISO signal disabled. The delay time needed is a minimum of three 32kHz clock periods until the bit reset activity has finished.

Bits	Field	Descriptions
[7]	DMOSON	DMOS Control 0: DMOS is OFF 1: DMOS is ON A DMOS is implemented to provide an alternative voltage source for the 1.8V power domain when the Cortex™-M3 enters the Deep-Sleep mode (SLEEPDEEP=1). The control bit DMOSON is set by software and cleared by software or PORB. If the DMOSON bit is set to 1, the LDO will automatically be turned off when the Cortex™-M3 enters the Deep-Sleep mode.
[3]	LDOOFF	LDO Operating Mode Control 0: The LDO operates in a low current mode when Cortex™-M3 enters the Deep-Sleep mode (SLEEPDEEP=1). The V_{DD18} power is available. 1: The LDO is turned off when the Cortex™-M3 enters the Deep-Sleep mode (SLEEPDEEP=1). The V_{DD18} power is not available. **Note:** This bit is only available when the DMOSON bit is cleared to 0.
[0]	BAKRST	Backup Domain Software Reset 0: No action 1: Backup Domain Software Reset is activated – includes all the related RTC and PWRCU registers.

Backup Domain Test Register – BAKTEST

This register specifies a read-only value for the software to recognize whether backup domain is ready for access.

Offset: 0x108

Reset value: 0x0000_0027

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	BAKTEST							
Type/Reset	RO 0	RO 0	RO 1	RO 0	RO 0	RO 1	RO 1	RO 1

Bits	Field	Descriptions
[7:0]	BAKTEST	Backup Domain Test Bits A constant 0x27 will be read when the Backup Domain is ready for Cortex™-M3 access.

HSI Ready Counter Control Register – HSIRCR

This register specifies the counter bit length of the HSI ready counter.

Offset: 0x10C

Reset value: 0x0000_0003 (Reset only by Backup Domain reset)

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved						HSIRCBL	
Type/Reset							RW 1	RW 1

Bits	Field	Descriptions
[1:0]	HSIRCBL	HSI Ready Counter Bit Length 00: 4 bits 01: 5 bits 10: 6 bits 11: 7 bits The HSIRCBL field specifies the bit length of the HSI ready counter. Software can set the HSIRCBL field to shorten the startup waiting time of the HSI oscillator before entering the Deep-Sleep mode or Power-Down mode. (HSICRBL is reset only by Backup Domain reset).

Low Voltage/Brown Out Detect Control and Status Register – LVDCSR

This register specifies flags, enable bits, and option bits for Low-Voltage/Brown-out detector.

Offset: 0x110

Reset value: 0x0000_0000 (Reset only by Backup Domain reset)

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
		Reserved	LVDEWEN	LVDIWEN	LVDF		LVDS	LVDEN
Type/Reset			RW 0	RW 0	RO 0	RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved				BODF	Reserved	BODRIS	BODEN
Type/Reset					RO 0		RW 0	RW 0

Bits	Field	Descriptions
[21]	LVDEWEN	LVD Event Wake-up Enable 0: LVD event wake-up is disabled 1: LVD event wake-up is enabled Setting this bit to 1 will enable the LVD event wake-up function to wake up the system when a LVD condition occurs which result in the LVDF bit being asserted. If the system requires to be woken up from the Deep-Sleep or Power-Down mode by a LVD condition, this bit must be set to 1.
[20]	LVDIWEN	LVD Interrupt Wake-up Enable 0: LVD interrupt wake-up is disabled 1: LVD interrupt wake-up is enabled Setting this bit to 1 will enable the LVD interrupt function. When a LVD condition occurs and the LVDIWEN bit is set to 1, a LVD interrupt will be generated and sent to the Cortex™-M3 NVIC unit.
[19]	LVDF	Low Voltage Detect Status Flag 0: V_{DD33} is higher than the specific voltage level 1: V_{DD33} is equal to or lower than the specific voltage level When the LVD condition occurs, the LVDF flag will be asserted. When the LVDF flag is asserted, a LVD interrupt will be generated for Cortex™-M3 if the LVDIWEN bit is set to 1. However, if the LVDEWEN bit is set to 1 and the LVDIWEN bit is cleared to 0, only a LVD event will be generated rather than a LVD interrupt when the LVDF flag is asserted.
[18:17]	LVDS	Low Voltage Detect Level Selection 00: 2.7V nominal – default value 01: 2.8V nominal 10: 2.9V nominal 11: 3.0V nominal

Bits	Field	Descriptions
[16]	LVDEN	Low Voltage Detect Enable 0: Disable Low Voltage Detect 1: Enable Low Voltage Detect Setting this bit to 1 will generate a LVD event when the 3.3V power is lower than the voltage set by LVDS bits. Therefore when the LVD function is enabled before the system is into the Deep-Sleep2 (DMOS is turn on and LDO is power down) or Power-Down mode (DMOS and LDO are power down), the LVDEWEN bit has to be enabled to avoid the LDO does not activate in the meantime when the CPU is woken up by the low voltage detection activity.
[3]	BODF	Brow Out Detection Flag If V_{DD33} < 2.6V, BODF=1. Otherwise, BODF=0.
[1]	BODRIS	BOD Reset or Interrupt Selection 0: Reset the whole device 1: Generate Interrupt
[0]	BODEN	Brown Out Detect Enable 0: Disable Brown Out Detect 1: Enable Brown Out Detect

Backup Register n – BAKREGn, n=0~9

This register specifies backup register n for storing data during the V_{DD18} power-off period.

Offset: 0x200~0x224

Reset value: 0x0000_0000 (Reset only by Backup Domain reset)

	31	30	29	28	27	26	25	24
	BAKREGn							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	BAKREGn							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	BAKREGn							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	BAKREGn							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[31:0]	BAKREGn	Backup Register n (n=0~9) These registers are used for data storage in general purpose. The contents of BAKREGn registers will remain even if the V_{DD18} power is lost.

6 Clock Control Unit (CKCU)

Introduction

The Clock Control unit, CKCU, provides a range of frequencies and clock functions. These include a High Speed Internal RC oscillator (HSI), a High Speed External crystal oscillator (HSE), a Low Speed Internal RC oscillator (LSI), a Low Speed External crystal oscillator (LSE), a Phase Lock Loop (PLL), a HSE clock monitor, clock prescalers, clock multiplexers and clock gating circuitry. The clocks of the AHB, APB and Cortex™-M3 are derived from the system clock (CK_SYS) which can source from the HSI, HSE or PLL. The Watchdog Timer and Real Time Clock (RTC) use either the LSI or LSE as their clock source. The maximum operating frequency of the system core clock (CK_AHB) can be up to 72MHz.

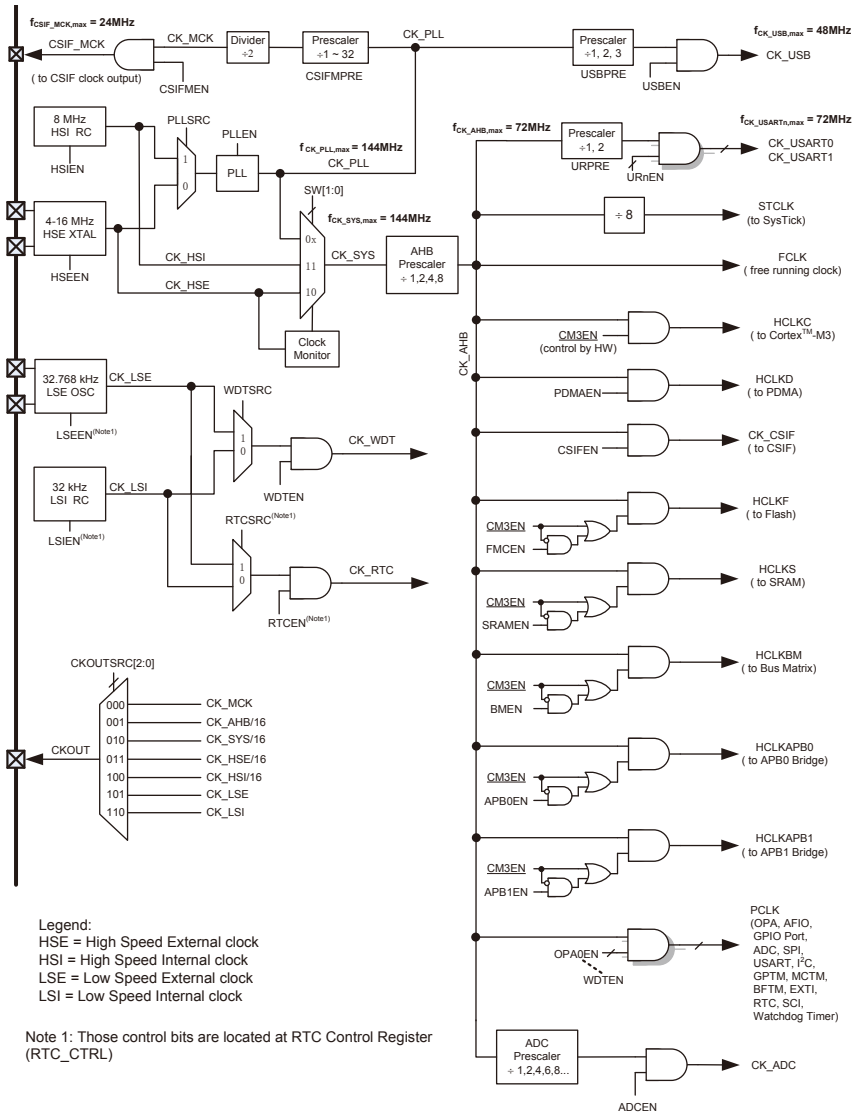


Figure 12. CKCU Block Diagram

Some of the internal clocks can also be wired out via the CKOUT pin for debugging purposes. The clock monitor circuit can be used to detect an HSE clock failure. Once the HSE clock has ceased to operate, for whatever reason, the CKCU will force the system clock source to switch to the HSI clock to prevent a system halt from occurring.

Features

- 4 to 16MHz High Speed External crystal oscillator – HSE
- 8MHz High Speed Internal RC oscillator – HSI
- 32,768Hz Low Speed External crystal oscillator – LSE
- 32kHz Low Speed Internal RC oscillator – LSI
- PLL clock source can be HSE or HSI
- HSE clock monitor

Functional Descriptions

High Speed External Crystal Oscillator – HSE

The high speed external crystal oscillator, HSE, which has a frequency from 4 to 16MHz, produces a highly accurate clock source for use as the system clock. The crystal with a specific frequency must be connected and located close to the two HSE pins, XTALIN/XTALOUT. The external resistor and capacitor components connected to the crystal are necessary for proper oscillation.

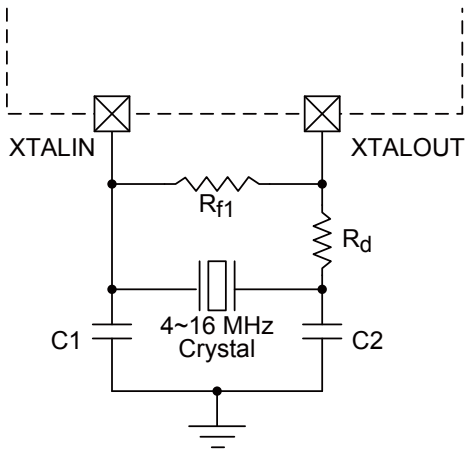


Figure 13. External HSE Crystal, Ceramic, and Resonator

The HSE crystal oscillator can be switched on or off using the HSEEN bit in the Global Clock Control Register GCCR. The HSERDY flag in the Global Clock Status Register GCSR indicates if the high-speed external crystal oscillator is stable. When the HSE is powered up, it will not be released for use until this HSERDY bit is set by the hardware. This specific delay period is known as the oscillator "Start-up time". As the HSE becomes stable, an interrupt will be generated if the related interrupt enable bit HSERDYIE in the Global Clock Interrupt Register GCIR is set. At this point the HSE clock can be used directly as the system clock source or the PLL input clock.

High Speed Internal RC Oscillator – HSI

The high speed internal RC oscillator, HSI, has a fixed frequency of 8MHz and is the default clock source selection for the CPU when the device is powered up. The HSI oscillator provides a lower cost type clock source as no external components are required. The HSI RC oscillator can be switched on or off using the HSIEN bit in the Global Clock Control Register GCCR. The HSIRDY flag in the Global Clock Status Register GCSR is used to indicate if the internal RC oscillator is stable. The start-up time of the HSI oscillator is shorter than the HSE crystal oscillator. An interrupt can be generated if the related interrupt enable bit, HSIRDYIE, in the Global Clock Interrupt Register, GCIR, is set when the HSI becomes stable. The HSI clock can also be used as the PLL input clock.

The frequency accuracy of the HSI can be calibrated by the manufacturer, but its operating frequency is still less accurate than HSE. The applications requirements, environmens and cost will determine which oscillator type is selected.

If the HSE or PLL is the system clock source, to minimize the time required for the system to recover from the Deep-Sleep Mode, the software can set the PSRCEN bit (Power Saving Wake-up RC Clock Enable) to 1 to force the HSI clock to be system clock when the system initially wake-up. Subsequently, the system clock will automatically be switched back to the original clock source, HSE or PLL, when the original clock source ready flag is asserted. This function will reduce the wake-up time when using the HSE or PLL as the system clock.

Phase Locked Loop – PLL

The internal Phase Locked Loop, PLL, can provide 8~144MHz clock output which is 2~36 multiples of a fundamental reference frequency of 4~16MHz. The PLL includes a reference divider, feedback dividers, a digital phase frequency detector (PD), a current-controlled charge pump (CP), an internal loop filter and a voltage-controlled oscillator (VCO) to achieve a stable phase-locked state.

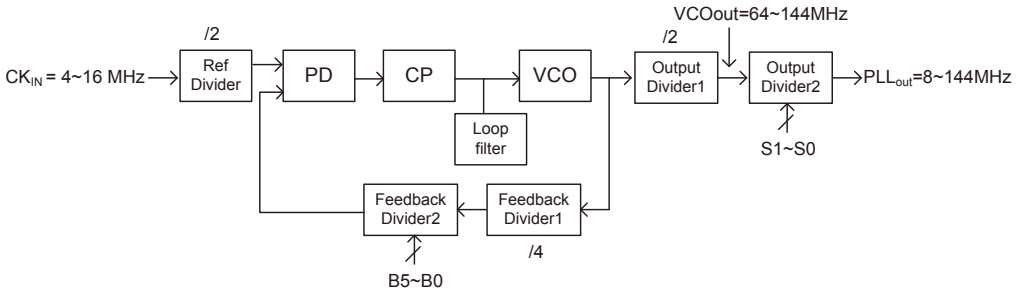


Figure 14. PLL Block Diagram

The PLL output clock frequency can be determined by the following formula:

$$PLL_{OUT} = CK_{IN} * \frac{NF1 * NF2}{NR * NO1 * NO2} = CK_{IN} * \frac{4 * NF2}{2 * 2 * NO2} = CK_{IN} * \frac{NF2}{NO2}$$

where NR=Ref divider=2, NF1=Feedback divider 1=4, NF2=Feedback divider 2=1~64,

NO1=Output divider 1=2, NO2=Output divider 2=1, 2, 4, or 8

Consider a duty cycle of 50% and where both input and output frequencies are divided by 2. If a given clock PLL input clock source frequency, CK_{IN}, generates a specific PLL output frequency, then it is recommended to use a higher value for NF2 in order to increase PLL stability and reduce jitter at the expense of settling time. The setup bits of the output and feedback divider 2 are described in the following two tables. All the setup bits named S1~S0 and B5~B0 in the tables are defined in the PLL Configuration Register PLLCFGR and the PLL Control Register PLLCR in the Register Definition section. Note that the VCO_{OUT} frequency must have a range from 64MHz to 144MHz. If the selected configuration exceeds this range, the PLL output frequency cannot be guaranteed to match the above PLL_{OUT} formula.

The PLL can be switched on or off by using the PLLEN bit in the Global Clock Control Register GCCR. The PLLRDY flag in the Global Clock Status Register GCSR will indicate if the PLL clock is stable. An interrupt can be generated if the related interrupt enable bit, PLLRDYIE, in the Global Clock Interrupt Register, GCIR, is set as the PLL becomes stable.

Table 15. Output Divider 2 Setting

Output divider 2 setup bits S1~S0 (POTD bits in the PLLCFGR register)	NO2 (Output divider 2 value)
00	1
01	2
10	4
11	8

Table 16. Feedback Divider 2 value Setting

Feedback divider 2 setup bits B5~B0 (PFBD bits in the PLLCFGR register)	NF2 (Feedback divider 2 value)
000000	64
000001	1
000010	2
000011	3
000100	4
000101	5
000110	6
000111	7
001000	8
001001	9
001010	10
001011	11
001100	12
001101	13
001110	14
⋮	⋮
111111	63

Low Speed External Crystal Oscillator – LSE

The low speed external crystal or ceramic resonator oscillator, which has a frequency of 32,768Hz, produces a low power but highly accurate clock source for the Real-Time-Clock circuit and the Watchdog Timer. The crystal or ceramic resonator must be located close to the two LSE pins, XTAL32KIN and XTAL32KOUT. Their external resistors and capacitors are necessary for proper oscillation. The LSE oscillator can be switched on or off using the LSEEN bit in the RTC Control Register RTCCR. The LSERDY flag in the Global Clock Status Register GCSR will indicate if the LSE clock is stable. An interrupt can be generated if the related interrupt enable bit LSERDYIE, in the Global Clock Interrupt Register GCIR is set when the LSE becomes stable.

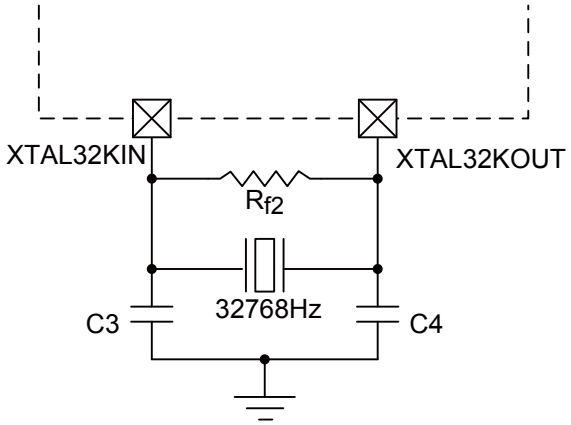


Figure 15. External Crystal, Ceramic, and Resonator for LSE

Low Speed Internal RC Oscillator – LSI

The low speed internal RC oscillator has a frequency of about 32kHz and is a low power clock source for the Real Time Clock circuit or the Watchdog Timer. The LSI offers a low cost clock source as no external components are required. The LSI RC oscillator can be switched on or off by using the LSIEN bit in the RTC Control Register, RTCCR. The frequency accuracy can be calibrated using the configuration options. The LSIRDY flag in the Global Clock Status Register GCSR will indicate if the LSI clock is stable. An interrupt can be generated if the related interrupt enable bit LSIRDYIE in the Global Clock Interrupt Register GCIR is set when the LSI becomes stable.

Clock Ready Flag

The CKCU provides the corresponding clock ready flags of the HSI, HSE, PLL, LSI, and LSE to indicate if these clocks are stable. Before users select the clock as the system clock source or other purpose, it is necessary to confirm the specific clock ready flag is set. Software can check the specific clock is ready or not by polling the individual clock ready status bit in the GCSR register. Additionally, the CKCU can trigger an interrupt to notify the specific clock is ready if the corresponding interrupt enable bit in the GCIR register is set. Software should clear the interrupt status bit in the GCIR register during the interrupt service routine.

System Clock Selection – CK_SYS

After the system reset, the default CK_SYS source will be HSI and can be switched to HSE or PLL by changing the System Clock Switch bits, SW, in the Global Clock Control Register, GCCR. When the SW value is changed, the CK_SYS will continue to operate using the original clock source until the target clock source is stable. The corresponding clock ready status is in the Global Clock Status Register, GCSR, and the clock source usage can be found in the Clock Source Status Register, CKST. When a clock source is used directly by the CK_SYS or the PLL, it is not possible to stop it.

HSE Clock Monitor

The HSE clock monitor function is enabled by the HSE Clock Monitor Enable bit, CKMEN, in the Global Clock Control Register, GCCR. This function should be enabled after the HSE start-up delay and disabled when the HSE is stopped. Once the HSE failure is detected, the HSE will be automatically disabled. The HSE Clock Stuck Flag, CKSF, in the Global Clock Interrupt Register, GCIR, will be set and the HSE failure event will be generated if the Clock Stuck Interrupt Enable bit, CKSIE, in the GCIR register is set. This failure interrupt is connected to the Non-Maskable Interrupt, NMI, of the Cortex™-M3. If the HSE is selected as the clock source of CK_SYS or PLL, the HSE failure will force the CK_SYS source to HSI and the PLL will be disabled automatically.

Clock Output Capability

The clock output capability of HT32 series MCU is ranging from 32kHz to 9MHz. There are several clock signals can be selected via the CKOUT Clock Source Selection bits, CKOUTSRC, in the Global Clock Configuration Register, GCFGR. The corresponding GPIO pin should be configured in the properly Alternate Function I/O (AFIO) mode to output the selected clock signal.

Table 17. CKOUT Clock Source

CKOUTSRC	Clock Source
000	CK_MCK
001	CK_AHB/16
010	CK_SYS/16
011	CK_HSE/16
100	CK_HSI/16
101	CK_LSE
110	CK_LSI
111	Reserved

Register Map

The following table shows the CKCU registers and their reset value.

Table 18. CKCU Register Map

Register	Offset	Description	Reset Value
CKCU Base Address=0x4008_8000			
GCFGR	0x000	Global Clock Configuration Register	0x0000_0102
GCCR	0x004	Global Clock Control Register	0x0000_0803
GCSR	0x008	Global Clock Status Register	0x0000_0028
GCIR	0x00C	Global Clock Interrupt Register	0x0000_0000
PLLCFGR	0x018	PLL Configuration Register	0x0000_0000
PLLCR	0x01C	PLL Control Register	0x0000_0000
AHBCFGR	0x020	AHB Configuration Register	0x0001_0000
AHBCCR	0x024	AHB Clock Control Register	0x0000_00E5
APBCFGR	0x028	APB Configuration Register	0x0001_0000
APBCCR0	0x02C	APB Clock Control Register 0	0x0000_0000
APBCCR1	0x030	APB Clock Control Register 1	0x0000_0000
CKST	0x034	Clock Source Status Register	0xC100_0000
LPCR	0x300	Low Power Control Register	0x0000_0000
MCUDBGCR	0x304	MCU Debug Control Register	0x0000_0000

Register Descriptions

Global Clock Configuration Register – GCFGR

This register specifies the clock source for the CSIF/USB/PLL/USART/Watchdog Timer/CKOUT circuit.

Offset: 0x000

Reset value: 0x0000_0102

	31	30	29	28	27	26	25	24
	LPMOD			CSIFMPRE				
Type/Reset	RO 0	RO 0	RO 0	RW 0	RW 0	RW 0	RW 0	RW 0
	23	22	21	20	19	18	17	16
	USBPRE		URPRE		Reserved			
Type/Reset	RW 0	RW 0	RW 0	RW 0				
	15	14	13	12	11	10	9	8
	Reserved							PLLSRC
Type/Reset								RW 1
	7	6	5	4	3	2	1	0
	Reserved				WDTSRC	CKOUTSRC		
Type/Reset					RW 0	RW 0	RW 1	RW 0

Bits	Field	Descriptions
[31:29]	LPMOD	Lower Power Mode Status 000: Device in initial status 001: Device has been woken up from Sleep mode 010: Device has been woken up from Deep Sleep mode 1 011: Device has been woken up from Deep Sleep mode 2 100: Device has been woken up from Power Down mode Others: Reserved This field is set and reset by hardware.
[28:24]	CSIFMPRE	CSIF_MCK Clock Prescaler Selection CK_MCK=CK_PLL/(CSIFMPRE + 1)/2 00000: CK_MCK=CK_PLL/2 00001: CK_MCK=CK_PLL/4 ... 11111: CK_MCK=CK_PLL/64 This field is set and reset by software to control the CSIF_MCK clock prescaler division.
[23:22]	USBPRE	USB Clock Prescaler Selection 00: CK_USB=CK_PLL 01: CK_USB=CK_PLL/2 10: CK_USB=CK_PLL/3 11: Reserved This field is set and reset by software to control the USB clock prescaler division.
[21:20]	URPRE	USART Clock Prescaler Selection 00: CK_USART=CK_AHB 01: CK_USART=CK_AHB/2 Others: Reserved This field is set and reset by software to control the USART clock prescaler value.

Bits	Field	Descriptions
[8]	PLLSRC	PLL Clock Source Selection 0: External 4~16MHz crystal oscillator clock is selected (HSE) 1: Internal 8MHz RC oscillator clock is selected (HSI) This bit is set and reset by software to control the PLL clock source.
[3]	WDTSRC	Watchdog Timer Clock Source Selection 0: Internal LSI 32kHz RC oscillator clock selected 1: External LSE 32,768Hz crystal oscillator clock selected This bit is set and reset by software to control the Watchdog Timer clock source.
[2:0]	CKOUTSRC	CKOUT Clock Source Selection Set and reset by software. 000: CK_MCK selected 001: (CK_AHB/16) selected 010: (CK_SYS/16) selected 011: (CK_HSE/16) selected 100: (CK_HSI/16) selected 101: CK_LSE selected 110: CK_LSI selected 111: Reserved

Global Clock Control Register – GCCR

This register specifies the clock enable bits.

Offset: 0x004

Reset value: 0x0000_0803

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved						PSRCEN	CKMEN
Type/Reset							RW 0	RW 0
	15	14	13	12	11	10	9	8
	Reserved				HSIEN	HSEEN	PLLEN	Reserved
Type/Reset					RW 1	RW 0	RW 0	
	7	6	5	4	3	2	1	0
	Reserved						SW	
Type/Reset							RW 1	RW 1

Bits	Field	Descriptions
[17]	PSRCEN	Power Saving Wakeup RC Clock Enable 0: No action 1: Use HSI as the temporary CK_SYS source after waking up from Deep-Sleep1 or Deep-Sleep2 When the PSRCEN bit is set to 1, the HSI will be used as the clock source of the CK_SYS after waking up from the Deep-Sleep1 or Deep-Sleep2 mode. This means that the instruction can be executed early before the original CK_SYS source such as HSE or PLL is stable.
[16]	CKMEN	HSE Clock Monitor Enable 0: Disable the External 4~16MHz crystal oscillator (HSE) clock monitor 1: Enable the External 4~16MHz crystal oscillator (HSE) clock monitor When the hardware detects that the HSE clock is stuck at a low or high state, the internal hardware will switch the system clock to be the internal high speed HSI RC clock. The way to recover the original system clock is by either an external reset, power on reset or clearing CKSF by software. **NOTE:** When the HSE clock monitor is enabled, the hardware will automatically enable the HSI internal RC oscillator regardless of the control bit, HSIEN, state.
[11]	HSIEN	Internal High Speed oscillator Enable 0: Internal 8MHz RC oscillator disabled 1: Internal 8MHz RC oscillator enabled Set and reset by software. This bit cannot be reset if the HSI clock is used as the system clock.
[10]	HSEEN	External High Speed oscillator Enable 0: External 4~16MHz crystal oscillator disabled 1: External 4~16MHz crystal oscillator enabled Set and reset by software. This bit cannot be reset if the HSE clock is used as the system clock or the PLL input clock.

Bits	Field	Descriptions
[9]	PLLEN	PLL Enable 0: PLL is switched off 1: PLL is switched on Set and reset by software. This bit cannot be reset if the PLL clock is used as the system clock.
[1:0]	SW	System Clock Switch 0X: Select CK_PLL as the CK_SYS source 10: Select CK_HSE as the CK_SYS source 11: Select CK_HSI as the CK_SYS source Set by software to select the CK_SYS source. Because the change of CK_SYS has inherent latency, software should read these bits to confirm whether the switching is complete or not. The switch will be forced to HSI by HSE clock monitor when the HSE failure is detected and the HSE is selected as the clock source of CK_SYS or PLL.

Global Clock Status Register – GCSR

This register indicates the clock ready status.

Offset: 0x008

Reset value: 0x0000_0028

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								

	7	6	5	4	3	2	1	0
		Reserved	LSIRDY	LSERDY	HSIRDY	HSERDY	PLLRDY	Reserved
Type/Reset			RO 1	RO 0	RO 1	RO 0	RO 0	

Bits	Field	Descriptions
[5]	LSIRDY	LSI Internal Low Speed Oscillator Ready Flag 0: LSI oscillator not ready 1: LSI oscillator ready This bit is set by hardware to indicate if the LSI oscillator is stable and ready for use.
[4]	LSERDY	LSE External Low Speed Oscillator Ready Flag 0: LSE oscillator not ready 1: LSE oscillator ready This bit is set by hardware to indicate if the LSE oscillator is stable and ready for use.
[3]	HSIRDY	HSI High Speed Internal Oscillator Ready Flag 0: HSI oscillator not ready 1: HSI oscillator ready This bit is set by hardware to indicate if the HSI oscillator is stable and ready for use.
[2]	HSERDY	HSE High Speed External Clock Ready Flag 0: HSE oscillator not ready 1: HSE oscillator ready This bit is set by hardware to indicate if the HSE oscillator is stable and ready for use.
[1]	PLLRDY	PLL Clock Ready Flag 0: PLL not ready 1: PLL ready This bit is set by hardware to indicate if the PLL output clock is stable and ready for use.

Global Clock Interrupt Register – GCIR

This register specifies the interrupt enable and flag bits.

Offset: 0x00C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved	LSIRDYIE	LSERDYIE	HSIRDYIE	HSERDYIE	PLLRDYIE	Reserved	CKSIE
Type/Reset		RW 0	RW 0	RW 0	RW 0	RW 0		RW 0
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved	LSIRDYF	LSERDYF	HSIRDYF	HSERDYF	PLLRDYF	Reserved	CKSF
Type/Reset		WC 0	WC 0	WC 0	WC 0	WC 0		WC 0

Bits	Field	Descriptions
[22]	LSIRDYIE	LSI Ready Interrupt Enable 0: Disable the LSI stabilization interrupt 1: Enable the LSI stabilization interrupt This bit is used to control whether the LSI stabilization interrupt is enabled or disabled.
[21]	LSERDYIE	LSE Ready Interrupt Enable 0: Disable the LSE stabilization interrupt 1: Enable the LSE stabilization interrupt This bit is used to control whether the LSE stabilization interrupt is enabled or disabled.
[20]	HSIRDYIE	HSI Ready Interrupt Enable 0: Disable the HSI stabilization interrupt 1: Enable the HSI stabilization interrupt This bit is set and reset by software used to enable or disable the HSI stabilization interrupt.
[19]	HSERDYIE	HSE Ready Interrupt Enablethe 0: Disable the HSE stabilization interrupt 1: Enable the HSE stabilization interrupt This bit is set and reset by software used to enable or disable the HSE stabilization interrupt.
[18]	PLLRDYIE	PLL Ready Interrupt Enable 0: Disable the PLL stabilization interrupt 1: Enable the PLL stabilization interrupt This bit is set and reset by software used to enable or disable the PLL stabilization interrupt.
[16]	CKSIE	Clock Stuck Interrupt Enable 0: Disable the clock fail interrupt 1: Enable the clock fail interrupt This bit is set and reset by software used to enable or disable the clock monitor interrupt.

Bits	Field	Descriptions
[6]	LSIRDYF	LSI Ready Interrupt Flag 0: No LSI stabilization clock ready interrupt generated 1: LSI stabilization interrupt generated This bit is cleared by writing 1 into it and set by hardware when the Internal 32kHz RC oscillator clock is stable and the LSIRDYIE bit is set.
[5]	LSERDYF	LSE Ready Interrupt Flag 0: No LSE stabilization interrupt generated 1: LSE stabilization interrupt generated This bit is cleared by writing 1 into it and set by hardware when the External 32,768Hz crystal oscillator clock is stable and the LSERDYIE bit is set.
[4]	HSIRDYF	HSI Ready Interrupt Flag 0: No HSI stabilization interrupt generated 1: HSI stabilization interrupt generated This bit is cleared by writing 1 into it and set by hardware when the internal 8MHz RC oscillator clock is stable and the HSIRDYIE bit is set.
[3]	HSERDYF	HSE Ready Interrupt Flag 0: No HSE stabilization interrupt generated 1: HSE stabilization interrupt generated This bit is cleared by writing 1 into it and set by hardware when the External 4~16MHz crystal oscillator clock is stable and the HSERDYIE bit is set.
[2]	PLLRDYF	PLL Ready Interrupt Flag 0: No PLL stabilization interrupt generated 1: PLL stabilization interrupt generated This bit is cleared by writing 1 into it and set by hardware when the PLL is stable and the PLLRDYIE bit is set.
[0]	CKSF	HSE Clock Stuck Interrupt Flag 0: Clock operating normally 1: HSE clock stuck This bit is cleared by writing 1 into it and set by hardware when the HSE clock is stuck and the CKSIE bit is set.

PLL Configuration Register – PLLCFGR

This register specifies the PLL configuration.

Offset: 0x018

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved			PFBD [5:1]				
Type/Reset				RW 0	RW 0	RW 0	RW 0	RW 0
	23	22	21	20	19	18	17	16
	PFBD[0]	POTD		Reserved				
Type/Reset	RW 0	RW 0	RW 0					
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved							
Type/Reset								

Bits	Field	Descriptions
[28:23]	PFBD	PLL VCO Output Clock Feedback Divider (B5~B0 in Figure 14) Feedback Divider divides the output clock from the PLL VCO.
[22:21]	POTD	PLL Output Clock Divider (S1~S0 in Figure 14)

PLL Control Register – PLLCR

This register specifies the PLL Bypass mode.

Address offset: 0x01C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	PLLBPS	Reserved						
Type/Reset	RW 0							
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved							
Type/Reset								

Bits	Field	Descriptions
[31]	PLLBPS	PLL Bypass Mode Enable 0: Disable the PLL Bypass mode 1: Enable the PLL Bypass mode in which the PLL output clock PLL_{OUT} is equal to the CK_{IN} clock (refer to the PLL Block diagram)

AHB Configuration Register – AHBCFGR

This register specifies the system clock frequency.

Offset: 0x020

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved						AHBPRE	
Type/Reset							RW 0	RW 0

Bits	Field	Descriptions
[1:0]	AHBPRE	AHB Pre-Scaler 00: CK_AHB=CK_SYS 01: CK_AHB=CK_SYS/2 10: CK_AHB=CK_SYS/4 11: CK_AHB=CK_SYS/8 This field is set and reset by software to control the AHB clock division ratio.

AHB Clock Control Register – AHBCCR

This register specifies the AHB clock enable bits.

Offset: 0x024

Reset value: 0x0000_00E5

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved						CSIFMEN	CSIFEN
Type/Reset							RW 0	RW 0
	7	6	5	4	3	2	1	0
	APB1EN	APB0EN	BMEN	PDMAEN	Reserved	SRAMEN	Reserved	Reserved
Type/Reset	RW 1	RW 1	RW 1	RW 0		RW 1		

Bits	Field	Descriptions
[9]	CSIFMEN	CSIF_MCK Clock Output Enable 0: CSIF_MCK clock disabled 1: CSIF_MCK clock enabled This bit is set and reset by software used to enable or disable the CSIF_MCK clock output.
[8]	CSIFEN	CSIF Clock Enable 0: CSIF clock disabled 1: CSIF clock enabled This bit is set and reset by software used to enable or disable the CSIF circuitry clock.
[7]	APB1EN	APB1 bridge Clock Enable 0: APB1 bridge clock disabled in Sleep mode 1: APB1 bridge clock enabled in Sleep mode This bit is set and reset by software. Note that this bit is only available in the Sleep mode. If the APB1 bridge is not used in the Sleep mode, users can clear the APB1EN bit to 0 to reduce the power consumption before the device enters the Sleep mode.
[6]	APB0EN	APB0 bridge Clock Enable 0: APB0 bridge clock disabled in Sleep mode 1: APB0 bridge clock enabled in Sleep mode This bit is set and reset by software. Note that this bit is only available in the Sleep mode. If the APB0 bridge is not used in the Sleep mode, users can clear the APB0EN bit to 0 to reduce the power consumption before the device enters the Sleep mode.
[5]	BMEN	Bus Matrix Clock Enable 0: Bus Matrix clock disabled in Sleep mode 1: Bus Matrix clock enabled in Sleep mode This bit is set and reset by software. Note that this bit is only available in the Sleep mode. If the Bus Matrix bridge is not used in the Sleep mode, users can clear the BMEN bit to 0 to reduce the power consumption before the device enters the Sleep mode.

Bits	Field	Descriptions
[4]	PDMAEN	Peripheral DMA Clock Enable 0: PDMA clock disabled 1: PDMA clock enabled This bit is set and reset by software. The PDMA can operate when the processor is in the Sleep mode. However, the relevant clocks of the AHB bus slave, such as SRAM or Flash, or the APB peripherals, such as I²C or SPI, which communicate with the PDMA in the Sleep mode have to be enabled before entering the Sleep mode.
[2]	SRAMEN	SRAM Clock Enable 0: SRAM clock disabled in Sleep mode 1: SRAM clock enabled in Sleep mode This bit is set and reset by software. Note that this bit is only available in the Sleep mode. If the SRAM is not used in the Sleep mode, users can clear the SRAMEN bit to 0 to reduce the power consumption before the device enters the Sleep mode.

APB Configuration Register – APBCFGR

This register specifies the frequency of the A/D Converter clock.

Offset: 0x028

Reset value: 0x0001_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved					ADCDIV		
Type/Reset						RW 0	RW 0	RW 1
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved							
Type/Reset								

Bits	Field	Descriptions
[18:16]	ADCDIV	A/D Converter Clock Frequency Division Selection 000: Reserved 001: CK_ADC=(CK_AHB/2) 010: CK_ADC=(CK_AHB/4) 011: CK_ADC=(CK_AHB/8) 100: CK_ADC=(CK_AHB/16) 101: CK_ADC=(CK_AHB/32) 110: CK_ADC=(CK_AHB/64) 111: CK_ADC=(CK_AHB/6) This field is set and reset by software to select the A/D Converter clock division ratio.

APB Clock Control Register 0 – APBCCR0

This register specifies several APB peripheral clock enable bits.

Offset: 0x02C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							SCIEN
Type/Reset								RW 0
	23	22	21	20	19	18	17	16
	Reserved			PEEN	PDEN	PCEN	PBEN	PAEN
Type/Reset				RW 0	RW 0	RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
	EXTIEN	AFIOEN	Reserved				UR1EN	UR0EN
Type/Reset	RW 0	RW 0					RW 0	RW 0
	7	6	5	4	3	2	1	0
		Reserved	SPI1EN	SPI0EN		Reserved	I2C1EN	I2C0EN
Type/Reset			RW 0	RW 0			RW 0	RW 0

Bits	Field	Descriptions
[24]	SCIEN	Smart Card Interface Clock Enable 0: Smart Card clock disabled 1: Smart Card clock enabled This bit is set and reset by software.
[20]	PEEN	GPIO Port E Clock Enable 0: Port E clock disabled 1: Port E clock enabled This bit is set and reset by software.
[19]	PDEN	GPIO Port D Clock Enable 0: Port D clock disabled 1: Port D clock enabled This bit is set and reset by software.
[18]	PCEN	GPIO Port C Clock Enable 0: Port C clock disabled 1: Port C clock enabled This bit is set and reset by software.
[17]	PBEN	GPIO Port B Clock Enable 0: Port B clock disabled 1: Port B clock enabled This bit is set and reset by software.
[16]	PAEN	GPIO Port A Clock Enable 0: Port A clock disabled 1: Port A clock enabled This bit is set and reset by software.
[15]	EXTIEN	External Interrupt Clock Enable 0: EXTI clock disabled 1: EXTI clock enabled This bit is set and reset by software.

Bits	Field	Descriptions
[14]	AFIOEN	Alternate Function I/O Clock Enable 0: AFIO clock disabled 1: AFIO clock enabled This bit is set and reset by software.
[9]	UR1EN	USART1 Clock Enable 0: USART1 clock disabled 1: USART1 clock enabled This bit is set and reset by software.
[8]	UR0EN	USART0 Clock Enable 0: USART0 clock disabled 1: USART0 clock enabled This bit is set and reset by software.
[5]	SPI1EN	SPI1 Clock Enable 0: SPI1 clock disabled 1: SPI1 clock enabled This bit is set and reset by software.
[4]	SPI0EN	SPI0 Clock Enable 0: SPI0 clock disabled 1: SPI0 clock enabled This bit is set and reset by software.
[1]	I2C1EN	I^2C1 Clock Enable 0: I^2C1 clock disabled 1: I^2C1 clock enabled This bit is set and reset by software.
[0]	I2C0EN	I^2C0 Clock Enable 0: I^2C0 clock disabled 1: I^2C0 clock enabled This bit is set and reset by software.

APB Clock Control Register 1 – APBCCR1

This register specifies several APB peripheral clock enable bits.

Offset: 0x030

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							ADCEN
Type/Reset								RW 0
	23	22	21	20	19	18	17	16
	OPA1EN	OPA0EN	Reserved				BFTM1EN	BFTM0EN
Type/Reset	RW 0	RW 0					RW 0	RW 0
	15	14	13	12	11	10	9	8
	Reserved	USBEN	Reserved				GPTM1EN	GPTM0EN
Type/Reset		RW 0					RW 0	RW 0
	7	6	5	4	3	2	1	0
	Reserved	RTCEN	Reserved	WDTEN	Reserved			MCTMEN
Type/Reset		RW 0		RW 0				RW 0

Bits	Field	Descriptions
[24]	ADCEN	ADC Clock Enable 0: ADC clock disabled 1: ADC clock enabled This bit is set and reset by software.
[23]	OPA1EN	OPA/CMP 1 Clock Enable 0: OPA/CMP 1 clock disabled 1: OPA/CMP 1 clock enabled This bit is set and reset by software.
[22]	OPA0EN	OPA/CMP 0 Clock Enable 0: OPA/CMP 0 clock disabled 1: OPA/CMP 0 clock enabled This bit is set and reset by software.
[17]	BFTM1EN	BFTM1 Clock Enable 0: BFTM1 clock disabled 1: BFTM1 clock enabled This bit is set and reset by software.
[16]	BFTM0EN	BFTM0 Clock Enable 0: BFTM0 clock disabled 1: BFTM0 clock enabled This bit is set and reset by software.
[14]	USBEN	USB Clock Enable 0: USB clock disabled 1: USB clock enabled This bit is set and reset by software.
[9]	GPTM1EN	GPTM1 Clock Enable 0: GPTM1 clock disabled 1: GPTM1 clock enabled This bit is set and reset by software.

Bits	Field	Descriptions
[8]	GPTM0EN	GPTM0 Clock Enable 0: GPTM0 clock disabled 1: GPTM0 clock enabled This bit is set and reset by software.
[6]	RTCEN	RTC Clock Enable 0: RTC clock disabled 1: RTC clock enabled This bit is set and reset by software.
[4]	WDTEN	Watchdog Timer Clock Enable 0: Watchdog Timer clock disabled 1: Watchdog Timer clock enabled This bit is set and reset by software.
[0]	MCTMEN	MCTM Clock Enable 0: MCTM0 clock disabled 1: MCTM0 clock enabled This bit is set and reset by software.

Clock Source Status Register – CKST

This register specifies the clock source status.

Offset: 0x034

Reset value: 0xC100_0000

	31	30	29	28	27	26	25	24
	CKSWST		Reserved			HSIST		
Type/Reset	RO 1	RO 1				RO 0	RO 0	RO 1
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	Reserved						HSEST	
Type/Reset							RO 0	RO 0
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	Reserved				PLLST			
Type/Reset					RO 0	RO 0	RO 0	RO 0
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	Reserved							
Type/Reset								

Bits	Field	Descriptions
[31:30]	CKSWST	Clock Switch Status 0x: CK_PLL used as system clock 10: CK_HSE used as system clock 11: CK_HSI used as system clock
[26:24]	HSIST	High Speed Internal Clock Occupation Status (CK_HSI) xx1: HSI used by System Clock (CK_SYS) (SW=0x03) x1x: HSI used by PLL 1xx: HSI used by Clock Monitor
[17:16]	HSEST	High Speed External Clock Occupation Status (CK_HSE) x1: HSE used by System Clock (CK_SYS) (SW=0x02) 1x: HSE used by PLL
[11:8]	PLLST	PLL Clock Occupation Status xxx1: PLL used by System Clock (CK_SYS) xx1x: PLL used by USART x1xx: PLL used by USB 1xxx: PLL used by CSIF

Low Power Control Register – LPCR

This register specifies low power control.

Offset: 0x300

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved							BKISO
Type/Reset								R/W 0

Bits	Field	Descriptions
[0]	BKISO	Backup Domain Isolation Control 0: Backup domain isolated from other power domain 1: Backup domain accessible by other power domain This bit is set and reset by software. Refer to the Power Control Unit chapter for more information.

MCU Debug Control Register – MCUDBGCR

This register specifies the MCU debug control bits.

Offset: 0x304

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved						DBBFTM1	DBBFTM0
Type/Reset							R/W 0	R/W 0
	15	14	13	12	11	10	9	8
	DBSCI	DBDSLP2	DBI2C1	DBI2C0	DBSPI1	DBSPI0	DBUR1	DBUR0
Type/Reset	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0
	7	6	5	4	3	2	1	0
	DBGPTM1	DBGPTM0	Reserved	DBMCTM	DBWDT	DBPD	DBDSLP1	DBSLP
Type/Reset	R/W 0	R/W 0		R/W 0	R/W 0	R/W 0	R/W 0	R/W 0

Bits	Field	Descriptions
[17]	DBBFTM1	BFTM1 Debug Mode Enable 0: BFTM1 counter keeps counting even if the core is halted 1: BFTM1 counter is stopped when the core is halted Set and reset by software. This bit is used to control whether the BFTM1 counter is stopped or not when the core is halted.
[16]	DBBFTM0	BFTM0 Debug Mode Enable 0: BFTM0 counter keeps counting even if the core is halted 1: BFTM0 counter is stopped when the core is halted Set and reset by software. This bit is used to control whether the BFTM0 counter is stopped or not when the core is halted.
[15]	DBSCI	SCI Debug Mode Enable 0: Same behavior as normal mode 1: SCI timeout is stopped Set and reset by software. This bit is used to control whether the SCI timeout mode is stopped or not when the core is halted.
[14]	DBDSLP2	Debug Deep-Sleep2 0: LDO=Off, DMOS=On, FCLK=Off and HCLK=Off in Deep-Sleep2 1: LDO=On, FCLK=On and HCLK=On in Deep-Sleep2 This bit is set and reset by software.
[13]	DBI2C1	I^2C1 Debug Mode Enable 0: Same behavior as normal mode 1: I^2C1 timeout is stopped Set and reset by software. This bit is used to control whether the I^2C1 timeout mode is stopped or not when the core is halted.
[12]	DBI2C0	I^2C0 Debug Mode Enable 0: Same behavior as normal mode 1: I^2C0 timeout is stopped Set and reset by software. This bit is used to control whether the I^2C0 timeout mode is stopped or not when the core is halted.

Bits	Field	Descriptions
[11]	DBSPI1	SPI1 Debug Mode Enable 0: Same behavior as normal mode 1: SPI1 FIFO timeout is stopped Set and reset by software. This bit is used to control whether the SPI1 timeout mode is stopped or not when the core is halted.
[10]	DBSPI0	SPI0 Debug Mode Enable 0: Same behavior as normal mode 1: SPI0 FIFO timeout is stopped Set and reset by software. This bit is used to control whether the SPI0 timeout mode is stopped or not when the core is halted.
[9]	DBUR1	USART1 Debug Mode Enable 0: Same behavior as normal mode 1: USART1 FIFO timeout is stopped Set and reset by software. This bit is used to control whether the USART1 timeout mode is stopped or not when the core is halted.
[8]	DBUR0	USART0 Debug Mode Enable 0: Same behavior as normal mode 1: USART0 FIFO timeout is stopped Set and reset by software. This bit is used to control whether the USART0 timeout mode is stopped or not when the core is halted.
[7]	DBGPTM1	GPTM1 Debug Mode Enable 0: GPTM1 counter keeps counting even if the core is halted 1: GPTM1 counter is stopped when the core is halted Set and reset by software. This bit is used to control whether the GPTM1 counter is stopped or not when the core is halted.
[6]	DBGPTM0	GPTM0 Debug Mode Enable 0: GPTM0 counter keeps counting even if the core is halted 1: GPTM0 counter is stopped when the core is halted Set and reset by software. This bit is used to control whether the GPTM0 counter is stopped or not when the core is halted.
[4]	DBMCTM	MCTM Debug Mode Enable 0: MCTM counter keeps counting even if the core is halted 1: MCTM counter is stopped when the core is halted Set and reset by software. This bit is used to control whether the MCTM counter is stopped or not when the core is halted.
[3]	DBWDT	Watchdog Timer Debug Mode Enable 0: Watchdog Timer counter keeps counting even if the core is halted 1: Watchdog Timer counter is stopped when the core is halted Set and reset by software. This bit is used to control whether the Watchdog Timer counter is stopped or not when the core is halted.
[2]	DBPD	Debug Power-Down Mode 0: LDO=Off, FCLK=Off, and HCLK=Off in Power-Down mode 1: LDO=On, FCLK=On, and HCLK=On in Power-Down mode This bit is set and reset by software.
[1]	DBDSLP1	Debug Deep-Sleep1 0: LDO=Low power mode, FCLK=Off, and HCLK=Off in Deep-Sleep1 1: LDO=On, FCLK=On, and HCLK=On in Deep-Sleep1 This bit is set and reset by software.
[0]	DBSLP	Debug Sleep Mode 0: LDO=On, FCLK=On, and HCLK=Off in Sleep mode 1: LDO=On, FCLK=On, and HCLK=On in Sleep mode This bit is set and reset by software.

7 Reset Control Unit (RSTCU)

Introduction

The Reset Control Unit, RSTCU, has three kinds of reset, the power on reset, system reset and APB unit reset. The power on reset, known as a cold reset, resets the full system during a power up. A system reset resets the processor core and peripheral IP components with the exception of the debug port controller. The resets can be triggered by an external signal, internal events and the reset generators. More information about these resets will be described in the following section.

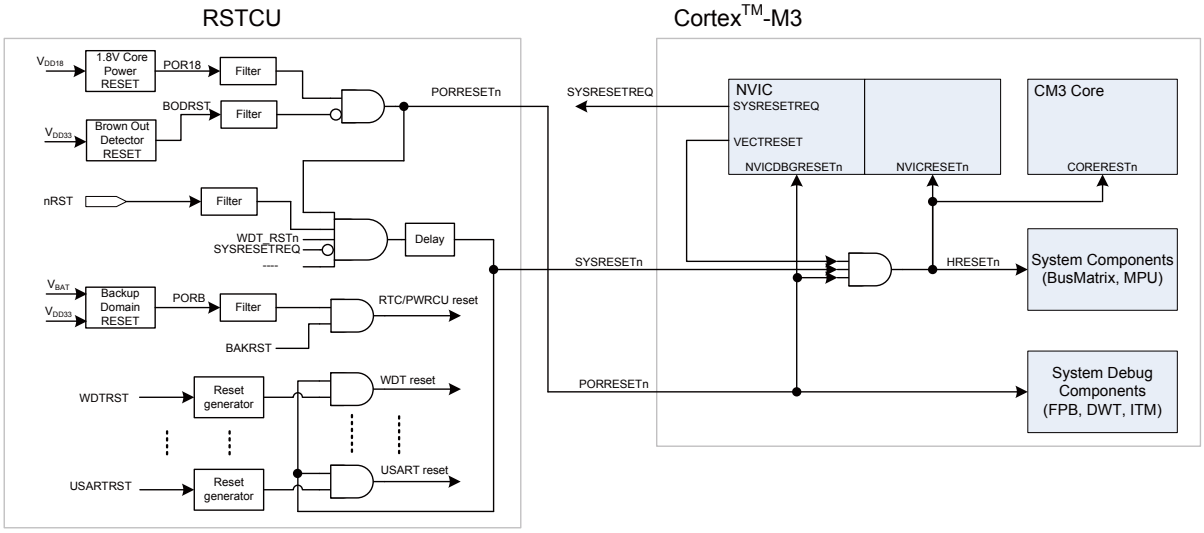


Figure 16. RSTCU Block Diagram

Functional Descriptons

Power On Rest

The Power on reset, POR, is generated by either an external reset or by the internal reset generator. Both types have an internal filter to prevent glitches from causing erroneous reset operations. By referring to Figure 16, the POR18 active low signal will be de-asserted when the internal LDO voltage regulator is ready to provide 1.8V power. In addition to the POR18 signal, the Power Control Unit, PWRCU, will assert the BODF signal as a Power Down Reset, PDR, when the BODEN bit in the LVDCSR register is set and the brown-out event occurs. For more details about the PWRCU function, refer to the PWRCU chapter.

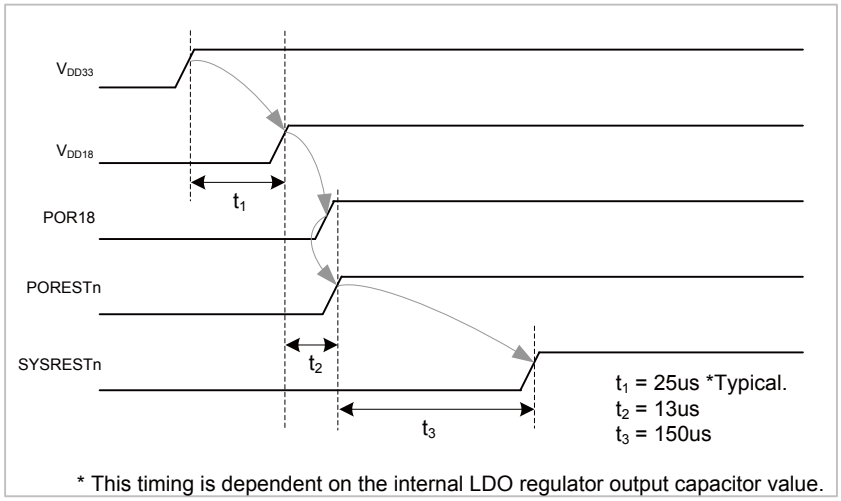


Figure 17. Power On Reset Sequence

System Reset

A System reset is generated by a power on reset (PORRESETn), a Watchdog Timer reset (WDT_RSTn) or a software reset (SYSRESETREQ) event. For more information about SYSRESETREQ and VECTRESET events, refer to the related chapter in the Cortex™-M3 reference manual.

AHB and APB Unit Reset

The AHB and APB unit reset can be divided into hardware and software resets. A hardware reset can be generated by either a power on reset or a system reset for all AHB and APB units. Each functional IP connected to the AHB and APB buses can be reset individually through the associated software reset bits in the RSTCU. For example, the application software can generate a USART0 reset via the UR0RST bit in the APBPRSTR0 register to reset the USART0 circuts.

Register Map

The following table shows the RSTCU registers and reset values.

Table 19. RSTCU Register Map

Register	Offset	Description	Reset Value
RSTCU Base Address=0x4008_8000			
GRSR	0x100	Global Reset Status Register	0x0000_0008
AHBPRSTR	0x104	AHB Peripheral Reset Register	0x0000_0000
APBPRSTR0	0x108	APB Peripheral Reset Register 0	0x0000_0000
APBPRSTR1	0x10C	APB Peripheral Reset Register 1	0x0000_0000

Register Descriptions

Global Reset Status Register – GRSR

This register specifies a variety of reset status conditions.

Offset: 0x100

Reset value: 0x0000_0008

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved				PORSTF	WDTRSTF	EXTRSTF	SYSRSTF
Type/Reset					WC 1	WC 0	WC 0	WC 0

Bits	Field	Descriptions
[3]	PORSTF	Core 1.8V Power On Reset Flag 0: No POR occured 1: POR occured This bit is set by hardware when a power on reset occurs and reset by writing 1 into it.
[2]	WDTRSTF	Watchdog Timer Reset Flag 0: No Watchdog Timer reset occured 1: Watchdog Timer occured This bit is set by hardware when a watchdog timer reset occurs and reset by writing 1 into it or by hardware when a power on reset occurs.
[1]	EXTRSTF	External Pin Reset Flag 0: No pin reset occured 1: Pin reset occured This bit is set by hardware when an external pin reset occurs and reset by writing 1 into it or by hardware when a power on reset occurs.
[0]	SYSRSTF	System Reset Flag 0: No NVIC asserting system reset occured 1: NVIC asserting system reset occured This bit is set by hardware when a system reset occurs and reset by writing 1 into it or by hardware when a power on reset occurs.

AHB Peripheral Reset Register – AHBPRSTR

This register specifies the AHB peripheral software reset control bits.

Offset: 0x104

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved			CSIFRST	Reserved			PDMARST
Type/Reset				RW 0				RW 0

Bits	Field	Descriptions
[4]	CSIFRST	CMOS Sensor Interface (CSIF) Reset Control 0: No reset 1: Reset CMOS Sensor Interface (CSIF) This bit is set by software and cleared to 0 by hardware automatically.
[0]	PDMARST	Peripheral DMA (PDMA) Reset Control 0: No reset 1: Reset Peripheral DMA (PDMA) This bit is set by software and cleared to 0 by hardware automatically.

APB Peripheral Reset Register 0 – APBPRSTR0

This register specifies several APB peripheral software reset control bits.

Offset: 0x108

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							SCIRST
Type/Reset								RW 0
	23	22	21	20	19	18	17	16
	Reserved			PERST	PDRST	PCRST	PBRST	PARST
Type/Reset				RW 0	RW 0	RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
	EXTIRST	AFIORST	Reserved				UR1RST	UR0RST
Type/Reset	RW 0	RW 0					RW 0	RW 0
	7	6	5	4	3	2	1	0
	Reserved		SPI1RST	SPI0RST	Reserved		I2C1RST	I2C0RST
Type/Reset			RW 0	RW 0			RW 0	RW 0

Bits	Field	Descriptions
[24]	SCIRST	Smart Card Interface Reset Control 0: No reset 1: Reset Smart Card Interface This bit is set by software and cleared to 0 by hardware automatically.
[20]	PERST	GPIO Port E Reset Control 0: No reset 1: Reset Port E This bit is set by software and cleared to 0 by hardware automatically.
[19]	PDRST	GPIO Port D Reset Control 0: No reset 1: Reset Port D This bit is set by software and cleared to 0 by hardware automatically.
[18]	PCRST	GPIO Port C Reset Control 0: No reset 1: Reset Port C Set and reset by software. It is cleared to 0 by hardware automatically.
[17]	PBRST	GPIO Port B Reset Control 0: No reset 1: Reset Port B This bit is set by software and cleared to 0 by hardware automatically.
[16]	PARST	GPIO Port A Reset Control 0: No reset 1: Reset Port A This bit is set by software and cleared to 0 by hardware automatically.
[15]	EXTIRST	External Interrupt Controller Reset Control 0: No reset 1: Reset EXTI This bit is set by software and cleared to 0 by hardware automatically.

Bits	Field	Descriptions
[14]	AFIORST	Alternate Function I/O Reset Control 0: No reset 1: Reset Alternate Function I/O This bit is set by software and cleared to 0 by hardware automatically.
[9]	UR1RST	USART1 Reset Control 0: No reset 1: Reset USART1 This bit is set by software and cleared to 0 by hardware automatically.
[8]	UR0RST	USART0 Reset Control 0: No reset 1: Reset USART0 This bit is set by software and cleared to 0 by hardware automatically.
[5]	SPI1RST	SPI1 Reset Control 0: No reset 1: Reset SPI1 This bit is set by software and cleared to 0 by hardware automatically.
[4]	SPI0RST	SPI0 Reset Control 0: No reset 1: Reset SPI0 This bit is set by software and cleared to 0 by hardware automatically.
[1]	I2C1RST	I^2C1 Reset Control 0: No reset 1: Reset I^2C1 This bit is set by software and cleared to 0 by hardware automatically.
[0]	I2C0RST	I^2C0 Reset Control 0: No reset 1: Reset I^2C0 This bit is set by software and cleared to 0 by hardware automatically.

APB Peripheral Reset Register 1 – APBPRSTR1

This register specifies several APB peripheral software reset control bits.

Offset: 0x10C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							ADCRST
Type/Reset								RW 0
	23	22	21	20	19	18	17	16
	OPA1RST	OPA0RST	Reserved				BFTM1RST	BFTM0RST
Type/Reset	RW 0	RW 0					RW 0	RW 0
	15	14	13	12	11	10	9	8
	Reserved	USBRST	Reserved				GPTM1RST	GPTM0RST
Type/Reset		RW 0					RW 0	RW 0
	7	6	5	4	3	2	1	0
	Reserved			WDTRST	Reserved			MCTMRST
Type/Reset				RW 0				RW 0

Bits	Field	Descriptions
[24]	ADCRST	A/D Converter Reset Control 0: No reset 1: Reset A/D Converter This bit is set by software and cleared to 0 by hardware automatically.
[23]	OPA1RST	Comparator and OPA1 Controller Reset Control 0: No reset 1: Reset CMP/OPA1 This bit is set by software and cleared to 0 by hardware automatically.
[22]	OPA0RST	Comparator and OPA0 Controller Reset Control 0: No reset 1: Reset CMP/OPA0 This bit is set by software and cleared to 0 by hardware automatically.
[17]	BFTM1RST	BFTM1 Reset Control 0: No reset 1: Reset BFTM1 This bit is set by software and cleared to 0 by hardware automatically.
[16]	BFTM0RST	BFTM0 Reset Control 0: No reset 1: Reset BFTM0 This bit is set by software and cleared to 0 by hardware automatically.
[14]	USBRST	USB Reset Control 0: No reset 1: Reset USB This bit is set by software and cleared to 0 by hardware automatically.

Bits	Field	Descriptions
[9]	GPTM1RST	GPTM1 Reset Control 0: No reset 1: Reset GPTM1 This bit is set by software and cleared to 0 by hardware automatically.
[8]	GPTM0RST	GPTM0 Reset Control 0: No reset 1: Reset GPTM0 This bit is set by software and cleared to 0 by hardware automatically.
[4]	WDTRST	Watchdog Timer Reset Control 0: No reset 1: Reset Watchdog Timer This bit is set by software and cleared to 0 by hardware automatically.
[0]	MCTMRST	MCTM Reset Control 0: No reset 1: Reset MCTM This bit is set by software and cleared to 0 by hardware automatically.

8 General Purpose I/O (GPIO)

Introduction

There are up to 80 General Purpose I/O port, GPIO, named PA0~PA15, PB0~PB15, PC0~PC15, PD0~PD15 and PE0~PE15 for the device to implement the logic input/output functions. Each of the GPIO ports has related control and configuration registers to satisfy the requirement of specific applications.

The GPIO ports are pin-shared with other alternative functions (AFs) to obtain maximum flexibility on the package pins. The GPIO pins can be used as alternative functional pins by configuring the corresponding registers regardless of the AF input or output pins.

The external interrupts on the GPIO pins of the device have related control and configuration registers in the External Interrupt Control Unit (EXTI).

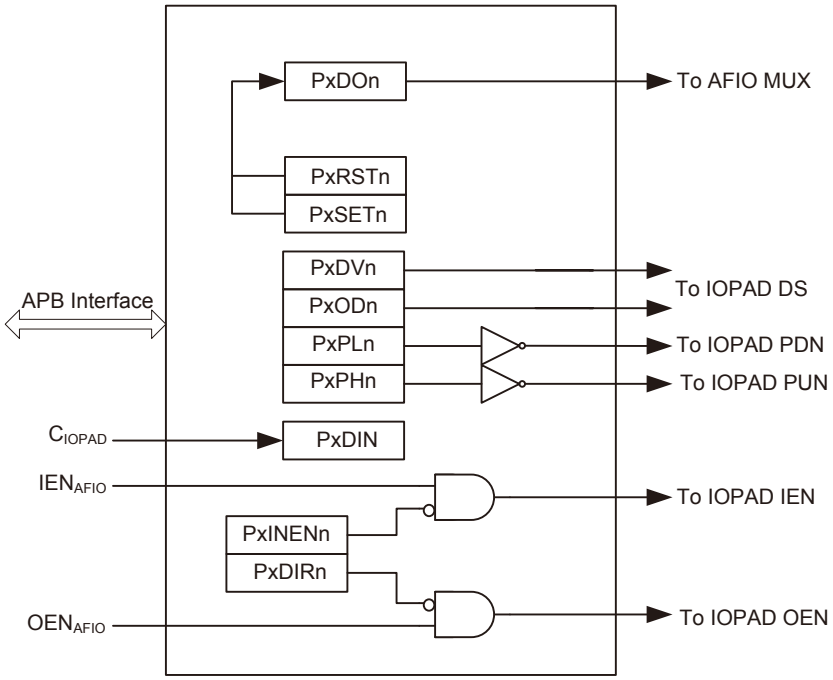


Figure 18. GPIO Block Diagram

Features

- Input/output direction control
- Schmitt Trigger Input function enable control
- Input weak pull-up/pull-down control
- Output push-pull/open drain enable control
- Output set/reset control
- Output drive current selection
- External interrupt with programmable trigger edge – using EXTI configuration registers
- Analog input/output configurations – using AFIO configuration registers
- Alternate function input/output configurations – using AFIO configuration registers
- Port configuration lock

Functional Descriptions

Default GPIO Pin Configuration

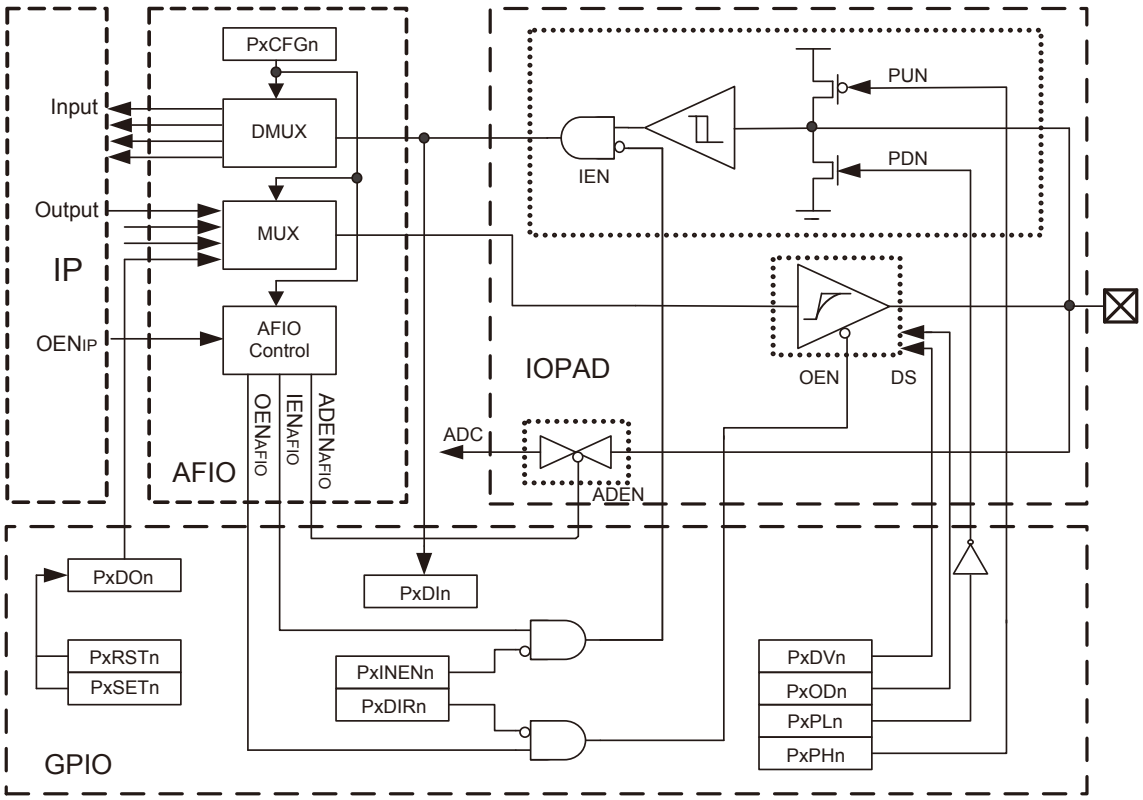
During or just after the reset period, the alternative functions are all inactive and the GPIO ports are configured into the input disable floating mode, i.e. input disabled without pull-up/pull-down resistors. Only the boot and Serial-Wired Debug pins which are pin-shared with the I/O pins PC8, PC9, PE11, PE12, PE13, PE14 and PE15 are active after a device reset.

- PC8/BOOT0: Input enable with internal pull-up
- PC9/BOOT1: Input enable with internal pull-up
- PE11/JTDO/TRACESWO: Input enable with internal pull-down
- PE12/JTCK/SWCLK: Input enable with internal pull-up
- PE13/JTMS/SWDIO: Input or output enable with internal pull-up
- PE14/JTDI: Input enable with internal pull-up
- PE15/JTRS: Input enable with internal pull-up

General Purpose I/O – GPIO

The GPIO pins can be configured as inputs or outputs via the data direction control registers PxDIRCR (where x=A~E). When the GPIO pins are configured as input pins, the data on the external pins can be read if the enable bits in the input enable function register PxINER are set. The GPIO pull-up/pull-down registers PxPUR/PxPDR can be configured to fit specific applications. When the pull-up and pull-down functions are both enabled, the pull-up function has the higher priority while the pull-down function will be blocked until the pull-up function is released.

The GPIO pins can be configured as output pins where the output data is latched into the data register PxDOUTR. The output type can be setup to be either push-pull or open-drain by the open drain selection register PxODR. Only one or several specific bits of the output data will be set or reset by configuring the port output set and reset control register PxSRR or the port output reset control register PxRR without affecting the unselected bits. As the port output set and reset functions are both enabled, the port output set function has the higher priority and the port output reset function will be blocked. The output driving current of the GPIO pins can be selected by configuring the drive current selection register PxDRVR.



PxDIn/PxDOn(x=A~E): Data Input/Data Output

PxRSTn/PxSETn(x=A~E): Reset/Set

PxDIRn(x=A~E): Direction

PxINENn(x=A~E): Input Enable

PxDVn(x=A~E): Output Drive

PXODn(x=A~E): Open Drain

PxPLn/PxPHn(x=A~E): Pull Low/High

PxCFGn(x=A~E): AFIO Configuration

Figure 19. AFIO/GPIO Control Signal

Table 20. AFIO, GPIO and I/O Pad Control Signal True Table

Type	AFIO			GPIO		PAD		
	$ADEN_{AFIO}$	OEN_{AFIO}	IEN_{AFIO}	PxDIRn	PxINENn	ADEN	OEN	IEN
GPIO Input(Note)	1	1	1	0	1	1	1	0
GPIO Output(Note)	1	1	1	1	0 (1 if need)	1	0	1 (0)
AFIO Input	1	1	0	0	X	1	1	0
AFIO Output	1	0	1	X	0 (1 if need)	1	0	1 (0)
ADC Input	0	1	1	0	0 (1 if need)	0	1	1 (0)
OSC Output	0	1	1	0	0 (1 if need)	0	1	1 (0)

Note: The signals, IEN and OEN, for I/O pads are derived from the GPIO register bits PxINENn and PxDIRn respectively when the associated pin is configured in the GPIO input/output mode.

GPIO Locking Mechanism

The GPIO also offers a lock function to lock the port until a reset event occurs. The PxLOCKR (x=A~E) registers are used to lock the port x and lock control options. The value 0x5FA0 is written into the PxLKEY field in the PxLOCKR registers to freeze the PxDIRCR, PxINER, PxPUR, PxPDR, PxODR, PxDRVR control and AFIO mode configuration (GPxCFGR, where x=A~E). If the value in the PxLOCKR is 0x5FA0_0001, it means that the Port x Lock function is enabled and the Port x pin 0 is frozen.

Register Map

The following table shows the GPIO registers and reset values of the Port A~E.

Table 21. Register map of GPIO

Register	Offset	Description	Reset Value
GPIO A Base Address=0x4001_A000			
PADIRCR	0x000	Port A Data Direction Control Register	0x0000_0000
PAINER	0x004	Port A Input Function Enable Control Register	0x0000_0000
PAPUR	0x008	Port A Pull-Up Selection Register	0x0000_0000
PAPDR	0x00C	Port A Pull-Down Selection Register	0x0000_0000
PAODR	0x010	Port A Open Drain Selection Register	0x0000_0000
PADRVR	0x014	Port A Drive Current Selection Register	0x0000_0000
PALOCKR	0x018	Port A Lock Register	0x0000_0000
PADINR	0x01C	Port A Data Input Register	0x0000_0000
PADOUTR	0x020	Port A Data Output Register	0x0000_0000
PASRR	0x024	Port A Output Set and Reset Control Register	0x0000_0000
PARR	0x028	Port A Output Reset Control Register	0x0000_0000
GPIO B Base Address=0x4001_B000			
PBDIRCR	0x000	Port B Data Direction Control Register	0x0000_0000
PBINER	0x004	Port B Input Function Enable Control Register	0x0000_0000
PBPUR	0x008	Port B Pull-Up Selection Register	0x0000_0000
PBPDR	0x00C	Port B Pull-Down Selection Register	0x0000_0000
PBODR	0x010	Port B Open Drain Selection Register	0x0000_0000
PBLOCKR	0x018	Port B Lock Register	0x0000_0000

Register	Offset	Description	Reset Value
PBDINR	0x01C	Port B Data Input Register	0x0000_0000
PBDOUTR	0x020	Port B Data Output Register	0x0000_0000
PBSRR	0x024	Port B Output Set and Reset Control Register	0x0000_0000
PBRR	0x028	Port B Output Reset Control Register	0x0000_0000
GPIO C Base Address=0x4001_C000			
PCDIRCR	0x000	Port C Data Direction Control Register	0x0000_0000
PCINER	0x004	Port C Input Function Enable Control Register	0x0000_0300
PCPUR	0x008	Port C Pull-Up Selection Register	0x0000_0300
PCPDR	0x00C	Port C Pull-Down Selection Register	0x0000_0000
PCODR	0x010	Port C Open Drain Selection Register	0x0000_0000
PCLOCKR	0x018	Port C Lock Register	0x0000_0000
PCDINR	0x01C	Port C Data Input Register	0x0000_0000
PCDOUTR	0x020	Port C Data Output Register	0x0000_0000
PCSRR	0x024	Port C Output Set and Reset Control Register	0x0000_0000
PCRR	0x028	Port C Output Reset Control Register	0x0000_0000
GPIO D Base Address=0x4001_D000			
PDDIRCR	0x000	Port D Data Direction Control Register	0x0000_0000
PDINER	0x004	Port D Input Function Enable Control Register	0x0000_0000
PDPUR	0x008	Port D Pull-Up Selection Register	0x0000_0000
PDPDR	0x00C	Port D Pull-Down Selection Register	0x0000_0000
PDODR	0x010	Port D Open Drain Selection Register	0x0000_0000
PDLOCKR	0x018	Port D Lock Register	0x0000_0000
PDDINR	0x01C	Port D Data Input Register	0x0000_0000
PDDOUTR	0x020	Port D Data Output Register	0x0000_0000
PDSRR	0x024	Port D Output Set and Reset Control Register	0x0000_0000
PDRR	0x028	Port D Output Reset Control Register	0x0000_0000
GPIO E Base Address=0x4001_E000			
PEDIRCR	0x000	Port E Data Direction Control Register	0x0000_0000
PEINER	0x004	Port E Input Function Enable Control Register	0x0000_D000
PEPUR	0x008	Port E Pull-Up Selection Register	0x0000_E000
PEPDR	0x00C	Port E Pull-Down Selection Register	0x0000_1000
PEODR	0x010	Port E Open Drain Selection Register	0x0000_0000
PEDRVR	0x014	Port E Drive Current Selection Register	0x0000_0000
PELOCKR	0x018	Port E Lock Register	0x0000_0000
PEDINR	0x01C	Port E Data Input Register	0x0000_0000
PEDOUTR	0x020	Port E Data Output Register	0x0000_0000
PESRR	0x024	Port E Output Set and Reset Control Register	0x0000_0000
PERR	0x028	Port E Output Reset Control Register	0x0000_0000

Register Descriptions

Port A Data Direction Control Register – PADIRCR

This register is used to control the direction of the GPIO Port A pin as input or output.

Offset: 0x000

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	PADIR							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	PADIR							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	PADIRn	GPIO Port A pin n Direction Control Bits (n=0~15) 0: Pin n is input mode 1: Pin n is output mode

Port A Input Function Enable Control Register – PAINER

This register is used to enable or disable the GPIO Port A input function.

Offset: 0x004

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	PAINEN							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	PAINEN							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	PAINENn	GPIO Port A pin n Input Enable Control Bits (n=0~15) 0: Pin n input function is disabled 1: Pin n input function is enabled When the pin n input function is disabled, the input Schmitt trigger will be turned off and the Schmitt trigger output will remain at a zero state.

Port A Pull-Up Selection Register – PAPUR

This register is used to enable or disable the GPIO Port A pull-up function.

Offset: 0x008

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	Reserved							
Type/Reset								
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PAPU							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	PAPU							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	PAPUn	GPIO Port A pin n Pull-Up Selection Control Bits (n=0~15) 0: Pin n pull-up function is disabled 1: Pin n pull-up function is enabled **Note:** When the pull-up and pull-down functions are both enabled, the pull-up function will have the higher priority and therefore the pull-down function will be blocked and disabled.

Port A Pull-Down Selection Register – PAPDR

This register is used to enable or disable the GPIO Port A pull-down function.

Offset: 0x00C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	Reserved							
Type/Reset								
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PAPD							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	PAPD							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	PAPDn	GPIO Port A pin n Pull-Down Selection Control Bits (n=0~15) 0: Pin n pull-down function is disabled 1: Pin n pull-down function is enabled **Note:** When the pull-up and pull-down functions are both enabled, the pull-up function will have the higher priority and therefore the pull-down function will be blocked and disabled.

Port A Open Drain Selection Register – PAODR

This register is used to enable or disable the GPIO Port A open drain function.

Offset: 0x010

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	PAOD							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	PAOD							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	PAODn	GPIO Port A pin n Open Drain Selection Control Bits (n=0~15) 0: Pin n Open Drain output is disabled (The output type is CMOS output) 1: Pin n Open Drain output is enabled (The output type is open-drain output)

Port A Output Current Drive Selection Register – PADRVR

This register specifies the GPIO Port A output driving current.

Offset: 0x014

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	PADV							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[7:0]	PADVn	GPIO Port A pin n Output Current Drive Selection Control Bits (n=0~7) 0: 4mA source/sink current 1: 8mA source/sink current

Port A Lock Register – PALOCKR

This register specifies the GPIO Port A lock configuration.

Offset: 0x018

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	PALKEY							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	PALKEY							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PALOCK							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	PALOCK							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[31:16]	PALKEY	GPIO Port A Lock Key 0x5FA0: Port A Lock function is enable Others: Port A Lock function is disable To lock the Port A function, a value 0x5FA0 should be written into the PALKEY field in this register. To execute a successful write operation on this lock register, the value written into the PALKEY field must be 0x5FA0. If the value written into this field is not equal to 0x5FA0, any write operations on the PALOCKR register will be aborted. The result of a read operation on the PALKEY field returns the GPIO Port A Lock Status which indicates whether the GPIO Port A is locked or not. If the read value of the PALKEY field is 0, this indicates that the GPIO Port A Lock function is disabled. Otherwise, it indicates that the GPIO Port A Lock function is enabled as the read value is equal to 1.
[15:0]	PALOCKn	GPIO Port A Pin n Lock Control Bits (n=0~15) 0: Port A Pin n is not locked 1: Port A Pin n is locked The PALOCKn bits are used to lock the configurations of corresponding GPIO Pins when the correct Lock Key is applied to the PALKEY field. The locked configurations including PADIRn, PAINENn, PAPUn, PAPDn, PAODn and PADVn setting in the related GPIO registers. Additionally, the GPACFGR field which is used to configure the alternative function of the associated GPIO pin will also be locked. Note that the PALOCKR can only be written once which means that PALKEY and PALOCKn (lock control bit) should be written together and can not be changed until a system reset or GPIO Port A reset occurs.

Port A Data Input Register – PADINR

This register specifies the GPIO Port A input data.

Offset: 0x01C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	PADIN							
Type/Reset	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0
	7	6	5	4	3	2	1	0
	PADIN							
Type/Reset	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0

Bits	Field	Descriptions
[15:0]	PADINn	GPIO Port A pin n Data Input Bits (n=0~15) 0: The input data of pin is 0 1: The input data of pin is 1

Port A Output Data Register – PADOUTR

This register specifies the GPIO Port A output data.

Offset: 0x020

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	PADOUT							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	PADOUT							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	PADOUTn	GPIO Port A pin n Data Output Bits (n=0~15) 0: Data to be output on pin n is 0 1: Data to be output on pin n is 1

Port A Output Set/Reset Control Register – PASRR

This register is used to set or reset the corresponding bit of the GPIO Port A output data.

Offset: 0x024

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	PARST							
Type/Reset	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0
	23	22	21	20	19	18	17	16
	PARST							
Type/Reset	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0
	15	14	13	12	11	10	9	8
	PASET							
Type/Reset	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0
	7	6	5	4	3	2	1	0
	PASET							
Type/Reset	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0

Bits	Field	Descriptions
[31:16]	PARSTn	GPIO Port A pin n Output Reset Control Bits (n=0~15) 0: No effect on the PADOUTn bit 1: Reset the PADOUTn bit
[15:0]	PASETn	GPIO Port A pin n Output Set Control Bits (n=0~15) 0: No effect on the PADOUTn bit 1: Set the PADOUTn bit Note that the function enabled by the PASETn bit has the higher priority if both the PASETn and PARSTn bits are set at the same time.

Port A Output Reset Register – PARR

This register is used to reset the corresponding bit of the GPIO Port A output data.

Offset: 0x028

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	PARST							
Type/Reset	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0
	7	6	5	4	3	2	1	0
	PARST							
Type/Reset	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0

Bits	Field	Descriptions
[15:0]	PARSTn	GPIO Port A pin n Output Reset Bits (n=0~15) 0: No effect on the PADOUTn bit 1: Reset the PADOUTn bit

Port B Data Direction Control Register – PBDIRCR

This register is used to control the direction of GPIO Port B pin as input or output.

Offset: 0x000

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	PBDIR							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	PBDIR							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	PBDIRn	GPIO Port B pin n Direction Control Bits (n=0~15) 0: Pin n is input mode 1: Pin n is output mode

Port B Input Function Enable Control Register – PBINER

This register is used to enable or disable the GPIO Port B input function.

Offset: 0x004

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	PBINEN							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	PBINEN							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	PBINENn	GPIO Port B pin n Input Enable Control Bits (n=0~15) 0: Pin n input function is disabled 1: Pin n input function is enabled When the pin n input function is disabled, the input Schmitt trigger will be turned off and the Schmitt trigger output will remain at a zero state.

Port B Pull-Up Selection Register – PBPUR

This register is used to enable or disable the GPIO Port B pull-up function.

Offset: 0x008

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	Reserved							
Type/Reset								
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PBPU							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	PBPU							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	PBPUn	GPIO Port B pin n Pull-Up Selection Control Bits (n=0~15) 0: Pin n pull-up function is disabled 1: Pin n pull-up function is enabled **Note:** When the pull-up and pull-down functions are both enabled, the pull-up function will have the higher priority and therefore the pull-down function will be blocked and disabled.

Port B Pull-Down Selection Register – PBPDR

This register is used to enable or disable the GPIO Port B pull-down function.

Offset: 0x00C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	Reserved							
Type/Reset								
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PBPD							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	PBPD							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	PBPDn	GPIO Port B pin n Pull-Down Selection Control Bits (n=0~15) 0: Pin n pull-down function is disabled 1: Pin n pull-down function is enabled **Note:** When the pull-up and pull-down functions are both enabled, the pull-up function will have the higher priority and therefore the pull-down function will be blocked and disabled.

Port B Open Drain Selection Register – PBODR

This register is used to enable or disable the GPIO Port B open drain function.

Offset: 0x010

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	PBOD							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	PBOD							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	PBODn	GPIO Port B pin n Open Drain Selection Control Bits (n=0~15) 0: Pin n Open Drain output is disabled (The output type is CMOS output) 1: Pin n Open Drain output is enabled (The output type is open-drain output)

Port B Lock Register – PBLOCKR

This register specifies the GPIO Port B lock configuration.

Offset: 0x018

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	PBLKEY							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	PBLKEY							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PBLOCK							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	PBLOCK							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[31:16]	PBLKEY	GPIO Port B lock Key 0x5FA0: Port B lock function is enable Others: Port B lock function is disable To lock the Port B function, a value 0x5FA0 should be written into the PBLKEY field in this register. To execute a successful write operation on this lock register, the value written into the PBLKEY field must be 0x5FA0. If the value written into this field is not equal to 0x5FA0, any write operations on the PBLOCKR register will be aborted. The result of a read operation on the PBLKEY field returns the GPIO Port B Lock Status which indicates whether the GPIO Port B is locked or not. If the read value of the PBLKEY field is 0, this indicates that the GPIO Port B Lock function is disabled. Otherwise, it indicates that the GPIO Port B Lock function is enabled as the read value is equal to 1.
[15:0]	PBLOCKn	GPIO Port B pin n Lock Control Bits (n=0~15) 0: Port B pin n is not locked 1: Port B pin n is locked The PBLOCKn bits are used to lock the configurations of corresponding GPIO Pins when the correct Lock Key is applied to the PBLKEY field. The locked configurations including PBDIRn, PBINENn, PBPUn, PBPDn and PBODn setting in the related GPIO registers. Additionally, the GPBCFGR field which is used to configure the alternative function of the associated GPIO pin will also be locked. Note that the PBLOCKR can only be written once which means that PBLKEY and PBLOCKn (lock control bit) should be written together and can not be changed until a system reset or GPIO Port B reset occurs.

Port B Data Input Register – PBDINR

This register specifies the GPIO Port B input data.

Offset: 0x01C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	PBDIN							
Type/Reset	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0
	7	6	5	4	3	2	1	0
	PBDIN							
Type/Reset	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0

Bits	Field	Descriptions
[15:0]	PBDINn	GPIO Port B pin n Data Input Bits (n=0~15) 0: The input data of corresponding pin is 0 1: The input data of corresponding pin is 1

Port B Output Data Register – PBDOUTR

This register specifies the GPIO Port B output data.

Offset: 0x020

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	PBDOUT							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	PBDOUT							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	PBDOUTn	GPIO Port B pin n Data Output Bits (n=0~15) 0: Data to be output on pin n is 0 1: Data to be output on pin n is 1

Port B Output Set/Reset Control Register – PBSRR

This register is used to set or reset the corresponding bit of the GPIO Port B output data.

Offset: 0x024

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	PBRST							
Type/Reset	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0
	23	22	21	20	19	18	17	16
	PBRST							
Type/Reset	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0
	15	14	13	12	11	10	9	8
	PBSET							
Type/Reset	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0
	7	6	5	4	3	2	1	0
	PBSET							
Type/Reset	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0

Bits	Field	Descriptions
[31:16]	PBRSTn	GPIO Port B pin n Output Reset Control Bits (n=0~15) 0: No effect on the PBDOUTn bit 1: Reset the PBDOUTn bit
[15:0]	PBSETn	GPIO Port B pin n Output Set Control Bits (n=0~15) 0: No effect on the PBDOUTn bit 1: Set the PBDOUTn bit Note that the function enabled by the PBSETn bit has the higher priority if both the PBSETn and PBRSTn bits are set at the same time.

Port B Output Reset Register – PBRR

This register is used to reset the corresponding bit of the GPIO Port B output data.

Offset: 0x028

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	PBRST							
Type/Reset	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0
	7	6	5	4	3	2	1	0
	PBRST							
Type/Reset	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0

Bits	Field	Descriptions
[15:0]	PBRSTn	GPIO Port B pin n Output Reset Bits (n=0~15) 0: No effect on the PBDOUTn bit 1: Reset the PBDOUTn bit

Port C Data Direction Control Register – PCDIRCR

This register is used to control the direction of GPIO Port C pin as input or output.

Offset: 0x000

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	PCDIR							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	PCDIR							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	PCDIRn	GPIO Port C pin n Direction Control Bits (n=0~15) 0: Pin n is input mode 1: Pin n is output mode

Port C Input Function Enable Control Register – PCINER

This register is used to enable or disable the GPIO Port C input function.

Offset: 0x004

Reset value: 0x0000_0300

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	PCINEN							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 1	RW 1
	7	6	5	4	3	2	1	0
	PCINEN							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	PCINENn	GPIO Port C pin n Input Enable Control Bits (n=0~15) 0: Pin n input function is disabled 1: Pin n input function is enabled When the pin n input function is disabled, the input Schmitt trigger will be turned off and the Schmitt trigger output will remain at a zero state.

Port C Pull-Up Selection Register – PCPUR

This register is used to enable or disable the GPIO Port C pull-up function.

Offset: 0x008

Reset value: 0x0000_0300

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	Reserved							
Type/Reset								
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PCPU							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 1	RW 1
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	PCPU							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	PCPUn	GPIO Port C pin n Pull-Up Selection Control Bits (n=0~15) 0: Pin n pull-up function is disabled 1: Pin n pull-up function is enabled **Note:** When the pull-up and pull-down functions are both enabled, the pull-up function will have the higher priority and therefore the pull-down function will be blocked and disabled.

Port C Pull-Down Selection Register – PCPDR

This register is used to enable or disable the GPIO Port C pull-down function.

Offset: 0x00C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	Reserved							
Type/Reset								
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PCPD							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	PCPD							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	PCPDn	GPIO Port C pin n Pull-Down Selection Control Bits (n=0~15) 0: Pin n pull-down function is disabled 1: Pin n pull-down function is enabled **Note:** When the pull-up and pull-down functions are both enabled, the pull-up function will have the higher priority and therefore the pull-down function will be blocked and disabled.

Port C Open Drain Selection Register – PCODR

This register is used to enable or disable the GPIO Port C open drain function.

Offset: 0x010

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	PCOD							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	PCOD							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	PCODn	GPIO Port C pin n Open Drain Selection Control Bits (n=0~15) 0: Pin n Open Drain output is disabled (The output type is CMOS output) 1: Pin n Open Drain output is enabled (The output type is open-drain output)

Port C Lock Register – PCLOCKR

This register specifies the GPIO Port C lock configuration.

Offset: 0x018

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	PCLKEY							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	PCLKEY							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PCLOCK							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	PCLOCK							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[31:16]	PCLKEY	GPIO Port C lock Key 0x5FA0: Port C Lock function is enable Others: Port C Lock function is disable To lock the Port C function, a value 0x5FA0 should be written into the PCLKEY field in this register. To execute a successful write operation on this lock register, the value written into the PCLKEY field must be 0x5FA0. If the value written into this field is not equal to 0x5FA0, any write operations on the PCLOCKR register will be aborted. The result of a read operation on the PCLKEY field returns the GPIO Port C Lock Status which indicates whether the GPIO Port C is locked or not. If the read value of the PCLKEY field is 0, this indicates that the GPIO Port C Lock function is disabled. Otherwise, it indicates that the GPIO Port C Lock function is enabled as the read value is equal to 1.
[15:0]	PCLOCKn	GPIO Port C pin n Lock Control Bits (n=0~15) 0: Port C pin n is not locked 1: Port C pin n is locked The PCLOCKn bits are used to lock the configurations of corresponding GPIO Pins when the correct Lock Key is applied to the PxCKEY field. The locked configurations including PCDIRn, PCINENn, PCPUn, PCPDn and PCODn setting in the related GPIO registers. Additionally, the GPCCFGR field which is used to configure the alternative function of the associated GPIO pin will also be locked. Note that the PCLOCKR can only be written once which means that PCLKEY and PCLOCKn (lock control bit) should be written together and can not be changed until a system reset or GPIO Port C reset occurs.

Port C Data Input Register – PCDINR

This register specifies the GPIO Port C input data.

Offset: 0x01C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	PCDIN							
Type/Reset	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0
	7	6	5	4	3	2	1	0
	PCDIN							
Type/Reset	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0

Bits	Field	Descriptions
[15:0]	PCDINn	GPIO Port C pin n Data Input Bits (n=0~15) 0: The input data of corresponding pin is 0 1: The input data of corresponding pin is 1

Port C Output Data Register – PCDOUTR

This register specifies the GPIO Port C output data.

Offset: 0x020

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	Reserved							
Type/Reset								
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PCDOUT							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	PCDOUT							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	PCDOUTn	GPIO Port C pin n Data Output Bits (n=0~15) 0: Data to be output on pin n is 0 1: Data to be output on pin n is 1

Port C Output Set/Reset Control Register – PCSRR

This register is used to set or reset the corresponding bit of the GPIO Port C output data.

Offset: 0x024

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	PCRST							
Type/Reset	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0
	23	22	21	20	19	18	17	16
	PCRST							
Type/Reset	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0
	15	14	13	12	11	10	9	8
	PCSET							
Type/Reset	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0
	7	6	5	4	3	2	1	0
	PCSET							
Type/Reset	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0

Bits	Field	Descriptions
[31:16]	PCRSTn	GPIO Port C pin n Output Reset Control Bits (n=0~15) 0: No effect on the PCDOUTn bit 1: Reset the PCDOUTn bit
[15:0]	PCSETn	GPIO Port C pin n Output Set Control Bits (n=0~15) 0: No effect on the PCDOUTn bit 1: Set the PCDOUTn bit Note that the function enabled by the PCSETn bit has the higher priority if both the PCSETn and PCRSTn bits are set at the same time.

Port C Output Reset Register – PCRR

This register is used to reset the corresponding bit of the GPIO Port C output data.

Offset: 0x028

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	PCRST							
Type/Reset	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0
	7	6	5	4	3	2	1	0
	PCRST							
Type/Reset	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0

Bits	Field	Descriptions
[15:0]	PCRSTn	GPIO Port C pin n Output Reset Bits (n=0~15) 0: No effect on the PCDOUTn bit 1: Reset the PCDOUTn bit

Port D Data Direction Control Register – PDDIRCR

This register is used to control the direction of GPIO Port D pin as input or output.

Offset: 0x000

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	PDDIR							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	PDDIR							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	PDDIRn	GPIO Port D pin n Direction Control Bits (n=0~15) 0: Pin n is input mode 1: Pin n is output mode

Port D Input Function Enable Control Register – PDINER

This register is used to enable or disable the GPIO Port D input function.

Offset: 0x004

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	PDINEN							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	PDINEN							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	PDINENn	GPIO Port D pin n Input Enable Control Bits (n=0~15) 0: Pin n input function is disabled 1: Pin n input function is enabled When the pin n input function is disabled, the input Schmitt trigger will be turned off and the Schmitt trigger output will remain at a zero state.

Port D Pull-Up Selection Register – PDPUR

This register is used to enable or disable the GPIO Port D pull-up function.

Offset: 0x008

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	Reserved							
Type/Reset								
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PDPU							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	PDPU							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	PDPUn	GPIO Port D pin n Pull-Up Selection Control Bits (n=0~15) 0: Pin n pull-up function is disabled 1: Pin n pull-up function is enabled **Note:** When the pull-up and pull-down functions are both enabled, the pull-up function will have the higher priority and therefore the pull-down function will be blocked and disabled.

Port D Pull-Down Selection Register – PDPDR

This register is used to enable or disable the GPIO Port D pull-down function.

Offset: 0x00C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	Reserved							
Type/Reset								
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PDPD							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	PDPD							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	PDPDn	GPIO Port D pin n Pull-Down Selection Control Bits (n=0~15) 0: Pin n pull-down function is disabled 1: Pin n pull-down function is enabled **Note:** When the pull-up and pull-down functions are both enabled, the pull-up function will have the higher priority and therefore the pull-down function will be blocked and disabled.

Port D Open Drain Selection Register – PDODR

This register is used to enable or disable the GPIO Port D open drain function.

Offset: 0x010

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	Reserved							
Type/Reset								
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PDOD							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	PDOD							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	PDODn	GPIO Port D pin n Open Drain Selection Control Bits (n=0~15) 0: Pin n Open Drain output is disabled (The output type is CMOS output) 1: Pin n Open Drain output is enabled (The output type is open-drain output)

Port D Lock Register – PDLOCKR

This register specifies the GPIO Port D lock configuration.

Offset: 0x018

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	PDLKEY							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	PDLKEY							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PDLOCK							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	PDLOCK							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[31:16]	PDLKEY	GPIO Port D Lock Key 0x5FA0: Port D Lock function is enable Others: Port D Lock function is disable To lock the Port D function, a value 0x5FA0 should be written into the PDLKEY field in this register. To execute a successful write operation on this lock register, the value written into the PDLKEY field must be 0x5FA0. If the value written into this field is not equal to 0x5FA0, any write operations on the PDLOCKR register will be aborted. The result of a read operation on the PDLKEY field returns the GPIO Port D Lock Status which indicates whether the GPIO Port D is locked or not. If the read value of the PDLKEY field is 0, this indicates that the GPIO Port D Lock function is disabled. Otherwise, it indicates that the GPIO Port D Lock function is enabled as the read value is equal to 1.
[15:0]	PDLOCKn	GPIO Port D pin n Lock Control Bits (n=0~15) 0: Port D pin n is not locked 1: Port D pin n is locked The PDLOCKn bits are used to lock the configurations of corresponding GPIO Pins when the correct Lock Key is applied to the PDLKEY field. The locked configurations including PDDIRn, PDINENn, PDPUn, PDPDn and PDODn setting in the related GPIO registers. Additionally, the GPDCFGR field which is used to configure the alternative function of the associated GPIO pin will also be locked. Note that the PDLOCKR can only be written once which means that PDLKEY and PDLOCKn (lock control bit) should be written together and can not be changed until a system reset or GPIO Port D reset occurs.

Port D Data Input Register – PDDINR

This register specifies the GPIO Port D input data.

Offset: 0x01C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	PDDIN							
Type/Reset	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0
	7	6	5	4	3	2	1	0
	PDDIN							
Type/Reset	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0

Bits	Field	Descriptions
[15:0]	PDDINn	GPIO Port D pin n Data Input Bits (n=0~15) 0: The input data of corresponding pin is 0 1: The input data of corresponding pin is 1

Port D Output Data Register – PDDOUTR

This register specifies the GPIO Port D output data.

Offset: 0x020

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	PDDOUT							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	PDDOUT							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	PDDOUTn	GPIO Port D pin n Data Output Bits (n=0~15) 0: Data to be output on pin n is 0 1: Data to be output on pin n is 1

Port D Output Set/Reset Control Register – PDSRR

This register is used to set or reset the corresponding bit of the GPIO Port D output data.

Offset: 0x024

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	PDRST							
Type/Reset	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0
	23	22	21	20	19	18	17	16
	PDRST							
Type/Reset	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0
	15	14	13	12	11	10	9	8
	PDSET							
Type/Reset	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0
	7	6	5	4	3	2	1	0
	PDSET							
Type/Reset	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0

Bits	Field	Descriptions
[31:16]	PDRSTn	GPIO Port D pin n Output Reset Control Bits (n=0~15) 0: No effect on the PDDOUTn bit 1: Reset the PDDOUTn bit
[15:0]	PDSETn	GPIO Port D pin n Output Set Control Bits (n=0~15) 0: No effect on the PDDOUTn bit 1: Set the PDDOUTn bit Note that the function enabled by the PDSETn bit has the higher priority if both the PDSETn and PDRSTn bits are set at the same time.

Port D Output Reset Register – PDRR

This register is used to reset the corresponding bit of the GPIO Port D output data.

Offset: 0x028

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	PDRST							
Type/Reset	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0
	7	6	5	4	3	2	1	0
	PDRST							
Type/Reset	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0

Bits	Field	Descriptions
[15:0]	PDRSTn	GPIO Port D pin n Output Reset Bits (n=0~15) 0: No effect on the PDDOUTn bit 1: Reset the PDDOUTn bit

Port E Data Direction Control Register – PEDIRCR

This register is used to control the direction of GPIO Port E pin as input or output.

Offset: 0x000

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	PEDIR							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	PEDIR							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	PEDIRn	GPIO Port E pin n Direction Control Bits (n=0~15) 0: Pin n is input mode 1: Pin n is output mode

Port E Input Function Enable Control Register – PEINER

This register is used to enable or disable the GPIO Port E input function.

Offset: 0x004

Reset value: 0x0000_D000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	PEINEN							
Type/Reset	RW 1	RW 1	RW 0	RW 1	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	PEINEN							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	PEINENn	GPIO Port E pin n Input Enable Control Bits (n=0~15) 0: Pin n input function is disabled 1: Pin n input function is enabled When the pin n input function is disabled, the input Schmitt trigger will be turned off and the Schmitt trigger output will remain at a zero state.

Port E Pull-Up Selection Register – PEPUR

This register is used to enable or disable the GPIO Port E pull-up function.

Offset: 0x008

Reset value: 0x0000_E000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	Reserved							
Type/Reset								
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PEPU							
Type/Reset	RW 1	RW 1	RW 1	RW 0	RW 0	RW 0	RW 0	RW 0
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	PEPU							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	PEPUn	GPIO Port E pin n Pull-Up Selection Control Bits (n=0~15) 0: Pin n pull-up function is disabled 1: Pin n pull-up function is enabled **Note:** When the pull-up and pull-down functions are both enabled, the pull-up function will have the higher priority and therefore the pull-down function will be blocked and disabled.

Port E Pull-Down Selection Register – PEPDR

This register is used to enable or disable the GPIO Port E pull-down function.

Offset: 0x00C

Reset value: 0x0000_1000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	Reserved							
Type/Reset								
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PEPD							
Type/Reset	RW 0	RW 0	RW 0	RW 1	RW 0	RW 0	RW 0	RW 0
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	PEPD							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	PEPDn	GPIO Port E pin n Pull-Down Selection Control Bits (n=0~15) 0: Pin n pull-down function is disabled 1: Pin n pull-down function is enabled **Note:** When the pull-up and pull-down functions are both enabled, the pull-up function will have the higher priority and therefore the pull-down function will be blocked and disabled.

Port E Open Drain Selection Register – PEODR

This register is used to enable or disable the GPIO Port E open drain function.

Offset: 0x010

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	PEOD							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	PEOD							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	PEODn	GPIO Port E pin n Open Drain Selection Control Bits (n=0~15) 0: Pin n Open Drain output is disabled (The output type is CMOS output) 1: Pin n Open Drain output is enabled (The output type is open-drain output)

Port E Output Current Drive Selection Register – PEDRVR

This register specifies the GPIO Port E output driving current.

Offset: 0x014

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved					PEDV		
Type/Reset								
	7	6	5	4	3	2	1	0
	PEDV			Reserved				
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[10:5]	PEDVn	GPIO Port E pin n Output Current Drive Selection Control Bits (n=5~10) 0: 4mA source/sink current 1: 8mA source/sink current

Port E Lock Register – PELOCKR

This register specifies the GPIO Port E lock configuration.

Offset: 0x018

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	PELKEY							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	PELKEY							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PELOCK							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	PELOCK							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[31:16]	PELKEY	GPIO Port E Lock Key 0x5FA0: Port E Lock function is enable Others: Port E Lock function is disable To lock the Port E function, a value 0x5FA0 should be written into the PELKEY field in this register. To execute a successful write operation on this lock register, the value written into the PELKEY field must be 0x5FA0. If the value written into this field is not equal to 0x5FA0, any write operations on the PELOCKR register will be aborted. The result of a read operation on the PELKEY field returns the GPIO Port E Lock Status which indicates whether the GPIO Port E is locked or not. If the read value of the PELKEY field is 0, this indicates that the GPIO Port E Lock function is disabled. Otherwise, it indicates that the GPIO Port E Lock function is enabled as the read value is equal to 1.
[15:0]	PELOCKn	GPIO Port E pin n Lock Control Bits (n=0~15) 0: Port E pin n is not locked 1: Port E pin n is locked The PELOCKn bits are used to lock the configurations of corresponding GPIO Pins when the correct Lock Key is applied to the PELKEY field. The locked configurations including PEDIRn, PEINENn, PEPUn, PEPDn, PEODn and PEDVn setting in the related GPIO registers. Additionally, the GPECFGR field which is used to configure the alternative function of the associated GPIO pin will also be locked. Note that the PELOCKR can only be written once which means that PELKEY and PELOCKn (lock control bit) should be written together and can not be changed until a system reset or GPIO Port E reset occurs.

Port E Data Input Register – PEDINR

This register specifies the GPIO Port E input data.

Offset: 0x01C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	PEDIN							
Type/Reset	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0
	7	6	5	4	3	2	1	0
	PEDIN							
Type/Reset	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0

Bits	Field	Descriptions
[15:0]	PEDINn	GPIO Port E pin n Data Input Bits (n=0~15) 0: The input data of corresponding pin is 0 1: The input data of corresponding pin is 1

Port E Output Data Register – PEDOUTR

This register specifies the GPIO Port E input data.

Offset: 0x020

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	PEDOUT							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	PEDOUT							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	PEDOUTn	GPIO Port E pin n Data Output Bits (n=0~15) 0: Data to be output on pin n is 0 1: Data to be output on pin n is 1

Port E Output Set/Reset Control Register – PESRR

This register is used to set or reset the corresponding bit of the GPIO Port E output data.

Offset: 0x024

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	PERST							
Type/Reset	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0
	23	22	21	20	19	18	17	16
	PERST							
Type/Reset	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0
	15	14	13	12	11	10	9	8
	PESET							
Type/Reset	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0
	7	6	5	4	3	2	1	0
	PESET							
Type/Reset	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0

Bits	Field	Descriptions
[31:16]	PERSTn	GPIO Port E pin n Output Reset Control Bits (n=0~15) 0: No effect on the PEDOUTn bit 1: Reset the PEDOUTn bit
[15:0]	PESETn	GPIO Port E pin n Output Set Control Bits (n=0~15) 0: No effect on the PEDOUTn bit 1: Set the PEDOUTn bit Note that the function enabled by the PESETn bit has the higher priority if both the PESETn and PERSTn bits are set at the same time.

Port E Output Reset Register – PERR

This register is used to reset the corresponding bit of the GPIO Port E output data.

Offset: 0x028

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	PERST							
Type/Reset	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0
	7	6	5	4	3	2	1	0
	PERST							
Type/Reset	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0

Bits	Field	Descriptions
[15:0]	PERSTn	GPIO Port E pin n Output Reset Bits (n=0~15) 0: No effect on the PEDOUTn bit 1: Reset the PEDOUTn bit

9 Alternate Function I/O Control Unit (AFIO)

Introduction

In order to expand the flexibility of the GPIO or the usage of peripheral functions, each I/O pin can be configured to have up to four different functions such as GPIO or IP functions by setting the GPxCFGR register where x is the different port name. According to the usage of the IP resource and application requirements, suitable pin-out locations can be selected by using the peripheral I/O remapping mechanism. Additionally, various GPIO pins can be selected to be the EXTI interrupt line by setting the EXTInPIN [3:0] field in the ESSRn register to trigger an interrupt or event. Please refer to the EXTI section for more details.

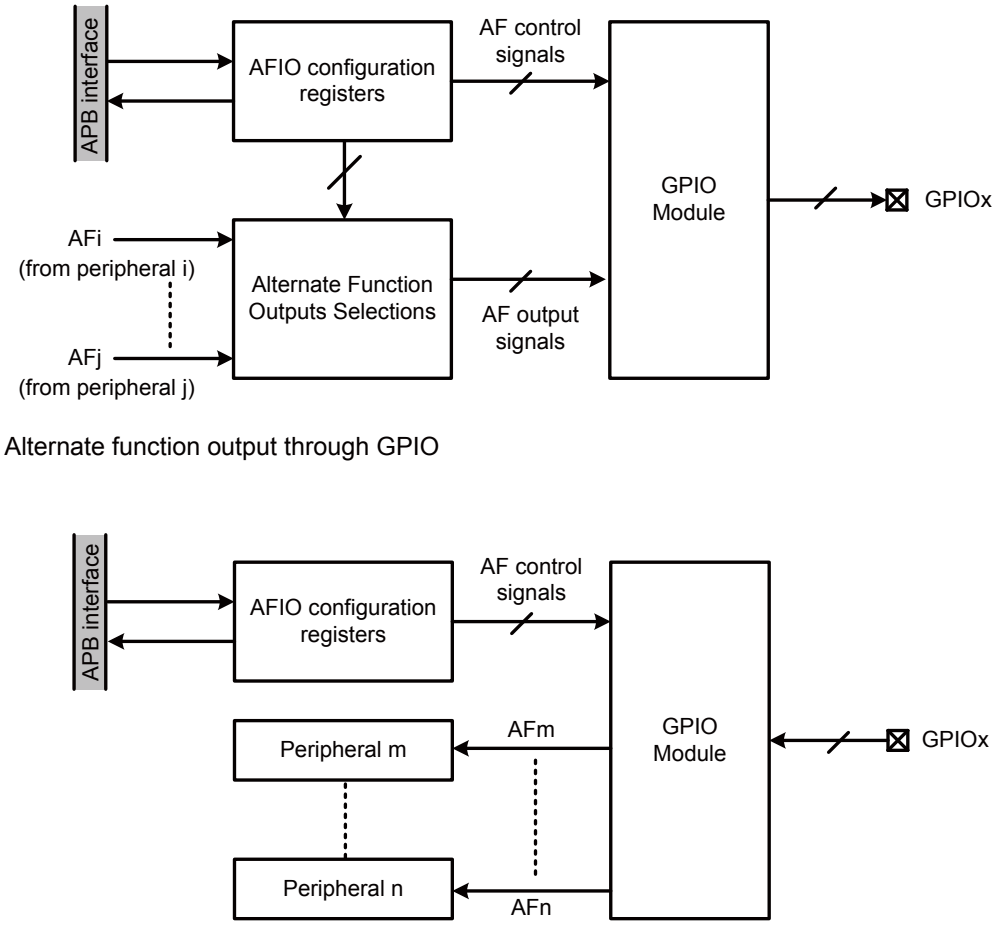


Figure 20. AFIO Block Diagram

Features

- APB slave interface for register access
- EXTI source selection
- Configurable pin function for each GPIO, up to four alternative functions on each pin

Functional Descriptions

External Interrupt Pin Selection

The GPIO pins are connected to the 16 EXTI lines as shown in the accompanying figure. For example, the user can set the EXTI0PIN [3:0] field in the ESSR0 register to b0000 to select the GPIO PA0 pin as EXTI line 0 input. Since not all the pins of the Port A~E pins are available in all package types, please refer to the pin assignment section for detailed pin information. The setting of the EXTInPIN [3:0] field is invalid when the corresponding pin is not available.

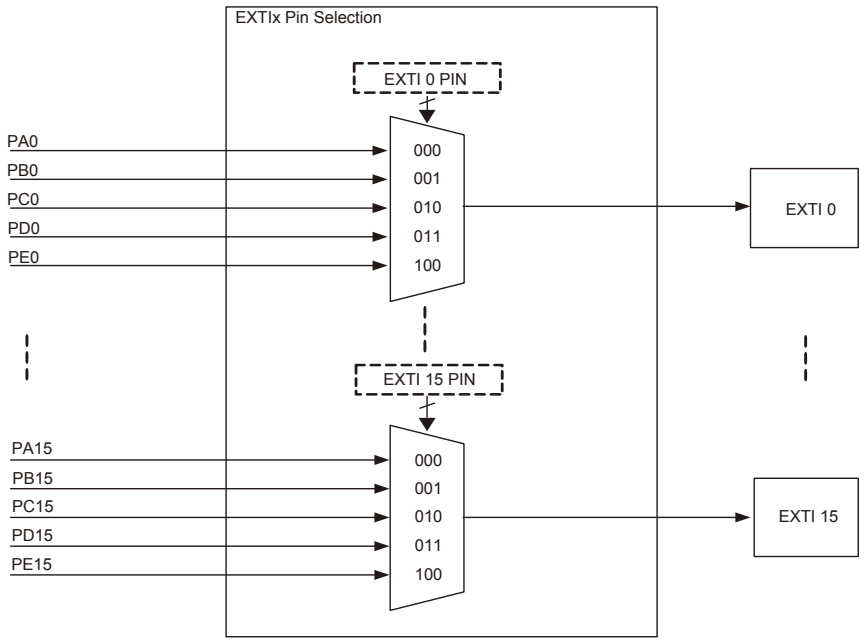


Figure 21. EXTI Channel Input Selection

Alternate Function

Up to four alternative functions can be chosen for each I/O pad by setting the PxCFGn [1:0] field in the GPxCFGR (x=A~E) register. Refer to the register description section for detailed AFIO assignments. The following description shows the setting of the PxCFGn [1:0] field. Note that if the Operational Amplifier/Comparator is active, then pins PE [7:5] or PE [10:8] can not be set as other AFIO functional pins simultaneously.

- PxCFGn [1:0]=00: The default alternated function (after reset).
- PxCFGn [1:0]=01: Alternate Function 1
- PxCFGn [1:0]=10: Alternate Function 2
- PxCFGn [1:0]=11: Alternate Function 3

Register Map

The following table shows the AFIO register and reset value.

Table 22. AFIO Register Map

Register	Offset	Description	Reset Value
AFIO Base Address=0x4002_2000			
ESSR0	0x000	EXTI Source Selection Register 0	0x0000_0000
ESSR1	0x004	EXTI Source Selection Register 1	0x0000_0000
GPACFGR	0x008	GPIO Port A Configuration Register	0x0000_0000
GPBCFGR	0x00C	GPIO Port B Configuration Register	0x0000_0000
GPCCFGR	0x010	GPIO Port C Configuration Register	0x0000_0000
GPDCFGR	0x014	GPIO Port D Configuration Register	0x0000_0000
GPECFGR	0x018	GPIO Port E Configuration Register	0x0000_0000

Register Descriptions

EXTI Source Selection Register 0 – ESSR0

This register specifies the I/O selection of EXTI0~EXTI7.

Offset: 0x000

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	EXTI7PIN				EXTI6PIN			
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	EXTI5PIN				EXTI4PIN			
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	EXTI3PIN				EXTI2PIN			
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	EXTI1PIN				EXTI0PIN			
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[31:0]	EXTInPIN[3:0]	EXTIn Pin Selection (n=0~7) 0000: PA Bit n is selected as EXTIn source signal 0001: PB Bit n is selected as EXTIn source signal 0010: PC Bit n is selected as EXTIn source signal 0011: PD Bit n is selected as EXTIn source signal 0100: PE Bit n is selected as EXTIn source signal Others: Reserved **Note:** Since not all GPIO pins are available in all products and package types, refer to the pin assignment section for detailed pin information. The EXTInPIN [3:0] field setting is invalid when the corresponding pin is not available.

EXTI Source Selection Register 1 – ESSR1

This register specifies the I/O selection of EXTI8~EXTI15.

Offset: 0x004

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	EXTI15PIN				EXTI14PIN			
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	23	22	21	20	19	18	17	16
	EXTI13PIN				EXTI12PIN			
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
	EXTI11PIN				EXTI10PIN			
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	EXTI9PIN				EXTI8PIN			
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[31:0]	EXTInPIN[3:0]	EXTIn Pin Selection (n=8~15) 0000: PA Bit n is selected as EXTIn source signal 0001: PB Bit n is selected as EXTIn source signal 0010: PC Bit n is selected as EXTIn source signal 0011: PD Bit n is selected as EXTIn source signal 0100: PE Bit n is selected as EXTIn source signal Others: Reserved **Note:** Since not all Port GPIO pins are available in all products and package types, please refer to the pin assignment section for detailed pin information. The EXTInPIN [3:0] field setting is invalid when the corresponding pin is not available.

GPIO A Configuration Register – GPACFGR

This register specifies the GPIO Port A pin alternative function.

Offset: 0x008

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	PACFG15		PACFG14		PACFG13		PACFG12	
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	23	22	21	20	19	18	17	16
	PACFG11		PACFG10		PACFG9		PACFG8	
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
	PACFG7		PACFG6		PACFG5		PACFG4	
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	PACFG3		PACFG2		PACFG1		PACFG0	
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[31:30]	PACFG15	Port A pin 15 AFIO Configuration

PACFG15 [1:0]	Function
00	PA15
01	GT1_CH3
10	Reserved
11	Reserved

[29:28] PACFG14 Port A pin 14 AFIO Configuration

PACFG14 [1:0]	Function
00	PA14
01	GT1_CH2
10	Reserved
11	Reserved

[27:26] PACFG13 Port A pin 13 AFIO Configuration

PACFG13 [1:0]	Function
00	PA13
01	GT1_CH1
10	Reserved
11	Reserved

Bits	Field	Descriptions
[25:24]	PACFG12	Port A pin 12 AFIO Configuration

PACFG12 [1:0]	Function
00	PA12
01	GT1_CH0
10	Reserved
11	Reserved

[23:22] PACFG11 Port A pin 11 AFIO Configuration

PACFG11 [1:0]	Function
00	PA11
01	SPI1_MISO
10	UR0_RX
11	Reserved

[21:20] PACFG10 Port A pin 10 AFIO Configuration

PACFG10 [1:0]	Function
00	PA10
01	SPI1_MOSI
10	UR0_TX
11	Reserved

[19:18] PACFG9 Port A pin 9 AFIO Configuration

PACFG9 [1:0]	Function
00	PA9
01	SPI1_SCK
10	UR0_CTS/SCK
11	Reserved

[17:16] PACFG8 Port A pin 8 AFIO Configuration

PACFG8 [1:0]	Function
00	PA8
01	SPI1_SEL
10	UR0_RTS/TXE
11	Reserved

[15:14] PACFG7 Port A pin 7 AFIO Configuration

PACFG7 [1:0]	Function
00	PA7
01	ADC_IN7
10	UR1_RX
11	SPI1_MISO

Bits	Field	Descriptions
[13:12]	PACFG6	Port A pin 6 AFIO Configuration

PACFG6 [1:0]	Function
00	PA6
01	ADC_IN6
10	UR1_TX
11	SPI1_MOSI

[11:10] PACFG5 Port A pin 5 AFIO Configuration

PACFG5 [1:0]	Function
00	PA5
01	ADC_IN5
10	UR1_CTS/SCK
11	SPI1_SCK

[9:8] PACFG4 Port A pin 4 AFIO Configuration

PACFG4 [1:0]	Function
00	PA4
01	ADC_IN4
10	UR1_RTS/TXE
11	SPI1_SEL

[7:6] PACFG3 Port A pin 3 AFIO Configuration

PACFG3 [1:0]	Function
00	PA3
01	ADC_IN3
10	UR0_RX
11	GT1_CH3

[5:4] PACFG2 Port A pin 2 AFIO Configuration

PACFG2 [1:0]	Function
00	PA2
01	ADC_IN2
10	UR0_TX
11	GT1_CH2

Bits	Field	Descriptions
[3:2]	PACFG1	Port A pin 1 AFIO Configuration

PACFG1 [1:0]	Function
00	PA1
01	ADC_IN1
10	SCI_DIO
11	GT1_CH1

[1:0] PACFG0 Port A pin 0 AFIO Configuration

PACFG0 [1:0]	Function
00	PA0
01	ADC_IN0
10	SCI_CLK
11	GT1_CH0

GPIO B Configuration Register – GPBCFGR

This register specifies the GPIO Port B pin alternative function.

Offset: 0x00C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	PBCFG15		PBCFG14		PBCFG13		PBCFG12	
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	23	22	21	20	19	18	17	16
	PBCFG11		PBCFG10		PBCFG9		PBCFG8	
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
	PBCFG7		PBCFG6		PBCFG5		PBCFG4	
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	PBCFG3		PBCFG2		PBCFG1		PBCFG0	
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[31:30]	PBCFG15	Port B pin 15 AFIO Configuration

PBCFG15 [1:0]	Function
00	PB15
01	UR1_RTS/TXE
10	Reserved
11	Reserved

[29:28] PBCFG14 Port B pin 14 AFIO Configuration

PBCFG14 [1:0]	Function
00	PB14
01	UR1_CTS/SCK
10	GT1_ETI
11	Reserved

[27:26] PBCFG13 Port B pin 13 AFIO Configuration

PBCFG13 [1:0]	Function
00	PB13
01	UR0_RX
10	Reserved
11	Reserved

Bits	Field	Descriptions

[25:24] PBCFG12 Port B pin 12 AFIO Configuration

PBCFG12 [1:0]	Function
00	XTALOUT
01	PB12
10	Reserved
11	Reserved

[23:22] PBCFG11 Port B pin 11 AFIO Configuration

PBCFG11 [1:0]	Function
00	XTALIN
01	PB11
10	Reserved
11	Reserved

[21:20] PBCFG10 Port B pin 10 AFIO Configuration

PBCFG10 [1:0]	Function
00	PB10
01	UR0_TX
10	Reserved
11	Reserved

[19:18] PBCFG9 Port B pin 9 AFIO Configuration

PBCFG9 [1:0]	Function
00	PB9
01	UR0_CTS/SCK
10	Reserved
11	Reserved

[17:16] PBCFG8 Port B pin 8 AFIO Configuration

PBCFG8 [1:0]	Function
00	PB8
01	UR0_RTS/TXE
10	Reserved
11	Reserved

[15:14] PBCFG7 Port B pin 7 AFIO Configuration

PBCFG7 [1:0]	Function
00	PB7
01	GT0_ETI
10	I^2C1_SDA
11	UR0_DTR

Bits	Field	Descriptions
[13:12]	PBCFG6	Port B pin 6 AFIO Configuration

PBCFG6 [1:0]	Function
00	RTCOUT
01	PB6_WAKEUP
10	Reserved
11	Reserved

[11:10] PBCFG5 Port B pin 5 AFIO Configuration

PBCFG5 [1:0]	Function
00	XTAL32KOUT
01	PB5
10	Reserved
11	Reserved

[9:8] PBCFG4 Port B pin 4 AFIO Configuration

PBCFG4 [1:0]	Function
00	XTAL32KIN
01	PB4
10	Reserved
11	Reserved

[7:6] PBCFG3 Port B pin 3 AFIO Configuration

PBCFG3 [1:0]	Function
00	PB3
01	GT0_CH3
10	UR1_RX
11	SPI0_MISO

[5:4] PBCFG2 Port B pin 2 AFIO Configuration

PBCFG2 [1:0]	Function
00	PB2
01	GT0_CH2
10	UR1_TX
11	SPI0_MOSI

Bits	Field	Descriptions
[3:2]	PBCFG1	Port B pin 1 AFIO Configuration

PBCFG1 [1:0]	Function
00	PB1
01	GT0_CH1
10	UR1_CTS/SCK
11	SPI0_SCK

[1:0] PBCFG0 Port B pin 0 AFIO Configuration

PACFG0 [1:0]	Function
00	PB0
01	GT0_CH0
10	UR1_RTS/TXE
11	SPI0_SEL

GPIO C Configuration Register – GPCCFGR

This register specifies the GPIO Port C pin alternative function.

Offset: 0x010

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	PCCFG15		PCCFG14		PCCFG13		PCCFG12	
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	23	22	21	20	19	18	17	16
	PCCFG11		PCCFG10		PCCFG9		PCCFG8	
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
	PCCFG7		PCCFG6		PCCFG5		PCCFG4	
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	PCCFG3		PCCFG2		PCCFG1		PCCFG0	
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[31:30]	PCCFG15	Port C pin 15 AFIO Configuration

PCCFG15 [1:0]	Function
00	PC15
01	SCI_DET
10	GT0_ETI
11	UR0_DSR

[29:28] PCCFG14 Port C pin 14 AFIO Configuration

PCCFG14 [1:0]	Function
00	PC14
01	SCI_DIO
10	MT_CH0N
11	UR1_CTS/SCK

[27:26] PCCFG13 Port C pin 13 AFIO Configuration

PCCFG13 [1:0]	Function
00	PC13
01	SCI_CLK
10	MT_CH0
11	UR1_RTS/TXE

Bits	Field	Descriptions

[25:24] PCCFG12 Port C pin 12 AFIO Configuration

PCCFG12 [1:0]	Function	
	HT32F1755/HT32F1765	HT32F2755
00	PC12	
01	I²C0_SDA	
10	MT_CH1N	
11	UR0_CTS/SCK	CSIF_MCK

[23:22] PCCFG11 Port C pin 11 AFIO Configuration

PCCFG11 [1:0]	Function	
	HT32F1755/HT32F1765	HT32F2755
00	PC11	
01	I²C0_SCL	
10	MT_CH1	
11	UR0_RTS/TXE	CSIF_PCK

[21:20] PCCFG10 Port C pin 10 AFIO Configuration

PCCFG10 [1:0]	Function
00	PC10
01	SCI_DET
10	MT_ETI
11	UR0_RX

[19:18] PCCFG9 Port C pin 9 AFIO Configuration

PCCFG9 [1:0]	Function
00	PC9_BOOT1
01	Reserved
10	Reserved
11	Reserved

[17:16] PCCFG8 Port C pin 8 AFIO Configuration

PCCFG8 [1:0]	Function
00	PC8_BOOT0
01	CKOUT
10	Reserved
11	UR0_TX

Bits	Field	Descriptions
[15:14]	PCCFG7	Port C pin 7 AFIO Configuration

PCCFG7 [1:0]	Function
00	PC7
01	I²C1_SDA
10	SCI_DIO
11	Reserved

[13:12] PCCFG6 Port C pin 6 AFIO Configuration

PCCFG6 [1:0]	Function
00	PC6
01	I²C1_SCL
10	SCI_CLK
11	Reserved

[11:10] PCCFG5 Port C pin 5 AFIO Configuration

PCCFG5 [1:0]	Function
00	PC5
01	UR1_RX
10	I²C0_SDA
11	Reserved

[9:8] PCCFG4 Port C pin 4 AFIO Configuration

PCCFG4 [1:0]	Function
00	PC4
01	UR1_TX
10	I²C0_SCL
11	Reserved

[7:6] PCCFG3 Port C pin 3 AFIO Configuration

PCCFG3 [1:0]	Function
00	PC3
01	SPI1_MISO
10	GT1_CH3
11	UR0_DCD

[5:4] PCCFG2 Port C pin 2 AFIO Configuration

PCCFG2 [1:0]	Function
00	PC2
01	SPI1_MOSI
10	GT1_CH2
11	UR0_RI

Bits	Field	Descriptions
[3:2]	PCCFG1	Port C pin 1 AFIO Configuration

PCCFG1 [1:0]	Function
00	PC1
01	SPI1_SCK
10	GT1_CH1
11	I²C1_SDA

[1:0] PCCFG0 Port C pin 0 AFIO Configuration

PCCFG0 [1:0]	Function
00	PC0
01	SPI1_SEL
10	GT1_CH0
11	I²C1_SCL

GPIO D Configuration Register – GPDCFGR

This register specifies the GPIO Port D pin alternative function.

Offset: 0x014

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	PDCFG15		PDCFG14		PDCFG13		PDCFG12	
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	23	22	21	20	19	18	17	16
	PDCFG11		PDCFG10		PDCFG9		PDCFG8	
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
	PDCFG7		PDCFG6		PDCFG5		PDCFG4	
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	PDCFG3		PDCFG2		PDCFG1		PDCFG0	
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[31:30]	PDCFG15	Port D pin 15 AFIO Configuration

PDCFG15 [1:0]	Function
00	PD15
01	MT_CH1N
10	SCI_DIO
11	Reserved

[29:28] PDCFG14 Port D pin 14 AFIO Configuration

PDCFG14 [1:0]	Function
00	PD14
01	MT_CH1
10	SCI_CLK
11	Reserved

[27:26] PDCFG13 Port D pin 13 AFIO Configuration

PDCFG13 [1:0]	Function
00	PD13
01	MT_CH0N
10	I²C0_SDA
11	GT0_ETI

Bits	Field	Descriptions

[25:24] PDCFG12 Port D pin 12 AFIO Configuration

PDCFG12 [1:0]	Function
00	PD12
01	MT_CH0
10	I²C0_SCL
11	GT1_ETI

[23:22] PDCFG11 Port D pin 11 AFIO Configuration

PDCFG11 [1:0]	Function	
	HT32F1755/HT32F1765	HT32F2755
00	PD11	
01	SPI0_MISO	
10	MT_BRK	
11	GT1_CH3	CSIF_D3

[21:20] PDCFG10 Port D pin 10 AFIO Configuration

PDCFG10 [1:0]	Function	
	HT32F1755/HT32F1765	HT32F2755
00	PD10	
01	SPI0_MOSI	
10	MT_CH3	
11	GT1_CH2	CSIF_D2

[19:18] PDCFG9 Port D pin 9 AFIO Configuration

PDCFG9 [1:0]	Function	
	HT32F1755/HT32F1765	HT32F2755
00	PD9	
01	SPI0_SCK	
10	MT_CH2N	
11	GT1_CH1	CSIF_D1

[17:16] PDCFG8 Port D pin 8 AFIO Configuration

PDCFG8 [1:0]	Function	
	HT32F1755/HT32F1765	HT32F2755
00	PD8	
01	SPI0_SEL	
10	MT_CH2	
11	GT1_CH0	CSIF_D0

Bits	Field	Descriptions
[15:14]	PDCFG7	Port D pin 7 AFIO Configuration

PDCFG7 [1:0]	Function
00	PD7
01	SPI1_MISO
10	Reserved
11	Reserved

[13:12] PDCFG6 Port D pin 6 AFIO Configuration

PDCFG6 [1:0]	Function
00	PD6
01	SPI1_MOSI
10	Reserved
11	Reserved

[11:10] PDCFG5 Port D pin 5 AFIO Configuration

PDCFG5 [1:0]	Function
00	PD5
01	SPI1_SCK
10	Reserved
11	Reserved

[9:8] PDCFG4 Port D pin 4 AFIO Configuration

PDCFG4 [1:0]	Function
00	PD4
01	SPI1_SEL
10	Reserved
11	Reserved

[7:6] PDCFG3 Port D pin 3 AFIO Configuration

PDCFG3 [1:0]	Function
00	PD3
01	GT0_CH3
10	SPI0_MISO
11	Reserved

[5:4] PDCFG2 Port D pin 2 AFIO Configuration

PDCFG2 [1:0]	Function
00	PD2
01	GT0_CH2
10	SPI0_MOSI
11	UR0_DCD

Bits	Field	Descriptions
[3:2]	PDCFG1	Port D pin 1 AFIO Configuration

PDCFG1 [1:0]	Function
00	PD1
01	GT0_CH1
10	SPI0_SCK
11	UR0_RI

[1:0] PDCFG0 Port D pin 0 AFIO Configuration

PDCFG0 [1:0]	Function
00	PD0
01	GT0_CH0
10	SPI0_SEL
11	UR0_DTR

GPIO E Configuration Register – GPECFGR

This register specifies the GPIO Port E pin alternative function.

Offset: 0x018

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	PECFG15		PECFG14		PECFG13		PECFG12	
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	23	22	21	20	19	18	17	16
	PECFG11		PECFG10		PECFG9		PECFG8	
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
	PECFG7		PECFG6		PECFG5		PECFG4	
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	PECFG3		PECFG2		PECFG1		PECFG0	
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[31:30]	PECFG15	Port E pin 15 AFIO Configuration

PECFG15 [1:0]	Function	
	HT32F1755/HT32F1765	HT32F2755
00	JTRST	
01	PE15	
10	MT_CH0N	
11	UR1_RX	CSIF_VSYNC

[29:28] PECFG14 Port E pin 14 AFIO Configuration

PECFG14 [1:0]	Function	
	HT32F1755/HT32F1765	HT32F2755
00	JTDI	
01	PE14	
10	MT_CH0	
11	UR1_TX	CSIF_HSYNC

[27:26] PECFG13 Port E pin 13 AFIO Configuration

PECFG13 [1:0]	Function
00	JTMS_SWDIO
01	PE13
10	Reserved
11	Reserved

Bits	Field	Descriptions

[25:24] PECFG12 Port E pin 12 AFIO Configuration

PECFG12 [1:0]	Function
00	JTCK_SWCLK
01	PE12
10	Reserved
11	Reserved

[23:22] PECFG11 Port E pin 11 AFIO Configuration

PECFG11 [1:0]	Function
00	JTDO_TRACESWO
01	PE11
10	Reserved
11	Reserved

[21:20] PECFG10 Port E pin 10 AFIO Configuration

PECFG10 [1:0]	Function
00	PE10
01	AOUT1
10	GT1_ETI
11	I²C1_SDA

[19:18] PECFG9 Port E pin 9 AFIO Configuration

PECFG9 [1:0]	Function
00	PE9
01	CP1
10	GT0_ETI
11	I²C1_SCL

[17:16] PECFG8 Port E pin 8 AFIO Configuration

PECFG8 [1:0]	Function	
	HT32F1755/HT32F1765	HT32F2755
00	PE8	
01	CN1	
10	GT0_CH3	
11	SPI1_MISO	CSIF_D7

[15:14] PECFG7 Port E pin 7 AFIO Configuration

PECFG7 [1:0]	Function	
	HT32F1755/HT32F1765	HT32F2755
00	PE7	
01	AOUT0	
10	GT0_CH2	
11	SPI1_MOSI	CSIF_D6

Bits	Field	Descriptions
[13:12]	PECFG6	Port E pin 6 AFIO Configuration

PECFG6 [1:0]	Function	
	HT32F1755/HT32F1765	HT32F2755
00	PE6	
01	CP0	
10	GT0_CH1	
11	SPI1_SCK	CSIF_D5

[11:10] PECFG5 Port E pin 5 AFIO Configuration

PECFG5 [1:0]	Function	
	HT32F1755/HT32F1765	HT32F2755
00	PE5	
01	CN0	
10	GT0_CH0	
11	SPI1_SEL	CSIF_D4

[9:8] PECFG4 Port E pin 4 AFIO Configuration

PECFG4 [1:0]	Function
00	PE4
01	MT_ETI
10	Reserved
11	Reserved

[7:6] PECFG3 Port E pin 3 AFIO Configuration

PECFG3 [1:0]	Function
00	PE3
01	MT_BRK
10	Reserved
11	Reserved

[5:4] PECFG2 Port E pin 2 AFIO Configuration

PECFG2 [1:0]	Function
00	PE2
01	MT_CH3
10	Reserved
11	Reserved

Bits	Field	Descriptions
[3:2]	PECFG1	Port E pin 1 AFIO Configuration

PECFG1 [1:0]	Function
00	PE1
01	MT_CH2N
10	Reserved
11	Reserved

[1:0] PECFG0 Port E pin 0 AFIO Configuration

PECFG0 [1:0]	Function
00	PE0
01	MT_CH2
10	Reserved
11	Reserved

10 Nested Vectored Interrupt Controller (NVIC)

Introduction

In order to reduce the latency and increase the interrupt processing efficiency, a tightly coupled integrated section, which is named as Nested Vectored Interrupt Controller (NVIC), is provided by the Cortex™-M3. The NVIC controls the system exceptions and the peripheral interrupts which include functions such as the enable/disable control, priority, clear-pending, active status report, software trigger and vector table remapping. Refer to the Technical Reference Manual of Cortex™-M3 for more details.

Additionally, an integrated simple, 24-bit down count timer (SysTick) is provided by the Cortex™-M3 to be used as a tick timer for the Real Timer Operation System (RTOS) or as a simple counter. The SysTick counts down from the preloaded value and generates a system interrupt when it reached zero.

The accompanying table lists the 16 system exception types and a variety of peripheral interrupts.

Table 23. Exception Types

Exception type	Priority	Interrupt Number	Exception Number	Vector Address	Description
—	—	—	0	0x000	Initial Stack Point value
Reset	-3 (Highest)	—	1	0x004	Reset
NMI	-2	—	2	0x008	Non-Maskable Interrupt. The clock stuck interrupt signal (clock monitor function provided by Clock Control Unit) is connected to the NMI input
Hard Fault	-1	—	3	0x00C	All fault classes
Memory Management	Configurable(1)	—	4	0x010	Memory Protection Unit (MPU) mismatch, including access violation and no match
Bus Fault	Configurable(1)	—	5	0x014	Pre-fetch fault, memory access fault and other address/memory related
Usage Fault	Configurable(1)	—	6	0x018	Usage fault, such as undefined executed instruction or illegal attempt of state transition
—	—	—	7	0x01C	Reserved
—	—	—	8	0x020	Reserved
—	—	—	9	0x024	Reserved
—	—	—	10	0x028	Reserved
SVCCall	Configurable(1)	—	11	0x02C	SVC instruction System service call
Debug Monitor	Configurable(1)	—	12	0x030	Debug monitor, when not halted
—	Configurable(1)	—	13	0x034	Reserved
PendSV	Configurable(1)	—	14	0x038	System Service Pendable request
SySTick	Configurable(1)	—	15	0x03C	SysTick timer decremented to zero
CKRDY	Configurable(2)	0	16	0x040	Clock ready interrupt (HSE, HSI, LSE, LSI, or PLL)
LVD	Configurable(2)	1	17	0x044	Low voltage detection interrupt

Exception type	Priority	Interrupt Number	Exception Number	Vector Address	Description
BOD	Configurable(2)	2	18	0x048	Brown-out detection interrupt
WDT	Configurable(2)	3	19	0x04C	Watchdog timer global interrupt
RTC	Configurable(2)	4	20	0x050	RTC global interrupt
FMC	Configurable(2)	5	21	0x054	FMC global interrupt
EVWUP	Configurable(2)	6	22	0x058	EXTI event wake up interrupt
LPWUP	Configurable(2)	7	23	0x05C	WAKEUP pin interrupt
EXTI0	Configurable(2)	8	24	0x060	EXTI Line 0 interrupt
EXTI1	Configurable(2)	9	25	0x064	EXTI Line 1 interrupt
EXTI2	Configurable(2)	10	26	0x068	EXTI Line 2 interrupt
EXTI3	Configurable(2)	11	27	0x06C	EXTI Line 3 interrupt
EXTI4	Configurable(2)	12	28	0x070	EXTI Line 4 interrupt
EXTI5	Configurable(2)	13	29	0x074	EXTI Line 5 interrupt
EXTI6	Configurable(2)	14	30	0x078	EXTI Line 6 interrupt
EXTI7	Configurable(2)	15	31	0x07C	EXTI Line 7 interrupt
EXTI8	Configurable(2)	16	32	0x080	EXTI Line 8 interrupt
EXTI9	Configurable(2)	17	33	0x084	EXTI Line 9 interrupt
EXTI10	Configurable(2)	18	34	0x088	EXTI Line 10 interrupt
EXTI11	Configurable(2)	19	35	0x08C	EXTI Line 11 interrupt
EXTI12	Configurable(2)	20	36	0x090	EXTI Line 12 interrupt
EXTI13	Configurable(2)	21	37	0x094	EXTI Line 13 interrupt
EXTI14	Configurable(2)	22	38	0x098	EXTI Line 14 interrupt
EXTI15	Configurable(2)	23	39	0x09C	EXTI Line 15 interrupt
COMP	Configurable(2)	24	40	0x0A0	Comparator global interrupt
ADC	Configurable(2)	25	41	0x0A4	ADC global interrupt
—	—	26	42	0x0A8	Reserved
MCTM_BRK	Configurable(2)	27	43	0x0AC	MCTM break interrupt
MCTM_UP	Configurable(2)	28	44	0x0B0	MCTM update interrupt
MCTM_TR_UP2	Configurable(2)	29	45	0x0B4	MCTM trigger/update event 2 interrupt
MCTM_CC	Configurable(2)	30	46	0x0B8	MCTM capture/compare interrupt
—	—	31	47	0x0BC	Reserved
—	—	32	48	0x0C0	Reserved
—	—	33	49	0x0C4	Reserved
—	—	34	50	0x0C8	Reserved
GPTM0	Configurable(2)	35	51	0x0CC	GPTM0 global interrupt
GPTM1	Configurable(2)	36	52	0x0D0	GPTM1 global interrupt
—	—	37	53	0x0D4	Reserved
—	—	38	54	0x0D8	Reserved
—	—	39	55	0x0DC	Reserved
—	—	40	56	0x0E0	Reserved
BFTM0	Configurable(2)	41	57	0x0E4	BFTM0 global interrupt

Exception type	Priority	Interrupt Number	Exception Number	Vector Address	Description
BFTM1	Configurable(2)	42	58	0x0E8	BFTM1 global interrupt
I²C0	Configurable(2)	43	59	0x0EC	I²C0 global interrupt
I²C1	Configurable(2)	44	60	0x0F0	I²C1 global interrupt
SPI0	Configurable(2)	45	61	0x0F4	SPI0 global interrupt
SPI1	Configurable(2)	46	62	0x0F8	SPI1 global interrupt
USART0	Configurable(2)	47	63	0x0FC	USART0 global interrupt
USART1	Configurable(2)	48	64	0x100	USART1 global interrupt
—	—	49	65	0x104	Reserved
—	—	50	66	0x108	Reserved
SCI	Configurable(2)	51	67	0x10C	SCI global interrupt
—	—	52	68	0x110	Reserved
USB	Configurable(2)	53	69	0x114	USB global interrupt
—	—	54	70	0x118	Reserved
PDMA_CH0	Configurable(2)	55	71	0x11C	PDMA channel 0 global interrupt
PDMA_CH1	Configurable(2)	56	72	0x120	PDMA channel 1 global interrupt
PDMA_CH2	Configurable(2)	57	73	0x124	PDMA channel 2 global interrupt
PDMA_CH3	Configurable(2)	58	74	0x128	PDMA channel 3 global interrupt
PDMA_CH4	Configurable(2)	59	75	0x12C	PDMA channel 4 global interrupt
PDMA_CH5	Configurable(2)	60	76	0x130	PDMA channel 5 global interrupt
PDMA_CH6	Configurable(2)	61	77	0x134	PDMA channel 6 global interrupt
PDMA_CH7	Configurable(2)	62	78	0x138	PDMA channel 7 global interrupt
PDMA_CH8	Configurable(2)	63	79	0x13C	PDMA channel 8 global interrupt
PDMA_CH9	Configurable(2)	64	80	0x140	PDMA channel 9 global interrupt
PDMA_CH10	Configurable(2)	65	81	0x144	PDMA channel 10 global interrupt
PDMA_CH11	Configurable(2)	66	82	0x148	PDMA channel 11 global interrupt
CSIF	Configurable(2)	67	83	0x14C	CSIF global interrupt

Note 1: The exception priority can be changed using the NVIC System Handler Priority Registers. For more information, refer to the ARM “Technical Reference Manual of Cortex™-M3” document.

2: The interrupt priority can be changed using the NVIC Interrupt Priority Registers. For more information, refer to the ARM “Technical Reference Manual of Cortex™-M3” document.

Features

- 16 system Cortex™-M3 exceptions
- Up to 55 maskable peripheral interrupts
- 16 programmable priority levels – 4 bit interrupt priority setup
- Non-Maskable interrupt
- Low-latency exception and interrupt handling
- Vector table remapping capability
  - Integrated simple, 24-bit system timer, SysTick
  - 24-bit down counter
  - Auto-reloading capability
  - Maskable system interrupt generation when counter decrements to 0
  - SysTick clock source derived from the HCLK or AHB clock divided by 8

Functional Descriptions

SysTick Calibration

The SysTick Calibration Value Register (SCALIB) is provided by the NVIC to give a reference time base of 1ms for the RTOS tick timer or other purpose. The TENMS field in the SCALIB register has a fixed value of 9000 which is the counter reload value to indicate 1 ms when the clock source comes from the SysTick reference input clock STCLK with a frequency of 9MHz (72MHz divide by 8).

Register Map

The following table shows the NVIC registers and reset values.

Table 24. NVIC Register Map

Register	Offset	Description	Reset Value
NVIC Base Address=0xE000_E000			
ICTR	0x004	Interrupt Control Type Register	0x0000_0001
SCTRL	0x010	SysTick Control and Status Register	0x0000_0000
SLOAD	0x014	SysTick Reload Value Register	Unpredictable
SVAL	0x018	SysTick Current Value Register	Unpredictable
SCALIB	0x01C	SysTick Calibration Value Register	0x4000_2328
ISER0_31	0x100	Irq 0 to 31 Set Enable Register	0x0000_0000
ISER32_63	0x104	Irq 32 to 63 Set Enable Register	0x0000_0000
ISER64_95	0x108	Irq 64 to 95 Set Enable Register	0x0000_0000
ICER0_31	0x180	Irq 0 to 31 Clear Enable Register	0x0000_0000
ICER32_63	0x184	Irq 32 to 63 Clear Enable Register	0x0000_0000
ICER64_95	0x188	Irq 64 to 95 Clear Enable Register	0x0000_0000
ISPR0_31	0x200	Irq 0 to 31 Set Pending Register	0x0000_0000
ISPR32_63	0x204	Irq 32 to 63 Set Pending Register	0x0000_0000
ISPR64_95	0x208	Irq 64 to 95 Set Pending Register	0x0000_0000
ICPR0_31	0x280	Irq 0 to 31 Clear Pending Register	0x0000_0000
ICPR32_63	0x284	Irq 32 to 63 Clear Pending Register	0x0000_0000
ICPR64_95	0x288	Irq 64 to 95 Clear Pending Register	0x0000_0000

Register	Offset	Description	Reset Value
IABR0_31	0x300	Irq 0 to 31 Active Bit Register	0x0000_0000
IABR32_63	0x304	Irq 32 to 63 Active Bit Register	0x0000_0000
IABR64_95	0x308	Irq 64 to 95 Active Bit Register	0x0000_0000
IRQ0_3	0x400	Irq 0 to 3 Priority Register	0x0000_0000
IRQ4_7	0x404	Irq 4 to 7 Priority Register	0x0000_0000
IRQ8_11	0x408	Irq 8 to 11 Priority Register	0x0000_0000
IRQ12_15	0x40C	Irq 12 to 15 Priority Register	0x0000_0000
IRQ16_19	0x410	Irq 16 to 19 Priority Register	0x0000_0000
IRQ20_23	0x414	Irq 20 to 23 Priority Register	0x0000_0000
IRQ24_27	0x418	Irq 24 to 27 Priority Register	0x0000_0000
IRQ28_31	0x41C	Irq 28 to 31 Priority Register	0x0000_0000
IRQ32_35	0x420	Irq 32 to 35 Priority Register	0x0000_0000
IRQ36_39	0x424	Irq 36 to 39 Priority Register	0x0000_0000
IRQ40_43	0x428	Irq 40 to 43 Priority Register	0x0000_0000
IRQ44_47	0x42C	Irq 44 to 47 Priority Register	0x0000_0000
IRQ48_51	0x430	Irq 48 to 51 Priority Register	0x0000_0000
IRQ52_55	0x434	Irq 52 to 55 Priority Register	0x0000_0000
IRQ56_59	0x438	Irq 56 to 59 Priority Register	0x0000_0000
IRQ60_63	0x43C	Irq 60 to 63 Priority Register	0x0000_0000
IRQ64_67	0x440	Irq 64 to 67 Priority Register	0x0000_0000
ICSR	0xD04	Interrupt Control State Register	0x0000_0000
VTOR	0xD08	Vector Table Offset Register	0x0000_0000
AIRCR	0xD0C	Application Interrupt/Reset Control Register	0xFA05_0000
SCR	0xD10	System Control Register	0x0000_0000
CCR	0xD14	Configuration Control Register	0x0000_0000
SHPR4-7	0xD18	System Handlers 4-7 Priority Register	0x0000_0000
SHPR8_11	0xD1C	System Handlers 8-11 Priority Register	0x0000_0000
SHPR12_15	0xD20	System Handlers 12-15 Priority Register	0x0000_0000
SHCSR	0xD24	System Handler Control and State Register	0x0000_0000
CFSR	0xD28	Configurable Fault Status Registers	0x0000_0000
HFSR	0xD2C	Hard Fault Status Register	0x0000_0000
DFSR	0xD30	Debug Fault Status Register	0x0000_0000
MMFAR	0xD34	Mem Manage Address Register	Unpredictable
BFAR	0xD38	Bus Fault Address Register	Unpredictable
AFSR	0xD3C	Auxiliary Fault Status Register	0x0000_0000
STIR	0xF00	Software Trigger Interrupt Register	0x0000_0000

Note: For more information of the above detail register descriptions, please refer to the “Technical Reference Manual of Cortex™-M3” document from ARM.

11 External Interrupt/Event Controller (EXTI)

Introduction

The External Interrupt/Event Controller, EXTI, comprises 16 edge detectors which can generate a wake-up event or interrupt requests independently. In interrupt mode there are five trigger types which can be selected as the external interrupt trigger type, low level, high level, negative edge, positive edge and both edges, selectable using the SRCnTYPE field in the EXTICFGRn register. In the wake-up event mode, the wake-up event polarity can be configured by setting the EXTInPOL field in the EXTIWAKUPPOLR register. If the EVWUPIEN bit in the EXTIWAKUPCR Register is set, the EVWUP interrupt can be generated when the associated wake-up event occurs and the corresponding EXTI wake-up enable bit is set. Each EXTI line can also be masked independently.

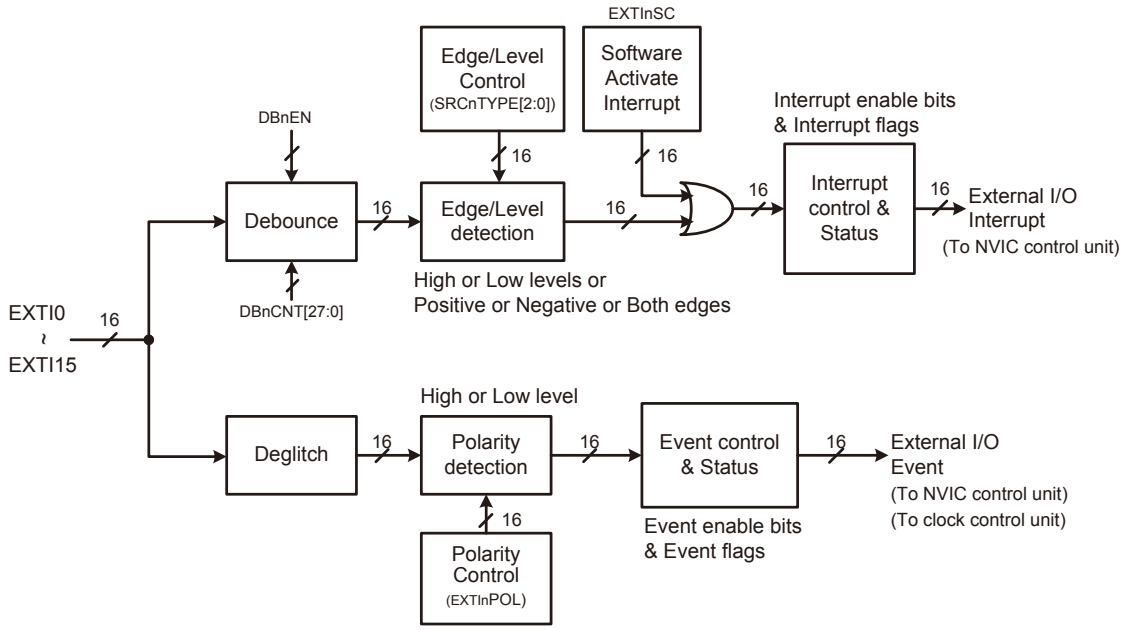


Figure 22. EXTI Block Diagram

Features

- Up to 16 EXTI lines with configurable trigger sources and types
  - All GPIO pins can be selected as an EXTI trigger source
  - Source trigger type includes high level, low level, negative edge, positive edge, or both edge
- Individual interrupt enable, wake-up enable and status bits for each EXTI line
- Software interrupt trigger mode for each EXTI line
- Integrated deglitch filter for short pulse blocking

Functional Descriptions

Wake-up Event Management

In order to wake-up the system from the power saving mode, the EXTI controller provides a function which can monitor external events and send them to the Cortex™-M3 core and the Clock Control Unit, CKCU. These external events include EXTI events, Low Voltage Detection, WAKEUP input pin and RTC wake-up functions. By configuring the wake-up event enable bit in the corresponding peripheral, the wake-up signal will be sent to the Cortex™-M3 and the CKCU via the EXTI controller when the corresponding wake-up event occurs. Additionally, the software can enable the event wake-up interrupt function by setting the EVWUPIEN bit in the EXTIWAKUPCR register and the EXTI controller will then assert an interrupt when the wake-up event occurs.

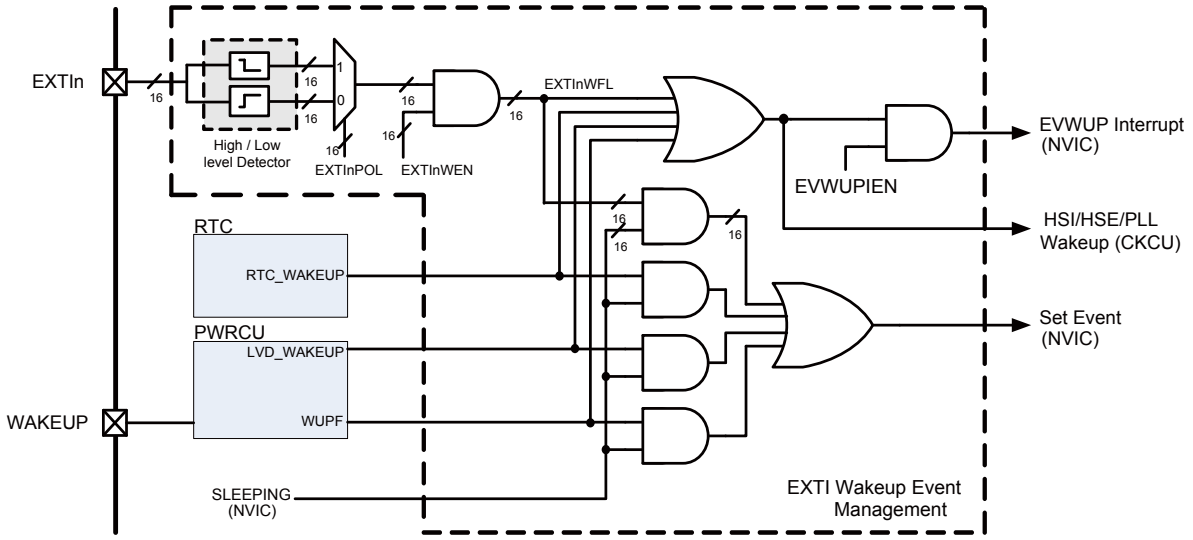


Figure 23. EXTI Wake-up Event Management

External Interrupt/Event Line Mapping

All GPIO pins can be selected as EXTI trigger sources by configuring the EXTInPIN [3:0] field in the AFIO ESSRn register to trigger an interrupt or event. Refer to the AFIO section for more details.

Interrupt and Debounce

The application software can set the DBnEN bit in the EXTIn Interrupt Configuration Register EXTICFGRn to enable the corresponding pin de-bounce function and configure the DBnCNT field in the EXTICFGRn so as to select an appropriate de-bounce time for specific applications. The interrupt signal will however be delayed due to the de-bounce function. When the device is woken up from the power saving mode by an external interrupt, an interrupt request will be generated by the EXTI wake-up flag. After the device has been woken up and the clock has recovered, the EXTI wake-up flag that was triggered by the EXTI line must be read and then cleared by application software. The accompanying diagram shows the relationship between the EXTI input signal and the EXTI interrupt/event request signal.

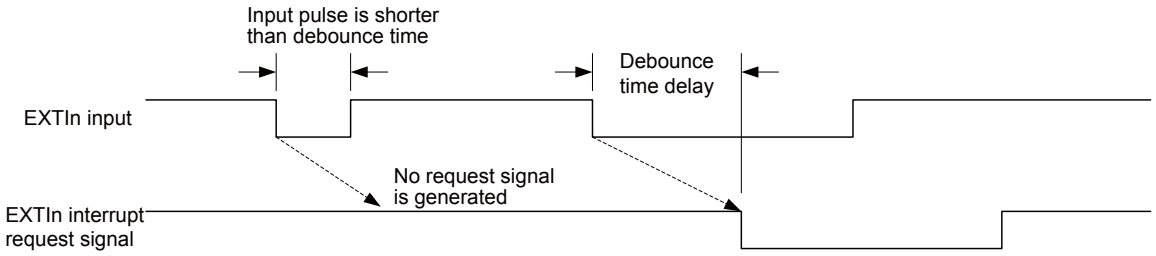


Figure 24. EXTI Debounce Function

Register Map

The following table shows the EXTI registers and reset values.

Table 25. EXTI Register Map

Register	Offset	Description	Reset Value
EXTI Base Address=0x4002_4000			
EXTICFGR0	0x000	EXTI Interrupt 0 Configuration Register	0x0000_0000
EXTICFGR1	0x004	EXTI Interrupt 1 Configuration Register	0x0000_0000
EXTICFGR2	0x008	EXTI Interrupt 2 Configuration Register	0x0000_0000
EXTICFGR3	0x00C	EXTI Interrupt 3 Configuration Register	0x0000_0000
EXTICFGR4	0x010	EXTI Interrupt 4 Configuration Register	0x0000_0000
EXTICFGR5	0x014	EXTI Interrupt 5 Configuration Register	0x0000_0000
EXTICFGR6	0x018	EXTI Interrupt 6 Configuration Register	0x0000_0000
EXTICFGR7	0x01C	EXTI Interrupt 7 Configuration Register	0x0000_0000
EXTICFGR8	0x020	EXTI Interrupt 8 Configuration Register	0x0000_0000
EXTICFGR9	0x024	EXTI Interrupt 9 Configuration Register	0x0000_0000
EXTICFGR10	0x028	EXTI Interrupt 10 Configuration Register	0x0000_0000
EXTICFGR11	0x02C	EXTI Interrupt 11 Configuration Register	0x0000_0000
EXTICFGR12	0x030	EXTI Interrupt 12 Configuration Register	0x0000_0000
EXTICFGR13	0x034	EXTI Interrupt 13 Configuration Register	0x0000_0000
EXTICFGR14	0x038	EXTI Interrupt 14 Configuration Register	0x0000_0000
EXTICFGR15	0x03C	EXTI Interrupt 15 Configuration Register	0x0000_0000
EXTICR	0x040	EXTI Interrupt Control Register	0x0000_0000
EXTIEDGEFLGR	0x044	EXTI Interrupt Edge Flag Register	0x0000_0000
EXTIEDGESR	0x048	EXTI Interrupt Edge Status Register	0x0000_0000
EXTISSCR	0x04C	EXTI Interrupt Software Set Command Register	0x0000_0000
EXTIWAKUPCR	0x050	EXTI Interrupt Wake-up Control Register	0x0000_0000
EXTIWAKUPPOLR	0x054	EXTI Interrupt Wake-up Polarity Register	0x0000_0000
EXTIWAKUPFLG	0x058	EXTI Interrupt Wake-up Flag Register	0x0000_0000

Register Descriptions

EXTI Interrupt Configuration Register n – EXTICFGRn, n=0~15

This register is used to specify the debounce function and select the trigger type.

Offset: 0x000 (EXTICFGR0)~0x03C (EXTICFGR15)

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	DBnEN	SRCnTYPE			DBnCNT			
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	23	22	21	20	19	18	17	16
	DBnCNT							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
	DBnCNT							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	DBnCNT							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[31]	DBnEN	EXTIn De-bounce Circuit Enable Bit (n=0~15) 0: De-bounce circuit disabled 1: De-bounce circuit enabled
[30:28]	SRCnTYPE	EXTIn Interrupt Source Trigger Type (n=0~15)

SRCnTYPE [2:0]			Interrupt Source Type
0	0	0	Low-level Sensitive
0	0	1	High-level Sensitive
0	1	0	Negative-edge Triggered
0	1	1	Positive-edge Triggered
1	X	X	Both-edge Triggered

[27:0]	DBnCNT	EXTIn De-bounce Counter (n=0~15) The de-bounce time is calculated with DBnCNT x APB clock period and should be long enough to take effect on the input signal.

EXTI Interrupt Control Register – EXTICR

This register is used to control the EXTI interrupt.

Offset: 0x040

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	EXTI15EN	EXTI14EN	EXTI13EN	EXTI12EN	EXTI11EN	EXTI10EN	EXTI9EN	EXTI8EN
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	EXTI7EN	EXTI6EN	EXTI5EN	EXTI4EN	EXTI3EN	EXTI2EN	EXTI1EN	EXTI0EN
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	EXTInEN	EXTIn Interrupt Enable Bit (n=0~15) 0: EXTI line n interrupt disabled 1: EXTI line n interrupt enabled

EXTI Interrupt Edge Flag Register – EXTIEDGEFLGR

This register is used to indicate if an EXTI edge has been detected.

Offset: 0x044

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	Reserved							
Type/Reset								
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	EXTI15EDF	EXTI14EDF	EXTI13EDF	EXTI12EDF	EXTI11EDF	EXTI10EDF	EXTI9EDF	EXTI8EDF
Type/Reset	WC 0	WC 0	WC 0	WC 0	WC 0	WC 0	WC 0	WC 0
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	EXTI7EDF	EXTI6EDF	EXTI5EDF	EXTI4EDF	EXTI3EDF	EXTI2EDF	EXTI1EDF	EXTI0EDF
Type/Reset	WC 0	WC 0	WC 0	WC 0	WC 0	WC 0	WC 0	WC 0

Bits	Field	Descriptions
[15:0]	EXTInEDF	EXTIn Edge Detection Flag (n=0~15) 0: No edge is detected 1: Positive or negative edge is detected This bit is set by the hardware circuitry when a positive or negative edge is detected on the corresponding EXTI line. Software should write 1 to clear it.

EXTI Interrupt Edge Status Register – EXTIEDGESR

This register indicates the polarity of a detected EXTI edge.

Offset: 0x048

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	Reserved							
Type/Reset								
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	EXTI15EDS	EXTI14EDS	EXTI13EDS	EXTI12EDS	EXTI11EDS	EXTI10EDS	EXTI9EDS	EXTI8EDS
Type/Reset	WC 0	WC 0	WC 0	WC 0	WC 0	WC 0	WC 0	WC 0
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	EXTI7EDS	EXTI6EDS	EXTI5EDS	EXTI4EDS	EXTI3EDS	EXTI2EDS	EXTI1EDS	EXTI0EDS
Type/Reset	WC 0	WC 0	WC 0	WC 0	WC 0	WC 0	WC 0	WC 0

Bits	Field	Descriptions
[15:0]	EXTInEDS	EXTIn Edge Detection Status (n=0~15) 0: Negative edge detected 1: Positive edge detected Software should write 1 to clear it.

EXTI Interrupt Software Set Command Register – EXTISSCR

This register is used to activate the EXTI interrupt.

Offset: 0x04C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	EXTI15SC	EXTI14SC	EXTI13SC	EXTI12SC	EXTI11SC	EXTI10SC	EXTI9SC	EXTI8SC
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	EXTI7SC	EXTI6SC	EXTI5SC	EXTI4SC	EXTI3SC	EXTI2SC	EXTI1SC	EXTI0SC
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	EXTInSC	EXTIn Software Set Command (n=0~15) 0: Deactivates the EXTIn interrupt 1: Activates the EXTIn interrupt

EXTI Interrupt Wake-up Control Register – EXTIWAKUPCR

This register is used to control the EXTI interrupt and wake-up function.

Offset: 0x050

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	EVWUPIEN	Reserved						
Type/Reset	RW 0							
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	EXTI15WEN	EXTI14WEN	EXTI13WEN	EXTI12WEN	EXTI11WEN	EXTI10WEN	EXTI9WEN	EXTI8WEN
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	EXTI7WEN	EXTI6WEN	EXTI5WEN	EXTI4WEN	EXTI3WEN	EXTI2WEN	EXTI1WEN	EXTI0WEN
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[31]	EVWUPIEN	EXTI Event Wake-up Interrupt Enable Bit 0: EVWUP interrupt disabled 1: EVWUP interrupt enabled
[15:0]	EXTInWEN	EXTIn Wake-up Enable Bit (n=0~15) 0: EXTIn wake-up disabled 1: EXTIn wake-up enabled

EXTI Interrupt Wake-up Polarity Register – EXTIWAKUPPOLR

This register is used to select the EXTI line interrupt wake-up polarity.

Offset: 0x054

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	EXTI15POL	EXTI14POL	EXTI13POL	EXTI12POL	EXTI11POL	EXTI10POL	EXTI9POL	EXTI8POL
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	EXTI7POL	EXTI6POL	EXTI5POL	EXTI4POL	EXTI3POL	EXTI2POL	EXTI1POL	EXTI0POL
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	EXTInPOL	EXTIn Wake-up Polarity (n=0~15) 0: EXTIn wake-up is high level active 1: EXTIn wake-up is low level active

EXTI Interrupt Wake-up Flag Register – EXTIWAKUPFLG

This register indicates if the system has been woken up by the EXTI line.

Offset: 0x058

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	Reserved							
Type/Reset								
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	EXTI15WFL	EXTI14WFL	EXTI13WFL	EXTI12WFL	EXTI11WFL	EXTI10WFL	EXTI9WFL	EXIT8WFL
Type/Reset	WC 0	WC 0	WC 0	WC 0	WC 0	WC 0	WC 0	WC 0
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	EXTI7WFL	EXTI6WFL	EXTI5WFL	EXTI4WFL	EXTI3WFL	EXTI2WFL	EXTI1WFL	EXTI0WFL
Type/Reset	WC 0	WC 0	WC 0	WC 0	WC 0	WC 0	WC 0	WC 0

Bits	Field	Descriptions
[15:0]	EXTInWFL	EXTIn Wake-up Flag (n=0~15) 0: No wake-up occurs 1: System is woken up by EXTIn Software should write 1 to clear it.

12 Analog to Digital Converter (ADC)

Introduction

A 12-bit multi-channel Analog to Digital Converter is integrated in the device. There are a total of 10 multiplexed channels including 8 external channels on which the external analog signal can be measured and 2 internal channels. If the input voltage is required to remain within a specific threshold window, the Analog Watchdog function will monitor and detect the signal. An interrupt will then be generated to inform that the input voltage is higher or lower than the set thresholds. There are three conversion modes to convert an analog signal to digital data. The A/D converter can be operated in one shot, continuous and discontinuous conversion mode. A right-aligned 16-bit data register is provided to store the data after conversion.

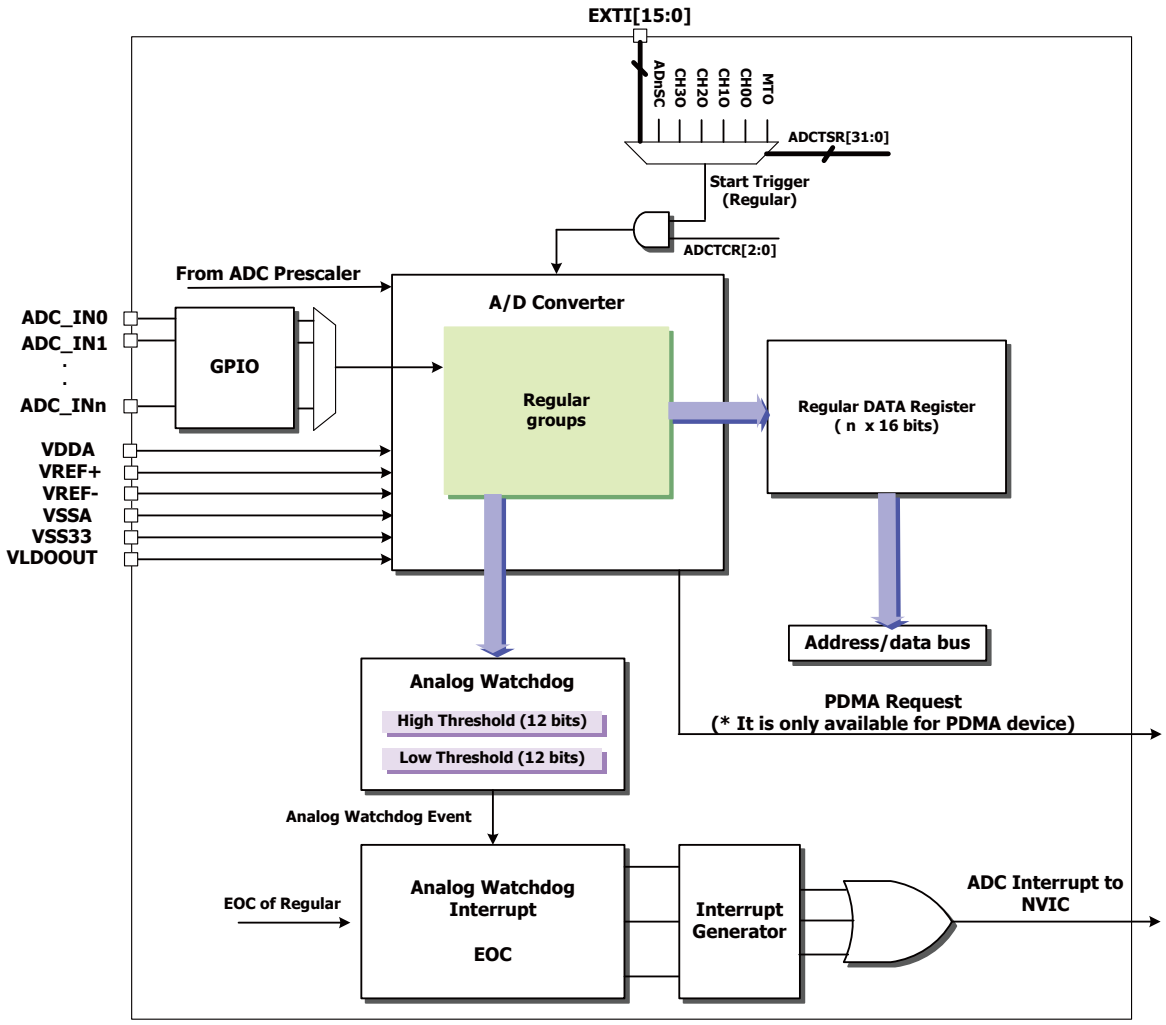


Figure 25. ADC Block Diagram

Features

- 12-bit SAR ADC engine
- Up to 1 MSPS conversion rate
  - 1μs at 56MHz, 1.17μs at 72MHz
- 8 external analog input channels
- 2 internal reference voltage detect analog input channels – V_{SSA} and V_{DDA}
- Individual programmable sampling time for each channel
- Three conversion modes
  - One shot conversion mode
  - Continuous conversion mode
  - Discontinuous conversion mode
- Up to 8 dedicated sequencer and data registers for conversion
  - Data format: unsigned right-aligned format
- Analog watchdog for predefined voltage range monitor
  - Lower/upper threshold register
  - Interrupt generation
- Various trigger start source for conversion modes
  - Software trigger
  - EXTI – external interrupt input pin
  - GPTM or MCTM trigger output – MTO and PWM CHnO
  - BFTM trigger
- Multiple generated interrupts
  - Single conversion end
  - Subgroup conversion end
  - Cycle conversion end
  - Analog Watchdog
  - Data register overwrite
- PDMA request on end of conversion occurrence

Functional Descriptions

ADC Clock Setup

The ADC clock, CK_ADC, is provided by the Clock Controller which is synchronous with the APB clock known as PCLK. Refer to the Clock Control Unit chapter for more details.

Channel Selection

The A/D converter supports 8 multiplexed channels and organizes the conversion results into the regular group. A regular group can organize a conversions sequence which can be implemented on the channel arranged in a specific conversion sequence length from 1 to 8. For example, conversion can be carried out with the following channel sequence: CH2, CH4, CH7, CH5, CH6, CH3, CH1 and CH0 one after another.

A regular group is composed of up to 8 conversions. The selected channels of the regular group conversion can be specified in the ADCLST0~ADCLST1 registers. The total conversion sequence length is setup using the ADSEQL [2:0] bits in the ADCCONV register.

Modifying the ADCCONV register during a conversion process will reset the current conversion, after which a new start pulse is required to restart a new conversion.

Conversion Mode

The A/D has three operating conversion modes. The conversion modes are One Shot Conversion Mode, Continuous Conversion Mode and Discontinuous Conversion mode. Details are provided later.

One Shot Conversion Mode

In one shot conversion mode, the A/D Converter will perform conversion cycles on the channels specified in the A/D conversion list registers ADCLSTn with a specific sequence when an A/D converter event occurs. When the A/D conversion mode field ADMODE [1:0] is set to 0x0, the A/D converter will operate in the One Shot Conversion Mode. This mode can be started by a software trigger, an external EXTI event or a TM event determined by the Trigger Control Register ADCTCR and the Trigger Source Register ADCTSR.

- The converted data will be stored in the 16-bit ADCDRn (n=0~7) registers.
- The ADC regular single sample end of conversion event raw status flag, ADIRAWS, in the ADCIRAW register will be set when the single sample conversion is finished.
- An interrupt will be generated after a single sample end of conversion if the ADIMS bit in the ADCIMR register is not masked.
- An interrupt will be generated after a regular group cycle end of conversion if the ADIMC bit in the ADCIMR register is not masked.

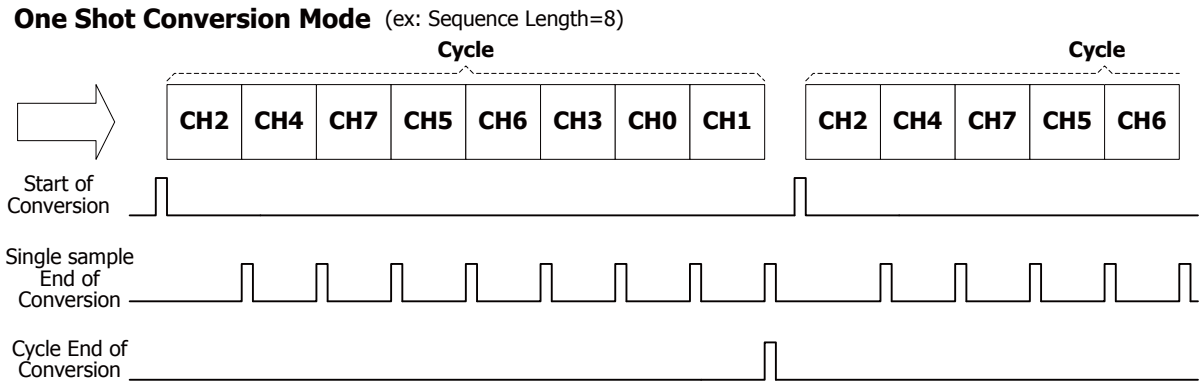


Figure 26. One Shot Conversion Mode

Continuous Conversion Mode

In Continuous Conversion Mode, repeat conversion cycle will start automatically without requiring additional A/D start trigger signals after a channel group conversion has completed. When the A/D conversion mode field ADMODE [1:0] is set to 0x2, the A/D converter will operate in the Continuous Conversion Mode which can be started by a software trigger, an external EXTI event or a TM event determined by the Trigger Control Register ADCTCR and the Trigger Source Register ADCTSR.

After each conversion:

- The converted data will be stored in the 16-bit ADCDRn (n=0~7) registers.
- The ADC regular group cycle end of conversion event raw status flag, ADIRAWC, in the ADCIRAW register will be set when the conversion cycle is finished.
- An interrupt will be generated after a single sample end of conversion if the ADIMS bit in the ADCIMR register is not masked.
- An interrupt will be generated after a regular group cycle end of conversion if the ADIMC bit in the ADCIMR register is not masked.

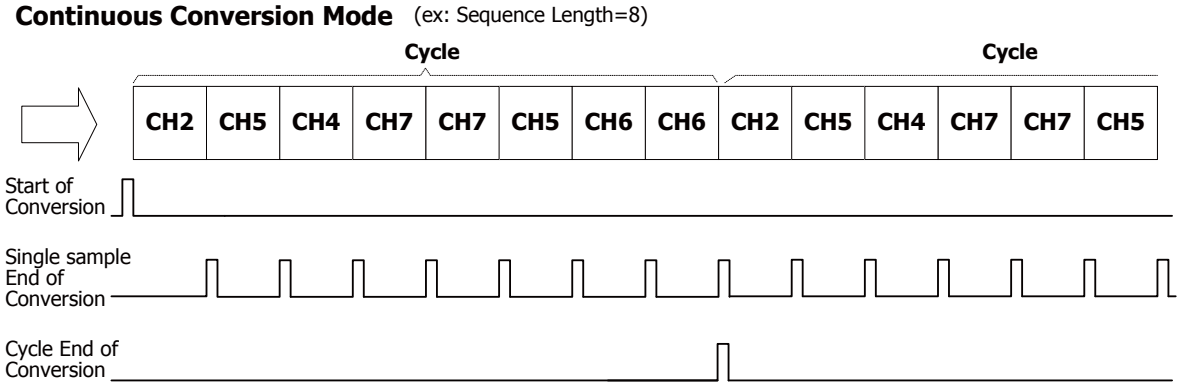


Figure 27. Continuous Conversion Mode

Discontinuous Conversion Mode

The A/D converter will operate in the Discontinuous Conversion Mode for regular groups when the A/D conversion mode bit field ADMODE [1:0] in the ADCCONV register is set to 0x3. The regular group to be converted can have up to 8 channels and can be arranged in a specific sequence by configuring the ADCLSTn registers where n ranges from 0 to 1. This mode is provided to convert data for the regular group with a short sequence, named as the A/D regular conversion subgroup, each time a trigger event occurs. The subgroup length is defined in the ADSUBL [2:0] field to specify the subgroup length. In the Discontinuous Conversion Mode the A/D converter can be started by a software trigger, an external EXTI event or a TM event for regular groups determined by the Trigger Control Register ADCTCR and the Trigger Source Register ADCTSR.

In the Discontinuous Conversion Mode, the A/D Converter will start to convert the next n conversions where the number n is the subgroup length defined by the ADSUBL field. When a trigger event occurs, the channels to be converted with a specific sequence are specified in the ADCLSTn registers. After n conversions have completed, the regular subgroup EOC interrupt raw flag ADIRAWG in the ADCIRAW register will be asserted. The A/D converter will now not continue to perform the next n conversions until the next trigger event occurs. The conversion cycle will end after all the regular group channels, of which the total number is defined by the ADSEQL [2:0] bits in the ADCCONV register, have finished their conversion, at which point the regular cycle EOC interrupt raw flag ADIRAWC in the ADCIRAW register will be asserted. If a new trigger event occurs after all the subgroup channels have all been converted, i.e., a complete conversion cycle has been finished, the conversion will restart from the first subgroup.

Example:

- A/D subgroup length=3 (ADSUBL=2) and sequence length=8 (ADSEQL=7), channels to be converted=2, 4, 7, 5, 6, 3, 0 and 1 – specific converting sequence as defined in the ADCLSTn registers.
  - Trigger 1: subgroup channels to be converted are CH2, CH4 and CH7 with the ADIRAWG flag being asserted after subgroup EOC.
  - Trigger 2: subgroup channels to be converted are CH5, CH6 and CH3 with the ADIRAWG flag being asserted after subgroup EOC.
  - Trigger 3: subgroup channels to be converted are CH0 and CH1 with the ADIRAWG flag being asserted after subgroup EOC. Also a Cycle end of conversion (EOC) interrupt raw flag ADIRAWC will be asserted.
  - Trigger 4: subgroup channels to be converted are CH2, CH4 and CH7 with the ADIRAWG flag being asserted – conversion sequence restarts from the beginning.

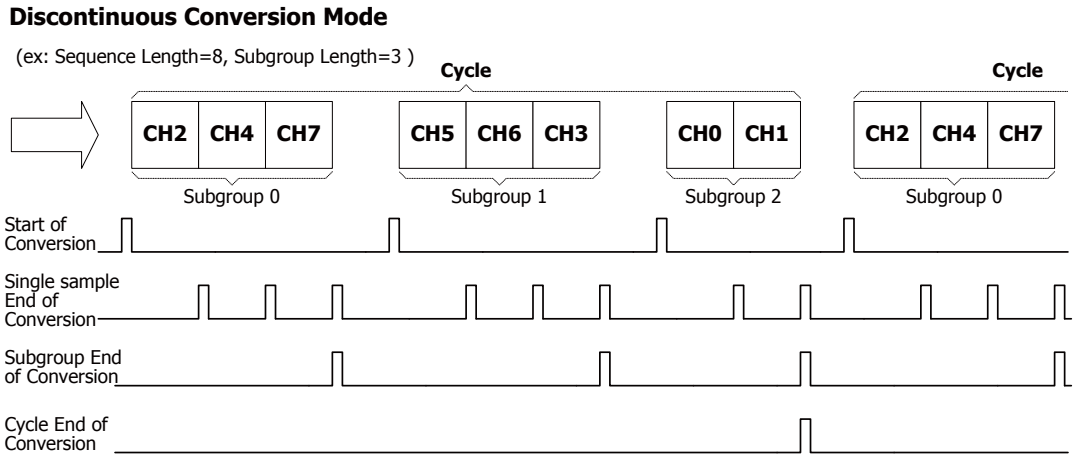


Figure 28. Discontinuous Conversion Mode

Start Conversion Trigger Sources

Data conversion can be initiated by a software trigger, a General-Purpose Timer Module (GPTM) event, a Motor Control Timer Module (MCTM) event, a Basic Function Timer Module (BFTM) event or an external trigger. Each trigger source can be enabled by setting the corresponding enable control bit in the ADCTCR register and then selected by configuring the associated selection bits in the ADCTSR register to start a group channel conversion.

An A/D converter conversion can be started by setting the software trigger bit, ADSC, in the ADCTSR register for the regular group channel when the software trigger enable bit, ADSW, in the ADCTCR register is set to 1. After the A/D converter starts converting the analog data, the corresponding enable bit ADSC will be cleared to 0 automatically.

The A/D converter can also be triggered to start a regular channel conversion by a TM event. The TM events include a GPTM or MCTM master trigger output MTO, four GPTM or MCTM channel outputs CH0~CH3 and a BFTM trigger output. If the corresponding TM trigger enable bit is set to 1 and the trigger output or the TM channel event is selected via the relevant TM event selection bits, the A/D converter will start a conversion when a rising edge of the selected trigger event occurs.

In addition to the internal trigger sources, the A/D converter can be triggered to start a conversion by an external trigger event. The external trigger event is derived from the external lines EXTIn. If the external trigger enable bit ADEXTI is set to 1 and the corresponding EXTI line is selected by configuring the ADEXTIS for regular group, the A/D converter will start a conversion when an EXTI line rising edge occurs.

Sampling Time Setting

Each conversion channel can be sampled with a different sampling time. By modifying the ADSTn [7:0] bits in the ADCSTRn (n=0~7) registers, the sampling time of the analog input signal can be determined.

The total conversion time (T_{conv}) is calculated using the following formula:

$$T_{conv}=T_{Sampling} + T_{Latency}$$

Where the minimum sampling time $T_{Sampling}$=1.5 cycles (when ADST [7:0]=0) and the minimum channel conversion latency $T_{Latency}$=12.5 cycles.

Example:

With the A/D Converter clock CK_ADC=14MHz and a sampling time=1.5 cycles:

$$T_{conv}=1.5 + 12.5=14 \text{ cycles}=1\mu s$$

Data Alignment

The ADC converted result has a right-aligned and unsigned output format as follows:

"0000_d11_d10_d9_d8_d7_d6_d5_d4_d3_d2_d1_d0".

If it is required to turn off the A/D converter, the A/D clock enable bit ADCEN should be cleared to 0 for at least two A/D clock cycles to disable the A/D converter function.

Analog Watchdog

The A/D converter includes a watchdog function to monitor the converted data. There are two kinds of thresholds for the watchdog monitor function, known as the watchdog upper threshold and watchdog lower threshold, which are specified in the Watchdog Upper and Lower Threshold Registers respectively. The watchdog monitor function is enabled by setting the watchdog upper and lower threshold monitor function enable bits, ADWUE and ADWLE, in the watchdog control register ADCWCR. The channel to be monitored can be specified by configuring the ADWCH and ADWALL bits. When the converted data is less or higher than the lower or upper threshold, as defined in the ADCLTR or ADCUTR registers respectively, the watchdog lower or upper threshold interrupt raw flags, ADIRAWL or ADIRAWU in the ADCIRAW register, will be asserted if the watchdog lower or upper threshold monitor function is enabled. If the lower or upper threshold interrupt raw flag is asserted and the corresponding interrupt is enabled by setting the ADIML or ADIMU bit in the ADCIME register, the A/D watchdog lower or upper threshold interrupt will be generated.

Interrupts

When an A/D conversion is completed, an End of Conversion EOC event will occur. There are three kinds of EOC events which are known as single sample EOC, subgroup EOC and cycle EOC for A/D conversion. A single sample EOC event will occur and the single sample EOC interrupt raw flag, ADIRAWS bits in the ADCIRAW register, will be asserted when a single channel conversion has completed. A subgroup EOC event will occur and the subgroup EOC interrupt raw flag, ADIRAWG in the ADCIRAW register, will be asserted when a subgroup conversion has completed. A cycle EOC event will occur and the cycle EOC interrupt raw flag, ADIRAWC bits in the ADCIRAW register, will be asserted when a cycle conversion is finished. When a single sample EOC, a subgroup EOC or a cycle EOC raw flag is asserted and the corresponding interrupt enable bit, ADIMC, ADIMG or ADIMS bit in the ADCIMR register, is set to 1, the associated interrupt will be generated.

After a conversion has completed, the 12-bit digital data will be stored in the associated ADCDRn register and the value of the data valid flag named as ADVLDn will be changed from low to high. The converted data should be read by the application program, after which the data valid flag ADVLDn will be automatically changed from high to low. Otherwise, a data overwrite event will occur and the data overwrite interrupt raw flag ADIRAWO bit in the ADCIRAW register will be asserted. When the related data overwrite raw flag is asserted, the data overwrite interrupt will be generated if the interrupt enable bit ADIMO in the ADCIMR register is set to 1.

If the A/D watchdog monitor function is enabled and the data after a channel conversion is less than the lower threshold or higher than the upper threshold, the watchdog lower or upper threshold interrupt raw flag ADIRAWL or ADIRAWU in the ADCIRAW register will be asserted. When the ADIRAWL or ADIRAWU flag is asserted and the corresponding interrupt enable bit, ADIML or ADIMU in the ADCIMR register, is set a watchdog lower or upper threshold interrupt will be generated.

The A/D Converter interrupt clear bits are used to clear the associated A/D converter interrupt raw and masked status bits. Writing 1 into the specific A/D converter interrupt clear bit in the A/D converter interrupt clear register ADCICLR will clear the corresponding A/D converter interrupt raw and masked status bits. These bits are automatically cleared to 0 by hardware after being set to 1.

PDMA Request

The converted channel value will be stored in the corresponding data register. The A/D Converter can inform the MCU using the A/D Converter EOC interrupt if a new conversion data is already stored in the ADCDRn register. Users also can determine the PDMA request is asserted by setting the ADDMAC, ADDMAG or ADDMAS bits in the ADCDMAR register. A PDMA request will be automatically generated at the end of each ADC conversion. The detail description will be introduced in the ADCDMAR register description.

Register Map

The following table shows the A/D Converter registers and reset values.

Table 26. A/D Converter Register Map

Register	Offset	Description	Reset Value
ADC Base Address=0x4001_0000			
ADCRST	0x004	ADC Reset Register	0x0000_0000
ADCCONV	0x008	ADC Regular Conversion Mode Register	0x0000_0000
ADCLST0	0x010	ADC Regular Conversion List Register 0	0x0000_0000
ADCLST1	0x014	ADC Regular Conversion List Register 1	0x0000_0000
ADCOFR0	0x030	ADC Input 0 Offset Register	0x0000_0000
ADCOFR1	0x034	ADC Input 1 Offset Register	0x0000_0000
ADCOFR2	0x038	ADC Input 2 Offset Register	0x0000_0000
ADCOFR3	0x03C	ADC Input 3 Offset Register	0x0000_0000
ADCOFR4	0x040	ADC Input 4 Offset Register	0x0000_0000
ADCOFR5	0x044	ADC Input 5 Offset Register	0x0000_0000
ADCOFR6	0x048	ADC Input 6 Offset Register	0x0000_0000
ADCOFR7	0x04C	ADC Input 7 Offset Register	0x0000_0000
ADCSTR0	0x070	ADC Input 0 Sampling Time Register	0x0000_0000
ADCSTR1	0x074	ADC Input 1 Sampling Time Register	0x0000_0000
ADCSTR2	0x078	ADC Input 2 Sampling Time Register	0x0000_0000
ADCSTR3	0x07C	ADC Input 3 Sampling Time Register	0x0000_0000
ADCSTR4	0x080	ADC Input 4 Sampling Time Register	0x0000_0000
ADCSTR5	0x084	ADC Input 5 Sampling Time Register	0x0000_0000
ADCSTR6	0x088	ADC Input 6 Sampling Time Register	0x0000_0000
ADCSTR7	0x08C	ADC Input 7 Sampling Time Register	0x0000_0000
ADCDR0	0x0B0	ADC Regular Conversion Data Register 0	0x0000_0000
ADCDR1	0x0B4	ADC Regular Conversion Data Register 1	0x0000_0000
ADCDR2	0x0B8	ADC Regular Conversion Data Register 2	0x0000_0000
ADCDR3	0x0BC	ADC Regular Conversion Data Register 3	0x0000_0000

Register	Offset	Description	Reset Value
ADCDR4	0x0C0	ADC Regular Conversion Data Register 4	0x0000_0000
ADCDR5	0x0C4	ADC Regular Conversion Data Register 5	0x0000_0000
ADCDR6	0x0C8	ADC Regular Conversion Data Register 6	0x0000_0000
ADCDR7	0x0CC	ADC Regular Conversion Data Register 7	0x0000_0000
ADCTCR	0x100	ADC Regular Trigger Control Register	0x0000_0000
ADCTSR	0x104	ADC Regular Trigger Source Register	0x0000_0000
ADCWCR	0x120	ADC Watchdog Control Register	0x0000_0000
ADCLTR	0x124	ADC Watchdog Lower Threshold Register	0x0000_0000
ADCUTR	0x128	ADC Watchdog Upper Threshold Register	0x0000_0000
ADCIMR	0x130	ADC Interrupt Mask Enable register	0x0000_0000
ADCIRAW	0x134	ADC Interrupt Raw Status Register	0x0000_0000
ADCIMASK	0x138	ADC Interrupt Masked Status Register	0x0000_0000
ADCICLR	0x13C	ADC Interrupt Clear Register	0x0000_0000
ADCDMAR	0x140	ADC PDMA Request Register	0x0000_0000

Register Descriptions

ADC Reset Register – ADCRST

This register is used to reset the A/D Converter by software.

Offset: 0x004

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved							ADRST
Type/Reset								RW 0

Bits	Field	Descriptions
[0]	ADRST	ADC Software Reset 0: No reset 1: Reset A/D converter except for the A/D Converter registers

ADC Regular Conversion Mode Register – ADCCONV

This register specifies the mode setting, sequence length and subgroup length of A/D Converter regular group conversion. Note that once the contents of the ADCCONV register have changed, any regular conversion presently in progress will be aborted and the A/D Converter will be reset. The application program has to wait for at least one A/D converter clock CK_ADC before issuing the next command.

Offset: 0x008

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved					ADSUBL		
Type/Reset						RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
	Reserved					ADSEQL		
Type/Reset						RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	Reserved							ADMODE
Type/Reset							RW 0	RW 0

Bits	Field	Descriptions
[18:16]	ADSUBL[2:0]	A/D Converter Regular Conversion Subgroup Length The ADSUBL field specifies the conversion channel length of each subgroup for the regular group in the discontinuous mode. The subgroup length is equal to ADSUB value plus 1. If the regular sequence length is not a multiple of the regular subgroup length, the last subgroup will be the rest of the regular group channels that have not been converted.
[10:8]	ADSEQL[2:0]	A/D Converter Regular Conversion Sequence Length The ADSEQL field specifies the conversion length of the whole sequence for the regular group. The sequence length is equal to the ADSEQL value plus 1.
[1:0]	ADMODE	A/D Converter Regular Conversion Mode Regular channels for the whole sequence continuously until the conversion mode is changed.

ADMODE [1:0]	Mode	Descriptions
00	One shot mode	After a start trigger, the conversion will be executed on the whole sequence of the regular channels once.
01	Reserved	—
10	Continuous mode	After a start trigger, the conversion will be executed on the regular channels for the whole sequence continuously until the conversion mode is changed.
11	Discontinuous mode	After a start trigger, the conversion will be executed on the current regular subgroup. When the last subgroup is finished, the conversion restarts from the first subgroup.

ADC Regular Conversion List Register 0 – ADCLST0

This register specifies the conversion sequence order No.0~No.3 of the A/D Converter regular group.

Offset: 0x010

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved			ADSEQ3				
Type/Reset				RW 0	RW 0	RW 0	RW 0	RW 0
	23	22	21	20	19	18	17	16
	Reserved			ADSEQ2				
Type/Reset				RW 0	RW 0	RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
	Reserved			ADSEQ1				
Type/Reset				RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	Reserved			ADSEQ0				
Type/Reset				RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[28:24]	ADSEQ3	A/D Converter Regular Conversion Sequence No.3 Define the A/D Converter input channel order No.3 of the regular conversion sequence. 0x00~0x07: ADC_IN0~ADC_IN7 0x08~0x0F: Reserved 0x10: Analog ground, V_{SSA} (V_{REF-}) 0x11: Analog power, V_{DDA} (V_{REF+}) 0x12~0x1F: Invalid setting. These values must not be selected as they may cause abnormal ADC operation
[20:16]	ADSEQ2	A/D Converter Regular Conversion Sequence No.2 Define the A/D Converter input channel order No.2 of the regular conversion sequence. 0x00~0x07: ADC_IN0~ADC_IN7 0x08~0x0F: Reserved 0x10: Analog ground, V_{SSA} (V_{REF-}) 0x11: Analog power, V_{DDA} (V_{REF+}) 0x12~0x1F: Invalid setting. These values must not be selected as they may cause abnormal ADC operation
[12:8]	ADSEQ1	A/D Converter Regular Conversion Sequence No.1 Define the A/D Converter input channel order No.1 of the regular conversion sequence. 0x00~0x07: ADC_IN0~ADC_IN7 0x08~0x0F: Reserved 0x10: Analog ground, V_{SSA} (V_{REF-}) 0x11: Analog power, V_{DDA} (V_{REF+}) 0x12~0x1F: Invalid setting. These values must not be selected as they may cause abnormal ADC operation
[4:0]	ADSEQ0	A/D Converter Regular Conversion Sequence No.0 Define the A/D Converter input channel order No.0 of the regular conversion sequence. 0x00~0x07: ADC_IN0~ADC_IN7 0x08~0x0F: Reserved 0x10: Analog ground, V_{SSA} (V_{REF-}) 0x11: Analog power, V_{DDA} (V_{REF+}) 0x12~0x1F: Invalid setting. These values must not be selected as they may cause abnormal ADC operation

ADC Regular Conversion List Register 1 – ADCLST1

This register specifies the conversion sequence order No.4~No.7 of the A/D Converter regular group.

Offset: 0x014

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved			ADSEQ7				
Type/Reset				RW 0	RW 0	RW 0	RW 0	RW 0
	23	22	21	20	19	18	17	16
	Reserved			ADSEQ6				
Type/Reset				RW 0	RW 0	RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
	Reserved			ADSEQ5				
Type/Reset				RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	Reserved			ADSEQ4				
Type/Reset				RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[28:24]	ADSEQ3	A/D Converter Regular Conversion Sequence No.3 Define the A/D Converter input channel order No.3 of the regular conversion sequence. 0x00~0x07: ADC_IN0~ADC_IN7 0x08~0x0F: Reserved 0x10: Analog ground, V_{SSA} (V_{REF-}) 0x11: Analog power, V_{DDA} (V_{REF+}) 0x12~0x1F: Invalid setting. These values must not be selected as they may cause abnormal ADC operation
[20:16]	ADSEQ2	A/D Converter Regular Conversion Sequence No.2 Define the A/D Converter input channel order No.2 of the regular conversion sequence. 0x00~0x07: ADC_IN0~ADC_IN7 0x08~0x0F: Reserved 0x10: Analog ground, V_{SSA} (V_{REF-}) 0x11: Analog power, V_{DDA} (V_{REF+}) 0x12~0x1F: Invalid setting. These values must not be selected as they may cause abnormal ADC operation
[12:8]	ADSEQ1	A/D Converter Regular Conversion Sequence No.1 Define the A/D Converter input channel order No.1 of the regular conversion sequence. 0x00~0x07: ADC_IN0~ADC_IN7 0x08~0x0F: Reserved 0x10: Analog ground, V_{SSA} (V_{REF-}) 0x11: Analog power, V_{DDA} (V_{REF+}) 0x12~0x1F: Invalid setting. These values must not be selected as they may cause abnormal ADC operation
[4:0]	ADSEQ0	A/D Converter Regular Conversion Sequence No.0 Define the A/D Converter input channel order No.0 of the regular conversion sequence. 0x00~0x07: ADC_IN0~ADC_IN7 0x08~0x0F: Reserved 0x10: Analog ground, V_{SSA} (V_{REF-}) 0x11: Analog power, V_{DDA} (V_{REF+}) 0x12~0x1F: Invalid setting. These values must not be selected as they may cause abnormal ADC operation

ADC Input n Offset Register – ADCOFRn, n=0~7

This register specifies the A/D Converter input channel n offset together with the offset cancellation function enable control.

Offset: 0x030~04C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	ADOFEn	Reserved			ADOFn			
Type/Reset	RW 0				RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	ADOFn							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15]	ADOFEn	ADC Input Channel n Offset Cancellation Enable (n=0~7) 0: ADC_INn offset cancellation function disabled 1: ADC_INn offset cancellation function enabled
[11:0]	ADOFn	ADC Input Channel n Offset Value (n=0~7) This field is used to store the A/D Converter input channel n offset value. If the offset cancellation function is enabled, the data stored in the corresponding data register ADCDRn will be the result derived from the raw conversion data from ADC conversion engine minus the input Channel n offset specified in this field.

ADC Input Sampling Time Register n – ADCSTRn, n=0~7

This register specifies the sampling time of A/D Converter channel n.

Offset: 0x070~08C

Reset value: 0x0000_0000 (0x0000_0002) Note

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	ADSTn							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[7:0]	ADSTn	A/D Converter Input Channel n Sampling Time (n=0~7) Sampling time=(ADSTn [7:0] + 1.5) A/D Conversion clock cycles. **Note:** The reset default value of the A/D Converter input channel 5 input sampling time is 0x02.

ADC Regular Conversion Data Register n – ADCDRn, n=0~7

This register is used to store the conversion data of the regular conversion sequence No.n.

Offset: 0x0B0~0CC

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	ADVLDn	Reserved						
Type/Reset	RC 0							
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	Reserved							
Type/Reset								
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	ADDn							
Type/Reset	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	ADDn							
Type/Reset	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0

Bits	Field	Descriptions
[31]	ADVLDn	A/D Converter Regular Conversion Data of the sequence No.n Valid Bit (n=0~7) 0: Data is invalid or has been read 1: New data are valid
[15:0]	ADDn	A/D Converter Regular Conversion Data of the sequence No.n (n=0~7) The regular channel conversion result of the sequence No.n defined in the ADCLST register.

ADC Regular Trigger Control Register – ADCTCR

This register contains the A/D start conversion trigger enable bits of the regular conversion.

Offset: 0x100

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved				BFTM	TM	ADEXTI	ADSW
Type/Reset					RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[3]	BFTM	A/D Converter Regular Conversion BFTM Event Trigger Enable control 0: Disable regular conversion triggered by BFTM event 1: Enable regular conversion triggered by BFTM event
[2]	TM	A/D Converter Regular Conversion GPTM or MCTM Event Trigger Enable control 0: Disable regular conversion triggered by GPTM or MCTM event 1: Enable regular conversion triggered by GPTM or MCTM event
[1]	ADEXTI	A/D Converter Regular Conversion EXTI Event Trigger Enable control 0: Disable regular conversion triggered by EXTI lines 1: Enable regular conversion triggered by EXTI lines
[0]	ADSW	A/D Converter Regular Conversion Software Trigger Enable control 0: Disable regular conversion triggered by software trigger bit 1: Enable regular conversion triggered by software trigger bit

ADC Regular Trigger Source Register – ADCTSR

This register contains the trigger source selection and the software trigger bit of the regular conversion.

Offset: 0x104

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved					TME		
Type/Reset						RW 0	RW 0	RW 0
	23	22	21	20	19	18	17	16
	Reserved				BFTMS	TMS		
Type/Reset					RW 0	RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
	Reserved				ADEXTIS			
Type/Reset					RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	Reserved							ADSC
Type/Reset								RW 0

Bits	Field	Descriptions
[26:24]	TME	GPTM or MCTM Trigger Event Selection of the A/D Converter Regular Conversion 000: GPTM or MCTM MTO rising edge 001: GPTM or MCTM CH0O rising edge 010: GPTM or MCTM CH1O rising edge 011: GPTM or MCTM CH2O rising edge 100: GPTM or MCTM CH3O rising edge Others: Reserved – Should not be used, otherwise, the conversion results will be unpredictable
[19]	BFTMS	BFTM Trigger Timer Selection of the A/D Converter Regular Conversion 0: BFTM0 1: BFTM1
[18:16]	TMS	GPTM or MCTM Trigger Timer Selection of the A/D Converter Regular Conversion 000: MCTM 010: GPTM0 011: GPTM1 Others: Reserved – Should not be used, otherwise, the conversion results will be unpredictable.
[11:8]	ADEXTIS	EXTI Trigger Source Selection of A/D Converter Regular Conversion 0x0: EXTI line 0 0x1: EXTI line 1 … 0xF: EXTI line 15
[0]	ADSC	A/D Converter Regular Conversion Software Trigger Bit 0: No effect 1: Start the regular conversion This bit is set by software to start the regular conversion manually and then cleared by hardware automatically at the next A/D Converter clock cycle.

ADC Watchdog Control Register – ADCWCR

This register provides the control bits and status of the A/D Converter watchdog function.

Offset: 0x120

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved				ADUCH			
Type/Reset					RO 0	RO 0	RO 0	RO 0
	23	22	21	20	19	18	17	16
	Reserved				ADLCH			
Type/Reset					RO 0	RO 0	RO 0	RO 0
	15	14	13	12	11	10	9	8
	Reserved				ADWCH			
Type/Reset					RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	Reserved					ADWALL	ADWUE	ADWLE
Type/Reset						RW 0	RW 0	RW 0

Bits	Field	Descriptions
[27:24]	ADUCH	Channel Upper Threshold Status 0000: ADC_IN0 converted data is higher than the threshold ADUT defined in the ADCUTR register 0001: ADC_IN1 converted data is higher than the threshold ADUT defined in the ADCUTR register ... 0111: ADC_IN7 converted data is higher than the threshold ADUT defined in the ADCUTR register Others: Reserved If one of these statuses is set to 1 by the watchdog monitor function, the status field must be stored in the user-defined memory location first in the corresponding ISR. Otherwise, the ADUCH field will be changed if another channel upper threshold event occurs.
[19:16]	ADLCH	Channel Lower Threshold Status 0000: ADC_IN0 converted data is lower than the threshold ADLT defined in the ADCLTR register 0001: ADC_IN1 converted data is lower than the threshold ADLT defined in the ADCLTR register ... 0111: ADC_IN7 converted data is lower than the threshold ADLT defined in the ADCLTR register Others: Reserved If one of these statuses is set to 1 by the watchdog monitor function, the status field must be stored in the user-defined memory location first in the corresponding ISR. Otherwise, the ADLCH field will be changed if another channel lower threshold event occurs.

Bits	Field	Descriptions
[11:8]	ADWCH	A/D Converter Channel Selection for Watchdog function 0000: ADC_IN0 is monitored 0001: ADC_IN1 is monitored ... 0111: ADC_IN7 is monitored Others: Reserved
[2]	ADWALL	A/D Converter Specific or All Channel control for watchdog function 0: Only the channel specified by the ADWCH field is monitored 1: All channels are monitored
[1]	ADWUE	A/D Converter Watchdog Upper Threshold Monitor Enable Bit 0: Disable the upper threshold monitor function 1: Enable the upper threshold monitor function
[0]	ADWLE	A/D Converter Watchdog Lower Threshold Monitor Enable Bit 0: Disable the lower threshold monitor function 1: Enable the lower threshold monitor function

ADC Watchdog Lower Threshold Register – ADCLTR

This register specifies the lower threshold of the A/D Converter watchdog function.

Offset: 0x124

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved				ADLT			
Type/Reset					RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	ADLT							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[11:0]	ADLT	A/D Converter Watchdog Lower Threshold Value Specify the lower threshold of the A/D Conversion data.

ADC Watchdog Upper Threshold Register – ADCUTR

This register specifies the upper threshold of the A/D Converter watchdog function.

Offset: 0x128

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved				ADUT			
Type/Reset					RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	ADUT							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[11:0]	ADUT	A/D Converter Watchdog Upper Threshold Value Specify the upper threshold of the A/D Conversion data.

ADC Interrupt Mask Enable Register – ADCIMR

This register contains the A/D Converter interrupt enable bits.

Offset: 0x130

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							ADIMO
Type/Reset								RW 0
	23	22	21	20	19	18	17	16
	Reserved						ADIMU	ADIML
Type/Reset							RW 0	RW 0
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved					ADIMC	ADIMG	ADIMS
Type/Reset						RW 0	RW 0	RW 0

Bits	Field	Descriptions
[24]	ADIMO	A/D Converter Regular Data Register Overwrite Interrupt Mask 0: A/D Converter regular data register overwrite interrupt is masked 1: A/D Converter regular data register overwrite interrupt is not masked
[17]	ADIMU	A/D Converter Watchdog Upper Threshold Interrupt Mask 0: A/D Converter watchdog upper threshold interrupt is masked 1: A/D Converter watchdog upper threshold interrupt is not masked
[16]	ADIML	A/D Converter Watchdog Lower Threshold Interrupt Mask 0: A/D Converter watchdog lower threshold interrupt is masked 1: A/D Converter watchdog lower threshold interrupt is not masked
[2]	ADIMC	A/D Converter Regular Cycle EOC Interrupt Mask 0: A/D Converter regular cycle end of conversion interrupt is masked 1: A/D Converter regular cycle end of conversion interrupt is not masked
[1]	ADIMG	A/D Converter Regular Subgroup EOC Interrupt Mask 0: A/D Converter regular subgroup end of conversion interrupt is masked 1: A/D Converter regular subgroup end of conversion interrupt is not masked
[0]	ADIMS	A/D Converter Regular Single EOC Interrupt Mask 0: A/D Converter regular single end of conversion interrupt is masked 1: A/D Converter regular single end of conversion interrupt is not masked

ADC Interrupt Raw Status Register – ADCIRAW

This register contains the A/D Converter interrupt raw status bits.

Offset: 0x134

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							ADIRAWO
Type/Reset								RO 0
	23	22	21	20	19	18	17	16
	Reserved						ADIRAWU	ADIRAWL
Type/Reset							RO 0	RO 0
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved					ADIRAWC	ADIRAWG	ADIRAWS
Type/Reset						RO 0	RO 0	RO 0

Bits	Field	Descriptions
[24]	ADIRAWO	A/D Converter Regular Data Register Overwrite Interrupt Raw Status 0: A/D Converter regular data register overwrite event does not occur 1: A/D Converter regular data register overwrite event occurs The A/D Converter regular data overwrite event will occur at the end of the 3rd regular conversion if the 1st regular conversion data has not been read by the application program.
[17]	ADIRAWU	A/D Converter Watchdog Upper Threshold Interrupt Raw Status 0: A/D Converter watchdog upper threshold event does not occur 1: A/D Converter watchdog upper threshold event occurs
[16]	ADIRAWL	A/D Converter Watchdog Lower Threshold Interrupt Raw Status 0: A/D Converter watchdog lower threshold event does not occur 1: A/D Converter watchdog lower threshold event occurs
[2]	ADIRAWC	A/D Converter Regular Cycle EOC Interrupt Raw Status 0: A/D Converter regular cycle end of conversion event does not occur 1: A/D Converter regular cycle end of conversion event occurs
[1]	ADIRAWG	A/D Converter Regular Subgroup EOC Interrupt Raw Status 0: A/D Converter regular subgroup end of conversion event does not occur 1: A/D Converter regular subgroup end of conversion event occurs
[0]	ADIRAWS	A/D Converter Regular Single EOC Interrupt Raw Status 0: A/D Converter regular single sample end of conversion event does not occur 1: A/D Converter regular single sample end of conversion event occurs

ADC Interrupt Masked Status Register – ADCIMASK

This register contains the A/D Converter interrupt masked status bits. The corresponding masked status will be set to 1 if the associated interrupt event occurs and the related enable bit is set to 1.

Offset: 0x138

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							ADIMASKO
Type/Reset								RO 0
	23	22	21	20	19	18	17	16
	Reserved						ADIMASKU	ADIMASKL
Type/Reset							RO 0	RO 0
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved					ADIMASKC	ADIMASKG	ADIMASKS
Type/Reset						RO 0	RO 0	RO 0

Bits	Field	Descriptions
[24]	ADIMASKO	A/D Converter Regular Data Register Overwrite Interrupt Masked Status 0: A/D Converter regular data register overwrite event does not occur or the related interrupt control is disabled 1: A/D Converter regular data register overwrite interrupt occurs as the related interrupt control is enabled
[17]	ADIMASKU	A/D Converter Watchdog Upper Threshold Interrupt Masked Status 0: A/D Converter watchdog upper threshold event does not occur or the related interrupt control is disabled 1: A/D Converter watchdog upper threshold interrupt occurs as the related interrupt control is enabled
[16]	ADIMASKL	A/D Converter Watchdog Lower Threshold Interrupt Masked Status 0: A/D Converter watchdog lower threshold event does not occur or the related interrupt control is disabled 1: A/D Converter watchdog lower threshold interrupt occurs as the related interrupt control is enabled
[2]	ADIMASKC	A/D Converter Regular Cycle EOC Interrupt Masked Status 0: A/D Converter regular cycle end of conversion event does not occur or the related interrupt control is disabled 1: A/D Converter regular cycle end of conversion interrupt occurs as the related interrupt control is enabled
[1]	ADIMASKG	A/D Converter Regular Subgroup EOC Interrupt Masked Status 0: A/D Converter regular subgroup end of conversion event does not occur or the related interrupt control is disabled 1: A/D Converter regular subgroup end of conversion interrupt occurs as the related interrupt control is enabled
[0]	ADIMASKS	A/D Converter Regular Single EOC Interrupt Masked Status 0: A/D Converter regular single sample end of conversion event does not occur or the related interrupt control is disabled 1: A/D Converter regular single sample end of conversion interrupt occurs as the related interrupt control is enabled

ADC Interrupt Clear Register – ADCICLR

This register provides the clear bits used to clear the interrupt raw and masked status of the A/D Converter. These bits are set to 1 by software to clear the interrupt status and automatically cleared to 0 by hardware after being set to 1.

Offset: 0x13C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							ADICLRO
Type/Reset								WO 0
	23	22	21	20	19	18	17	16
	Reserved						ADICLRU	ADICLRL
Type/Reset							WO 0	WO 0
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved					ADICLRC	ADICLRG	ADICLRS
Type/Reset						WO 0	WO 0	WO 0

Bits	Field	Descriptions
[24]	ADICLRO	A/D Converter Regular Data Register Overwrite Interrupt Status Clear Bit 0: No effect 1: Clear ADIRAWO and ADIMASKO bits
[17]	ADICLRU	A/D Converter Watchdog Upper Threshold Interrupt Status Clear Bit 0: No effect 1: Clear ADIRAWU and ADIMASKU bits
[16]	ADICLRL	A/D Converter Watchdog Lower Threshold Interrupt Status Clear Bit 0: No effect 1: Clear ADIRAWL and ADIMASKL bits
[2]	ADICLRC	A/D Converter Regular Cycle EOC Interrupt Status Clear Bit 0: No effect 1: Clear ADIRAWC and ADIMASKC bits
[1]	ADICLRG	A/D Converter Regular Subgroup EOC Interrupt Status Clear Bit 0: No effect 1: Clear ADIRAWG and ADIMASKG bits
[0]	ADICLRS	A/D Converter Regular Single EOC Interrupt Status Clear Bit 0: No effect 1: Clear ADIRAWS and ADIMASKS bits

ADC PDMA Request Register – ADCDMAR

This register contains the A/D Converter PDMA request enable bits.

Offset: 0x140

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved					ADDMAC	ADDMAG	ADDMAS
Type/Reset						RW 0	RW 0	RW 0

Bits	Field	Descriptions
[2]	ADDMAC	A/D Converter Regular Cycle EOC PDMA Request Enable Bit 0: Cycle end of conversion PDMA request is disabled 1: Cycle end of conversion PDMA request is enabled
[1]	ADDMAG	A/D Converter Regular Subgroup EOC PDMA Request Enable Bit 0: Subgroup end of conversion PDMA request is disabled 1: Subgroup end of conversion PDMA request is enabled
[0]	ADDMAS	A/D Converter Regular Single EOC PDMA Request Enable Bit 0: Single end of conversion PDMA request is disabled 1: Single end of conversion PDMA request is enabled

13 Operational Amplifier/Comparator (OPA/CMP)

Introduction

Two Operational Amplifiers/Comparators, OPA/CMP, are implemented within the devices. They can be configured either as Operational Amplifiers or Analog Comparators. When configured as comparators, they are capable of asserting interrupts to the NVIC.

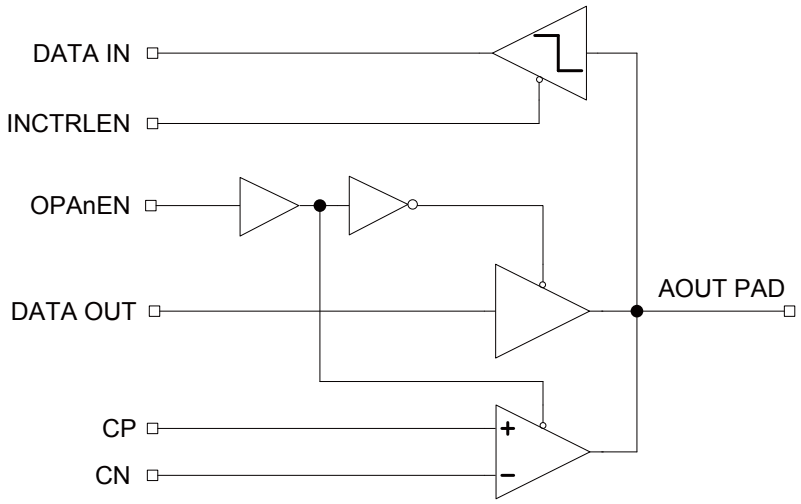


Figure 29. Simplied Block Diagram of OPA/CMP with Digital I/O

Features

- Operational Amplifier or Comparator function determined by software
- Supply Voltage Range: 2.5V~3.6V
- Typical Operating Current: 230μA (@V_{DD}=3.3V and Room Temperature=25˚C)
- Power Down Supply Current (OPAnEN=0 and AnOFM=0): < 0.1μA
- Comparator Offset (After Calibration): < ±1mV
- Comparator Response Time: < 2μs (@ overdrive voltage=10mV)

Functional Descriptions

Functional Diagram

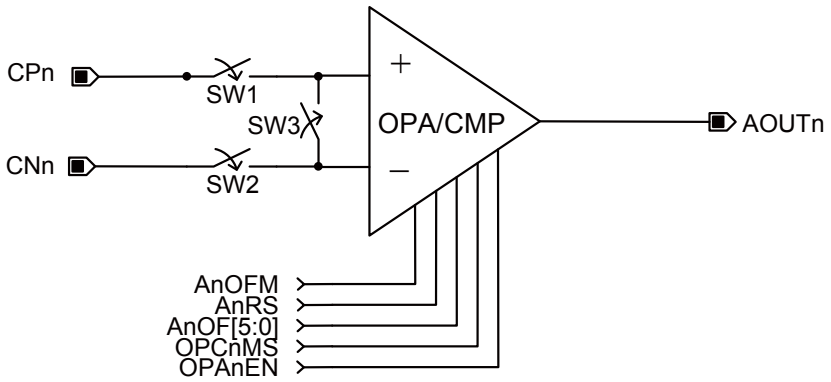


Figure 30. OPA/CMP Functional Diagram

Table 27. OPA/CMP Functional Signal Definition

AnOFM	AnRS	SW1	SW2	SW3
0	X	ON	ON	OFF
1	0	OFF	ON	ON
1	1	ON	OFF	ON

Interrupts and Status

The analog comparator can generate an interrupt when its output waveform generates a rising or falling edge and its corresponding interrupt enables control bit is also set.

For example, when a comparator output rising edge occurs, the comparator rising edge raw flag CRnRAW in the Comparator Raw Status Register CMPRSRn will be set. If the comparator output rising edge interrupt enable control bit CRnIEN in the Comparator Interrupt Enable Register CMPIERn is enabled, the comparator output rising edge masked interrupt status bit CRnIS in the Comparator Masked Interrupt Status Register CMPISRn, will be set when the comparator output rising edge occurs. An interrupt will then be generated and sent to the NVIC unit. Writing 1 into the comparator output rising edge interrupt clear bit CRnICLR in the Comparator Interrupt Clear Register CMPICLRn will clear the CRnIS and CRnRAW status bits. The comparator output falling edge interrupt also has the same corresponding interrupt setting.

Offset Cancellation Procedures

The device provides an offset cancellation function. Users can cancel the input voltage offset by using a specific procedure by configuring the corresponding registers. The offset cancellation procedure is shown in the following steps.

Cancellation procedure:

1. Set the AnOFM bit in the OPACRn register to 1 to enter the offset cancellation mode.
2. Configure the AnRS bit in the OPACRn register to select whether the reference voltage input comes from the comparator negative or positive input pin. If the AnRS bit is set to 1, the reference voltage input will come from the comparator positive input pin. Otherwise, the reference voltage input will come from the comparator negative input pin when the AnRS bit is cleared to 0.
3. Specify the OFVCRn register with a value of 0x00 to start the cancellation procedure.
4. If the CMPnS bit in the OPACRn register is equal to 0, then increase the OFVCRn register content, AnOF, by 1 and check whether the CMPnS bit state has changed from 0 to 1. If not, then keep increasing the register content until the CMPnS bit state changes from 0 to 1.
5. When the CMPnS bit changes to 1, then the AnOF data which is equal to N or (N-1) is the specific value written into the OFVCRn register to cancel the comparator input offset voltage.

Note that the reference input voltage must be in the range from (V_{DDA}-1.2V) to (V_{SSA}+0.5V) to obtain a more accurate cancellation result.

Register Map

The following table shows the OPA/CMP registers and reset values.

Table 28. OPA/CMP Register Map

Register	Offset	Description	Reset Value
OPACMP Base Address=0x4001_8000			
OPACR0	0x000	Operational Amplifier Control Register 0	0x0000_0000
OFVCR0	0x004	Comparator Input Offset Voltage Cancellation Register 0	0x0000_0000
CMPIER0	0x008	Comparator Interrupt Enable Register 0	0x0000_0000
CMPRSR0	0x00C	Comparator Raw Status Register 0	0x0000_0000
CMPISR0	0x010	Comparator Masked Interrupt Status Register 0	0x0000_0000
CMPICLR0	0x014	Comparator Interrupt Clear Register 0	NA
OPACR1	0x100	Operational Amplifier Control Register 1	0x0000_0000
OFVCR1	0x104	Comparator Input Offset Voltage Cancellation Register 1	0x0000_0000
CMPIER1	0x108	Comparator Interrupt Enable Register 1	0x0000_0000
CMPRSR1	0x10C	Comparator Raw Status Register 1	0x0000_0000
CMPISR1	0x110	Comparator Masked Interrupt Status Register 1	0x0000_0000
CMPICLR1	0x114	Comparator Interrupt Clear Register 1	NA

Register Descriptions

Operational Amplifier Control Register n – OPACRn, n=0 or 1

This register contains the OPA/CMP enable control, the OPA/CMP mode selection, input offset cancellation control bits and the comparator digital output status.

Offset: 0x000 (0), 0x100 (1)

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							CMPnS
Type/Reset								RO 0
	7	6	5	4	3	2	1	0
	Reserved				AnRS	AnOFM	OPCnMS	OPAnEN
Type/Reset					RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[8]	CMPnS	Comparator Digital Output Status This bit is read only and has the same polarity as Comparator output. It can be used for software monitor the Comparator output in the input offset voltage cancellation mode.
[3]	AnRS	Operational Amplifier Input Offset Cancellation Reference Voltage Selection 0: Comparator negative input is selected as the reference input 1: Comparator positive input is selected as the reference input
[2]	AnOFM	Operational Amplifier/Comparator Mode or Input Offset Voltage Cancellation Mode Selection 0: Operational Amplifier/Comparator mode 1: Input offset voltage cancellation mode
[1]	OPCnMS	Operational Amplifier or Comparator Mode Selection 0: Operational Amplifier mode 1: Comparator mode
[0]	OPAnEN	Operational Amplifier/Comparator Enable Control 0: Disable Operational Amplifier/Comparator (entering the power down mode) 1: Enable Operational Amplifier/Comparator

Comparator Input Offset Voltage Cancellation Register n – OFVCRn, n=0 or 1

The register is used to cancel the comparator n input offset voltage.

Offset: 0x004 (0), 0x104 (1)

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved		AnOF					
Type/Reset			RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[5:0]	AnOF	Operational Amplifier/Comparator Input Offset Voltage Cancellation Control 000000: Minumun ... 100000: Center ... 111111: Maxumun

Comparator Interrupt Enable Register n – CMPIERn, n=0 or 1

This register provides the comparator n output transition interrupt enable control bits.

Offset: 0x008 (0), 0x108 (1)

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved						CRnIEN	CFnIEN
Type/Reset							RW 0	RW 0

Bits	Field	Descriptions
[1]	CRnIEN	Comparator Output Rising Edge Interrupt Enable Control 0: Comparator output rising edge interrupt is disabled 1: Comparator output rising edge interrupt is enabled
[0]	CFnIEN	Comparator Output Falling Edge Interrupt Enable Control 0: Comparator output falling edge interrupt is disabled 1: Comparator output falling edge interrupt is enabled

Comparator Raw Status Register n – CMPRSRn, n=0 or 1

This register contains the comparator n output transition event raw status.

Offset: 0x00C (0), 0x10C (1)

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved						CRnRAW	CFnRAW
Type/Reset							RO 0	RO 0

Bits	Field	Descriptions
[1]	CRnRAW	Comparator Output Rising Edge Raw Flag 0: No Comparator output rising edge occurs 1: Comparator output rising edge occurs This bit can be cleared by writing 1 into the CRnICLR bit in the CMPICLRn register.
[0]	CFnRAW	Comparator Falling Edge Interrupt Raw Flag 0: No Comparator output falling edge occurs 1: Comparator output falling edge occurs This bit can be cleared by writing 1 into the CFnICLR bit in the CMPICLRn register.

Comparator Masked Interrupt Status Register n – CMPISRn, n=0 or 1

This register contains the comparator n transition event masked interrupt status.

Offset: 0x010 (0), 0x110 (1)

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved						CRnIS	CFnIS
Type/Reset							RO 0	RO 0

Bits	Field	Descriptions
[1]	CRnIS	Comparator Output Rising Edge Masked Interrupt Flag 0: No Comparator output rising edge occurs or the Comparator output rising edge interrupt is disabled 1: Comparator output rising edge occurs and the Comparator output rising edge interrupt is enabled
[0]	CFnIS	Comparator Output Falling Edge Masked Interrupt Flag Bit 0: No Comparator output falling edge occurs or the Comparator output falling edge interrupt is disabled 1: Comparator output falling edge occurs and the Comparator output falling edge interrupt is enabled

Comparator Interrupt Clear Register n – CMPICLRn, n=0 or 1

The register provides the interrupt status clear bits used to indicate the comparator n output transition interrupt raw and masked status. These bits are set to 1 by software to clear the associated interrupt raw and masked status bits and cleared to 0 by hardware automatically after being set to 1.

Offset: 0x014 (0), 0x114 (1)

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved						CRnICLR	CFnICLR
Type/Reset							WO 0	WO 0

Bits	Field	Descriptions
[1]	CRnICLR	Comparator Output Rising Edge Interrupt status Clear Control 0: No effect 1: Comparator output rising edge interrupt raw status and masked status is cleared
[0]	CFnICLR	Comparator Output Falling Edge Interrupt status Clear Control Bit 0: No effect 1: Comparator output falling edge interrupt raw status and masked status is cleared

14 General-Purpose Timers (GPTM0 & GPTM1)

Introduction

The General-Purpose Timer consists of one 16-bit up/down-counter, four 16-bit Capture/Compare Registers (CCRs), one 16-bit Counter-Reload Register (CRR) and several control/status registers. It can be used for a variety of purposes including general timer, input signal pulse width measurement or output waveform generation such as single pulse generation or PWM output. The GPTM supports an encoder interface using a quadrature decoder with two inputs.

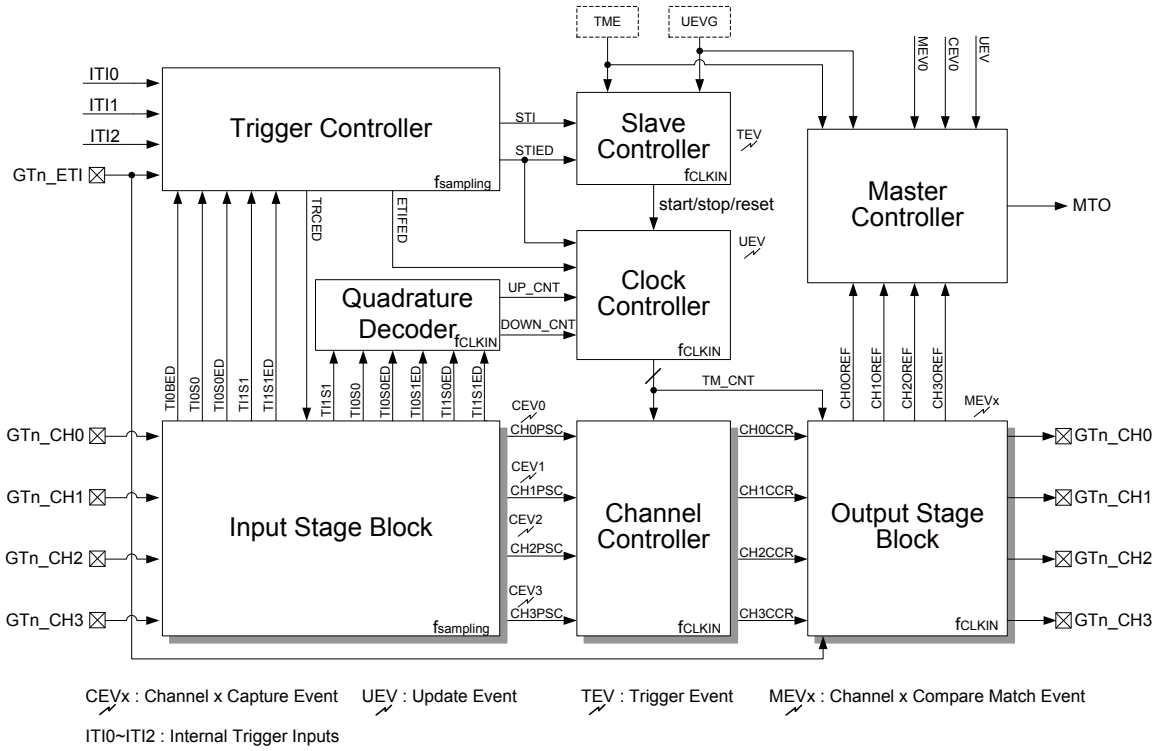


Figure 31. GPTM Block Diagram

Features

- 16-bit up/down auto-reload counter
- 16-bit programmable prescaler that allows division of the counter clock frequency by any factor between 1 and 65536
- Up to 4 independent channels for:
  - Input Capture function
  - Compare Match Output
  - Generation of PWM waveform – Edge-aligned and Center-aligned Counting Modes
  - Single Pulse Mode Output
- Encoder interface controller with two inputs using quadrature decoder
- Synchronization circuit to control the timer with external signals and to interconnect several timers together
- Interrupt/PDMA generation with the following events:
  - Update event
  - Trigger event
  - Input capture event
  - Output compare match event
- GPTM Master/Slave mode controller

Functional Descriptions

Counter Modes

Up-counting

In this mode the counter counts continuously from 0 to the counter-reload value, which is defined in the CRR register, in a count-up direction. Once the counter reaches the counter-reload value, the Timer Module generates an overflow event and the counter restarts to count once again from 0. This action will continue repeatedly. The counting direction bit DIR in the CNTCFR register should be set to 0 for the up-counting mode.

When the update event is generated by setting the UEVG bit in the EVGR register to 1, the counter value will also be initialized to 0.

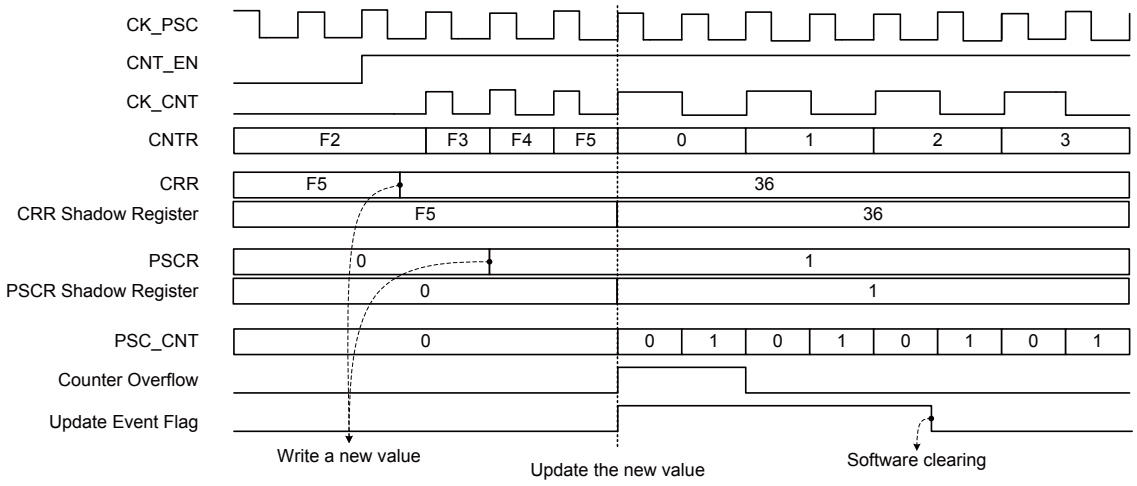


Figure 32. Up-counting Example

Down-counting

In this mode the counter counts continuously from the counter-reload value, which is defined in the CRR register, to 0 in a count-down direction. Once the counter reaches 0, the Timer module generates an underflow event and the counter restarts to count once again from the counter-reload value. This action will continue repeatedly. The counting direction bit DIR in the CNTCFR register should be set to 1 for the down-counting mode.

When the update event is set by the UEVG bit in the EVGR register, the counter value will also be initialized to the counter-reload value.

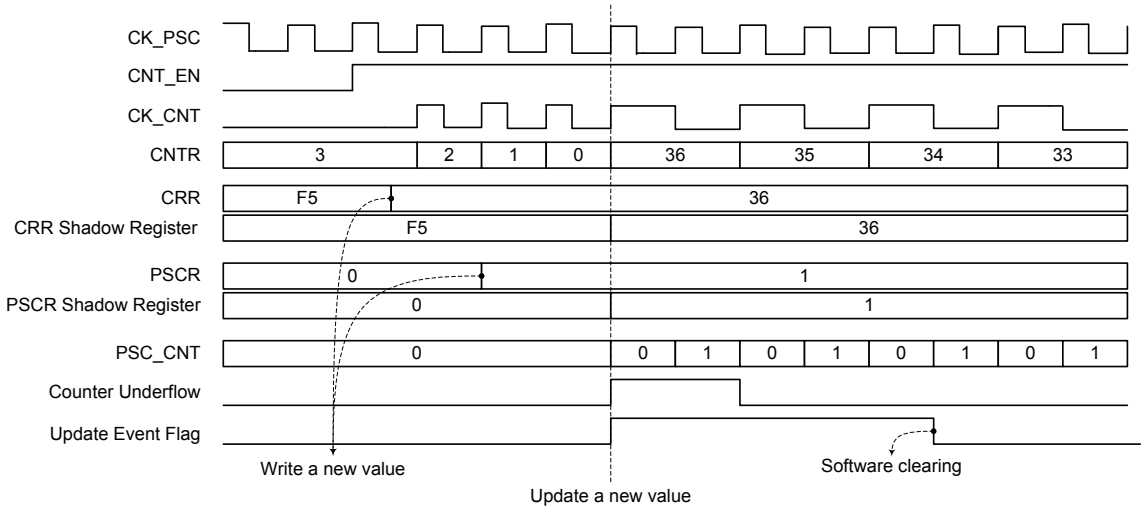


Figure 33. Down-counting Example

Center-aligned Counting

In the center-aligned counting mode, the counter counts up from 0 to the counter-reload value and then counts down to 0 alternatively. The Timer module generates an overflow event when the counter counts to the counter-reload value in the up-counting mode and generates an underflow event when the counter counts to 0 in the down-counting mode. The counting direction bit DIR in the CNTCFR register is read-only and indicates the counting direction when in the center-aligned counting mode. The counting direction is updated by hardware automatically.

Setting the UEVG bit in the EVGR register will initialize the counter value to 0 irrespective of whether the counter is counting up or down in the center-aligned counting mode.

The UEVIF bit in the INTSR register can be set to 1 according to the CMSEL field setting in the CNTCFR register. When CMSEL=0x01, an underflow event will set the UEVIF bit to 1. When CMSEL=0x10, an overflow event will set the UEVIF bit to 1. When CMSEL=0x11, either underflow or overflow event will set the UEVIF bit to 1.

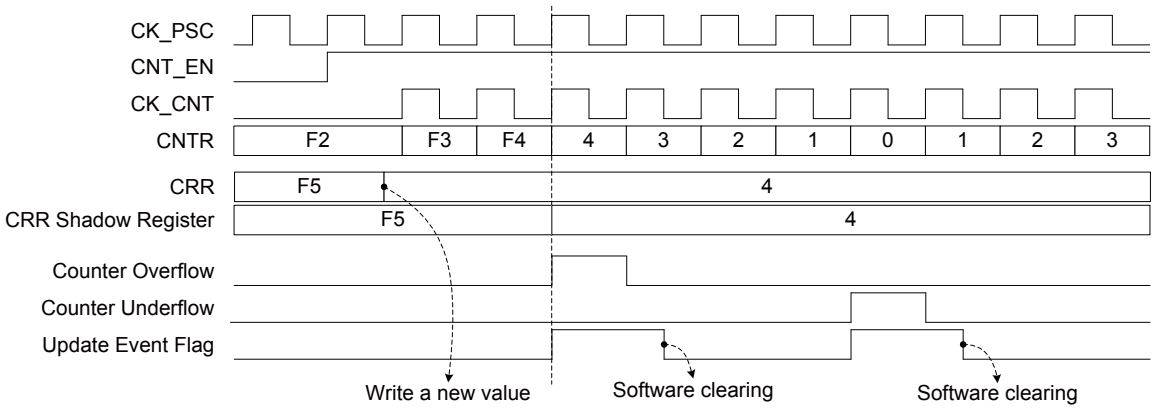


Figure 34. Center-aligned Counting Example

Clock Controller

The following describes the Timer Module clock controller which determines the clock source of the internal prescaler counter.

- Internal APB clock f_{CLKIN}:
  The default internal clock source is the APB clock f_{CLKIN} used to drive the counter prescaler when the slave mode is disabled. When the slave mode selection bits SMSEL are set to 0x4, 0x5 or 0x6, the internal APB clock f_{CLKIN} is the counter prescaler driving clock source.

- Quadrature Decoder:
  To select Quadrature Decoder mode the SMSEL field should be set to 0x1, 0x2 or 0x3 in the MDCFR register. The Quadrature Decoder function uses two input states of the GTn_CH0 and GTn_CH1 pins to generate the clock pulse to drive the counter prescaler. The counting direction bit DIR is modified by hardware automatically at each transition on the input source signal.

- STIED:
  The counter prescaler can count during each rising edge of the STI signal. This mode can be selected by setting the SMSEL field to 0x7 in the MDCFR register. Here the counter will act as an event counter. The input event, known as STI here, can be selected by setting the TRSEL field to an available value except the value of 0x0. When the STI signal is selected as the clock source, the internal edge detection circuitry will generate a clock pulse during each STI signal rising edge to drive the counter prescaler. It is important to note that if the TRSEL field is set to 0x0 to select the software UEVG bit as the trigger source, then when the SMSEL field is set to 0x7, the counter will be updated instead of counting.

- ETIFED:
  The counter prescaler can be driven to count during each rising edge on ETIF. This mode can be selected by setting the ECME bit in the TRCFR register to 1. The other way to select the ETIF signal as the clock source is to set the SMSEL field to 0x7 and the TRSEL field to 0x3 respectively. When the clock source is selected to come from the ETIF signal, the Trigger Controller including the edge detection circuitry will generate a clock pulse during each ETIF signal rising edge to clock the counter prescaler.

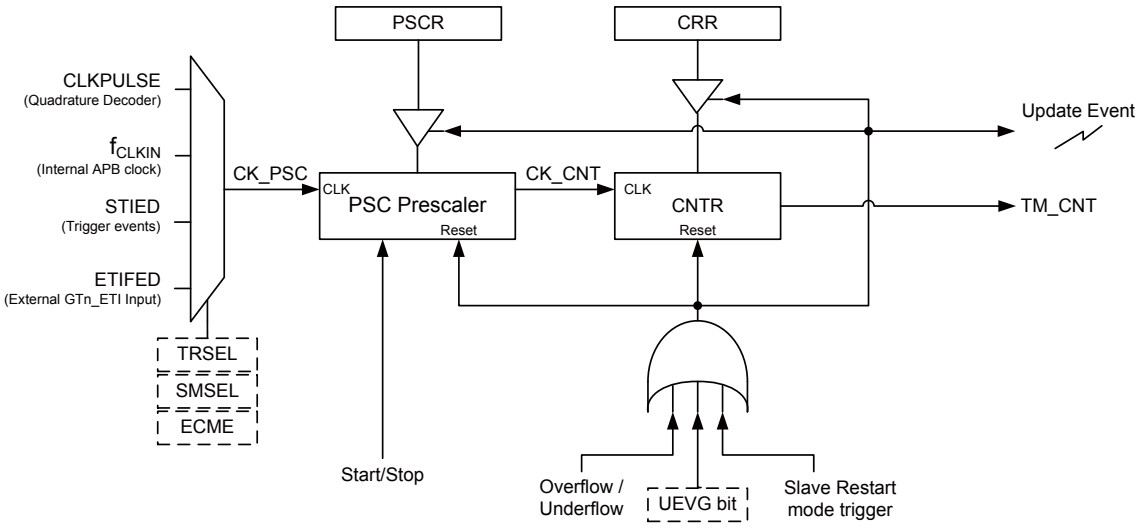


Figure 35. GPTM Clock Selection Source

Trigger Controller

The trigger controller is used to select the trigger source and setup the trigger level or edge trigger condition. The active polarity of the external trigger input signal GTn_ETI can be configured by the External Trigger Polarity control bit ETIPOL in the GPTM Trigger Configuration Register TRCFR. The frequency of the external trigger input can be divided by configuring the related bits, named as External Trigger Prescaler control bits ETIPSC, in the TRCFR register. The trigger signal can also be filtered by configuring the External Trigger Filter ETF selection bits in the TRCFR register if a filtered signal is necessary for specific applications. For the internal trigger input, it can be selected by the Trigger Selection bits TRSEL in the TRCFR register. For all the trigger sources except the UEVG bit software trigger, the internal edge detection circuitry will generate a clock pulse at each trigger signal rising edge to stimulate some GPTM functions which are triggered by a trigger signal rising edge.

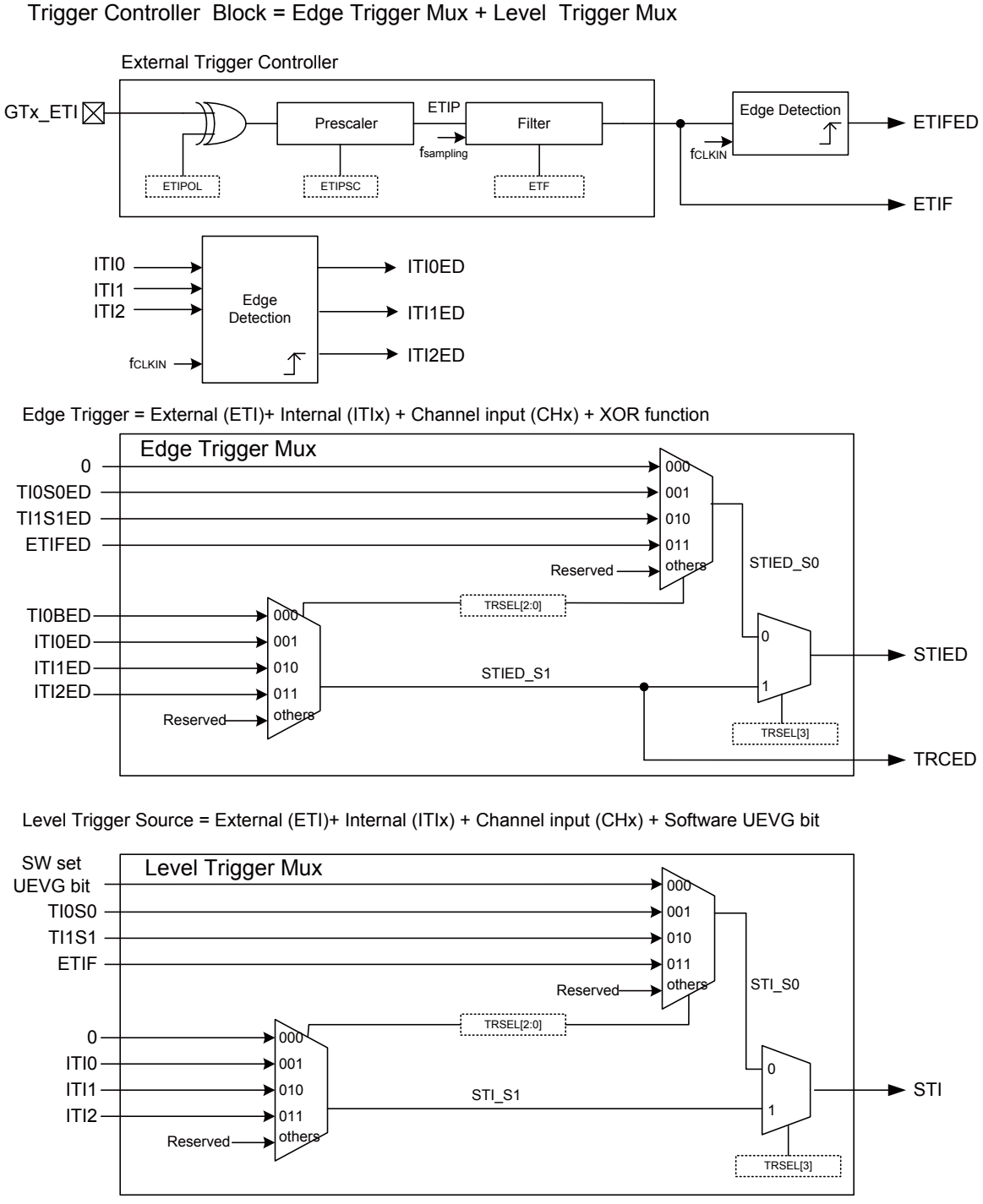


Figure 36. Trigger Control Block

Slave Controller

The GPTM can be synchronized with an internal/external trigger in several modes including the Restart mode, the Pause mode and the Trigger mode which is selected by the SMSEL field in the MDCFR register. The trigger input of these modes comes from the STI signal which is selected by the TRSEL field in the TRCFR register. The operation modes in the Slave Controller are described in the accompanying sections.

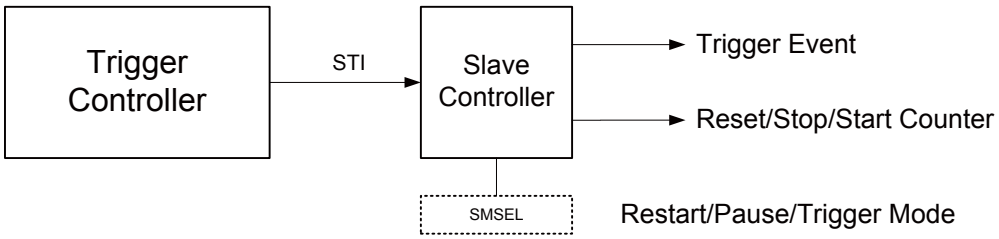


Figure 37. Slave Controller Diagram

Restart Mode

The counter and its prescaler can be reinitialized in response to a rising edge of the STI signal. When a STI rising edge occurs, the update event software generation bit named UEVG will automatically be asserted by hardware and the trigger event flag will also be set. Then the counter and prescaler will be reinitialized. Although the UEVG bit is set to 1 by hardware, the update event does not really occur. It depends upon whether the update event disable control bit UEVDIS is set to 1 or not. If the UEVDIS is set to 1 to disable the update event to occur, no update event will be generated, however the counter and prescaler are still reinitialized when the STI rising edge occurs. If the UEVDIS bit in the CNTCFR register is cleared to enable the update event to occur, an update event will be generated together with the STI rising edge, then all the preloaded registers will be updated.

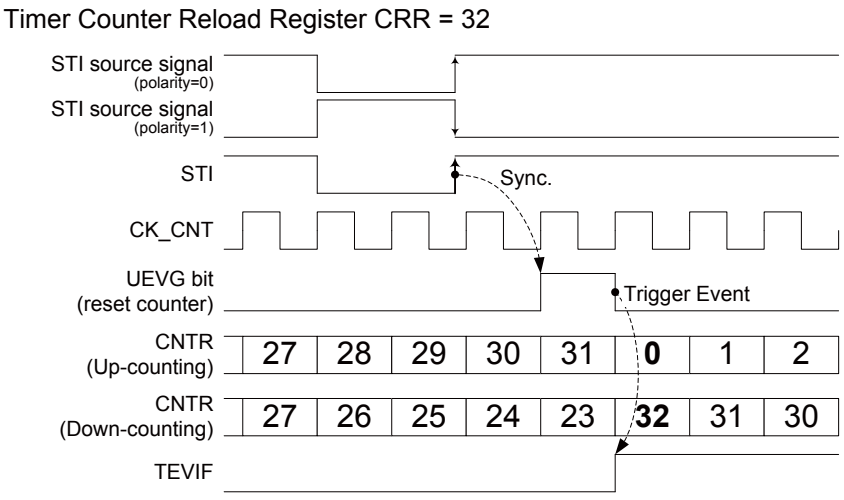


Figure 38. GPTM in Restart Mode

Pause Mode

In the Pause Mode, the selected STI input signal level is used to control the counter start/stop operation. The counter starts to count when the selected STI signal is at a high level and stops counting when the STI signal is changed to a low level, here the counter will maintain its present value and will not be reset. Since the Pause function depends upon the STI level to control the counter stop/start operation, the selected STI trigger signal can not be derived from the TI0BED signal.

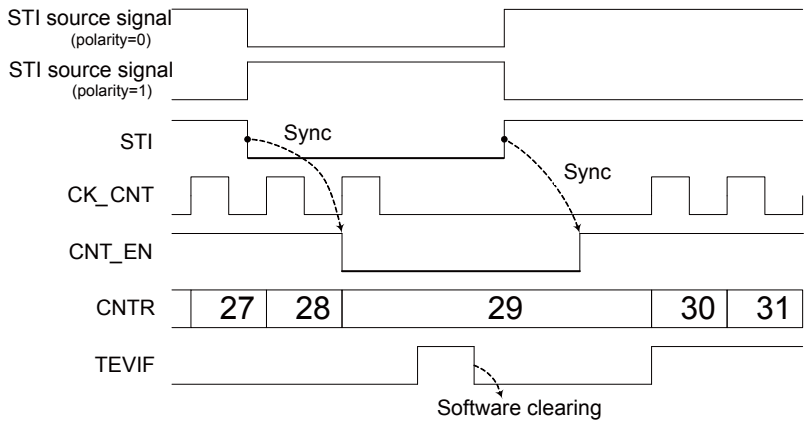


Figure 39. GPTM in Pause Mode

Trigger Mode

After the counter is disabled to count, the counter can resume counting when a STI rising edge signal occurs. When an STI rising edge occurs, the counter will start to count from the current value in the counter. Note that if the STI signal is selected to be derived from the UEVG bit software trigger, the counter will not resume counting. When software triggering using the UEVG bit is selected as the STI source signal, there will be no clock pulse generated which can be used to make the counter resume counting. Note that the STI signal is only used to enable the counter to resume counting and has no effect on controlling the counter to stop counting.

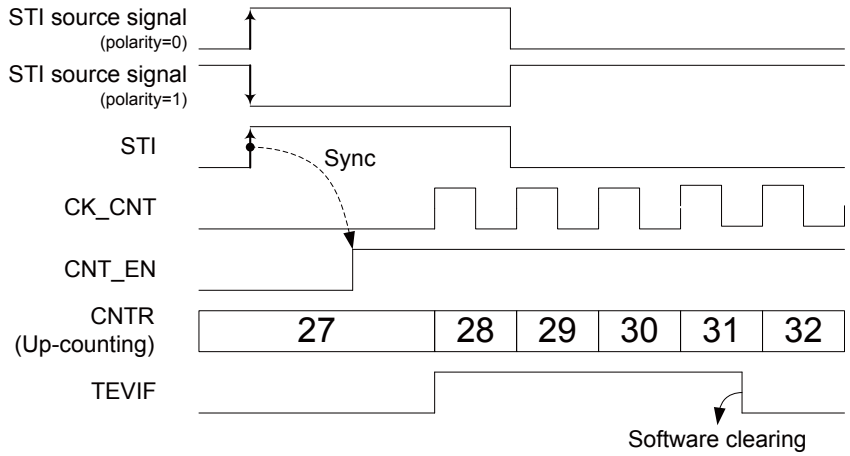


Figure 40. GPTM in Trigger Mode

Master Controller

The GPTMs and MCTMs can be linked together internally for timer synchronization or chaining. When one GPTM is configured to be in the Master Mode, the GPTM Master Controller will generate a Master Trigger Output (MTO) signal which can reset, start, stop the Slave counter or be a clock source of the Salve counter. This can be selected by the MMSEL field in the MDCFR register to trigger or drive another GPTM or MCTM, which is configured in the Slave Mode.

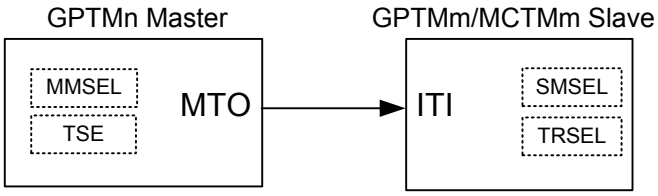


Figure 41. Master GPTMn and Slave GPTMm/MCTMm Connection

The Master Mode Selection bits, MMSEL, in the MDCFR register are used to select the MTO source for synchronizing another slave GPTM or MCTM.

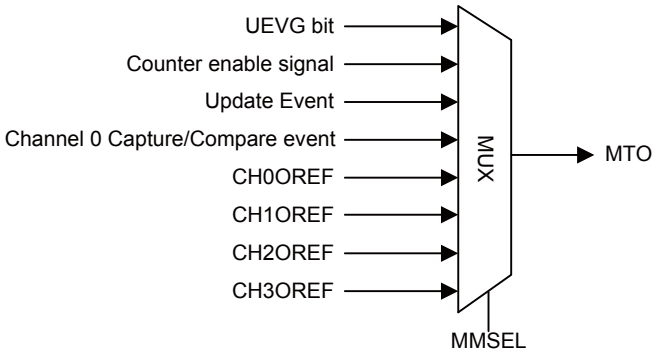


Figure 42. MTO Selection

For example, setting the MMSEL field to 0x5 is to select the CH1OREF signal as the MTO signal to synchronize another slave GPTM or MCTM. For a more detailed description, refer to the related MMSEL field definitions in the MDCFR register.

Channel Controller

The GPTM has four independent channels which can be used as capture inputs or compare match outputs. Each capture input or compare match output channel is composed of a preload register and a shadow register. Data access of the APB bus is always through the read/write preload register.

When used in the input capture mode, the counter value is captured into the CHxCCR shadow register first and then transferred into the CHxCCR preload register when the capture event occurs.

When used in the compare match output mode, the contents of the CHxCCR preload register is copied into the associated shadow register; the counter value is then compared with the register value.

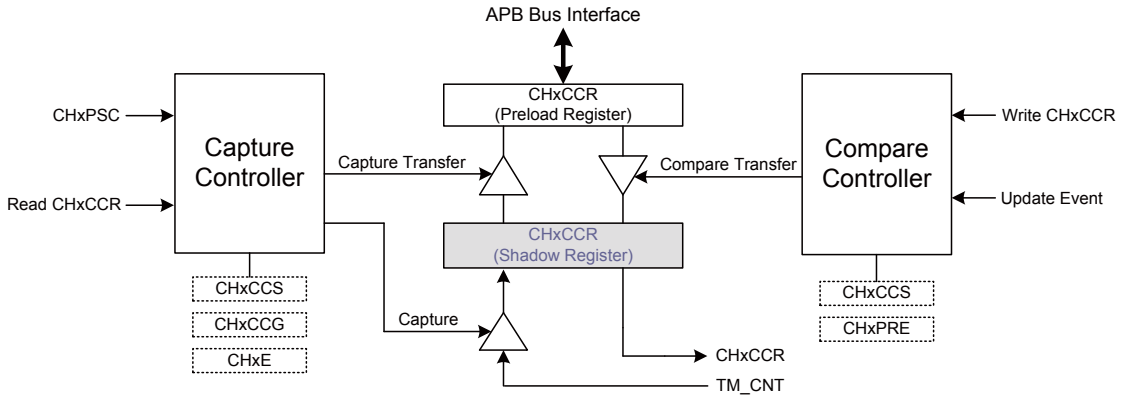


Figure 43. Capture/Compare Block Diagram

Capture Counter Value Transferred to CHxCCR

When the channel is used as a capture input, the counter value is captured into the Channel Capture/Compare Register (CHxCCR) when an effective input signal transition occurs. Once the capture event occurs, the CHxCCIF flag in the INTSR register is set accordingly. If the CHxCCIF bit is already set, i.e., the flag has not yet been cleared by software, and another capture event on this channel occurs, the corresponding channel Over-Capture flag, named CHxOCF, will be set.

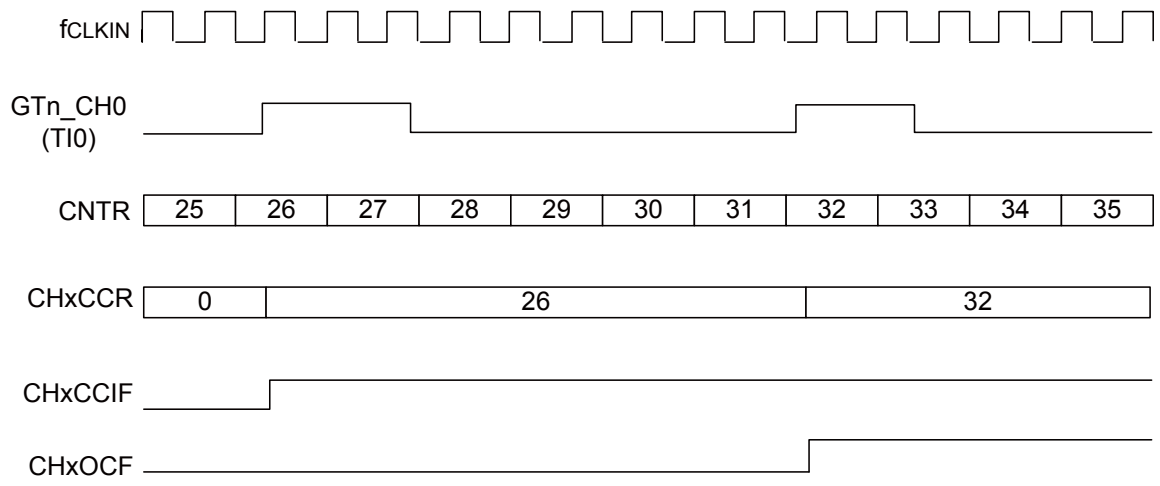


Figure 44. Input Capture Mode

Pulse Width Measurement

The input capture mode can be also used for pulse width measurement from signals on the GTn_CHx pins (TIx). The following example shows how to configure the GPTM operated in the input capture mode to measure the high pulse width and the input period on the GTn_CH0 pin using channel 0 and channel 1. The basic steps are shown as follows.

- Configure the capture channel 0 (CH0CCS=0x1) to select the TI0 signal as the capture input
- Configure the CH0P bit to 0 to choose the rising edge of the TI0 input as the active polarity
- Configure the capture channel 1 (CH1CCS=0x2) to select the TI0 signal as the capture input
- Configure the CH1P bit to 1 to choose the falling edge of the TI0 input as the active polarity
- Configure the TRSEL bits to 0x0001 to select TI0S0 as the trigger input
- Configure the Slave controller to operate in the Restart mode by setting the SMSEL field in the MDCFR register to 0x4
- Enable the input capture mode by setting the CH0E and CH1E bits in the CHCTR register to 1

As the following diagram shows, the high pulse width on the GTn_CH0 pin will be captured into the CH1CCR register while the input period will be captured into the CH0CCR register after input capture operation.

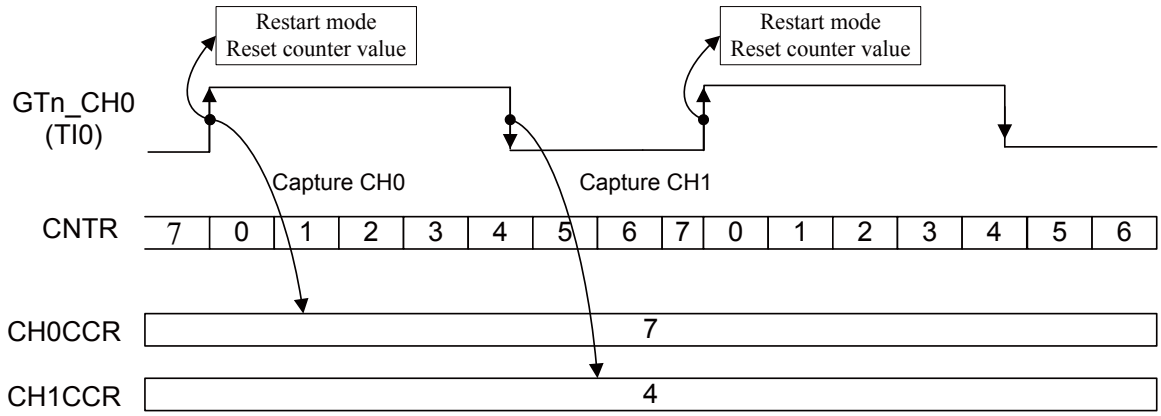


Figure 45. PWM Pulse Width Measurement Example

Input Stage

The input stage consists of a digital filter, a channel polarity selection, edge detection and a channel prescaler. The channel 0 input signal (TI0) can be chosen to come from the GTn_CH0 signal or the Excusive-OR function of the GTn_CH0, GTn_CH1 and GTn_CH2 signals. The channel input signal (TIx) is sampled by a digital filter to generate a filtered input signal TIxFP. Then the channel polarity and the edge detection block can generate a TIxSxED signal for the input capture function. The effective input event number can be set by the channel input prescaler register (CHxPSC).

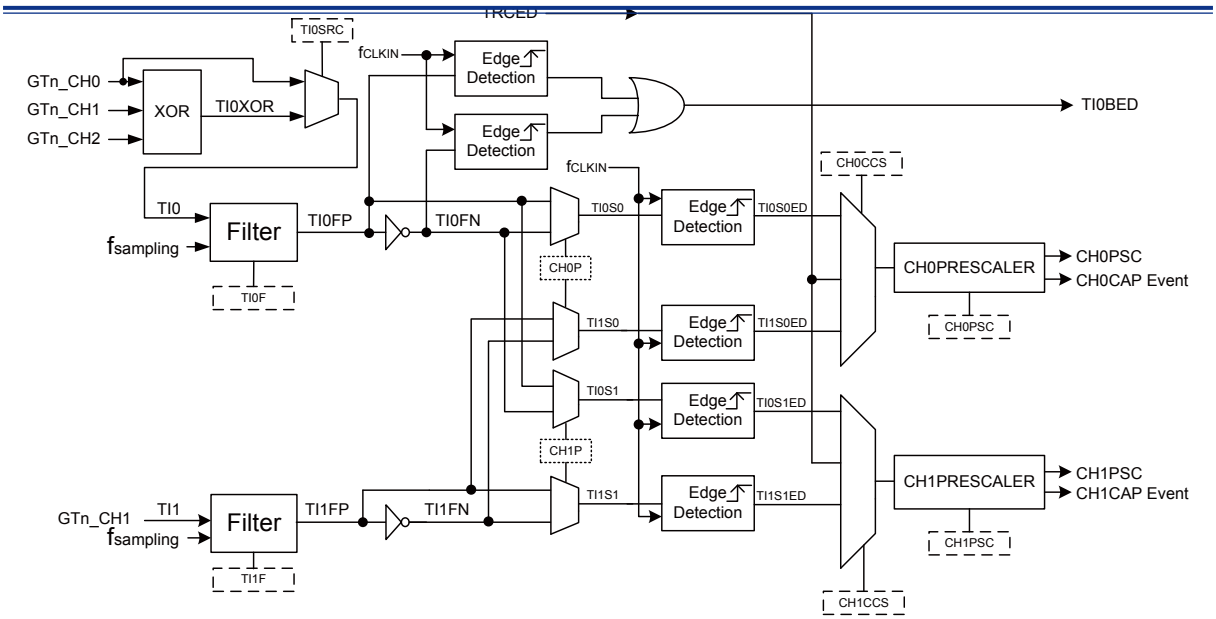


Figure 46. Channel 0 and Channel 1 Input Stage

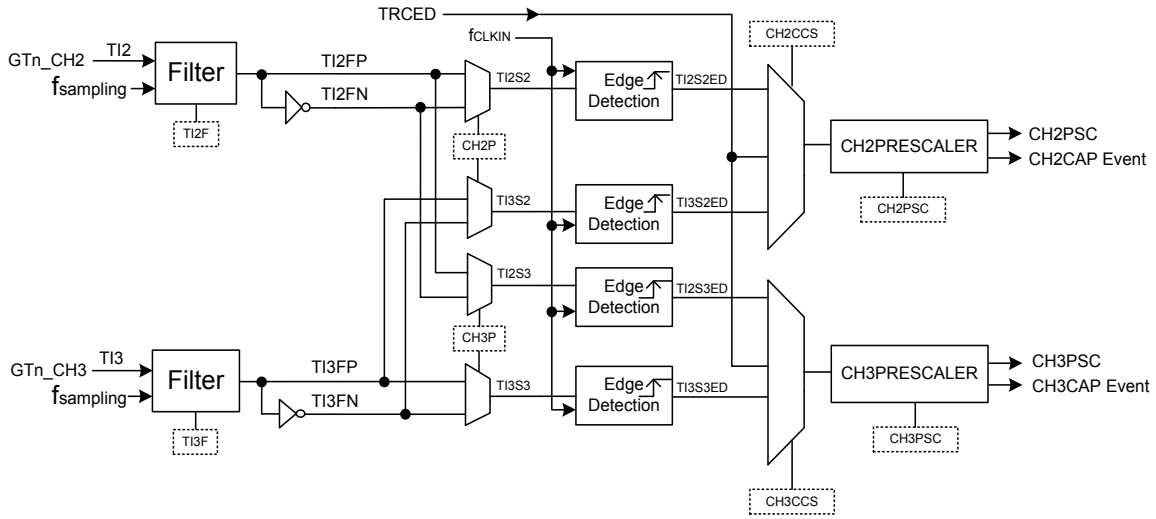


Figure 47. Channel 2 and Channel 3 Input Stage

Output Stage

The GPTM has four channels for compare match, single pulse or PWM output function. The channel output GTn_CHx is controlled by the REFxCE, CHxOM, CHxP and CHxE bits in the corresponding CHxOCFR, CHPOLR and CHCTR registers.

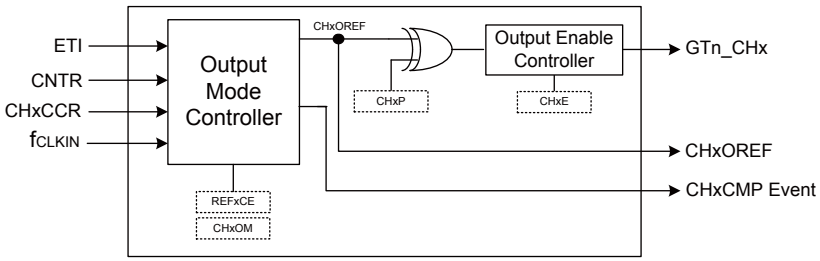


Figure 48. Output Stage Block Diagram

Channel Output Reference Signal

When the GPTM is used in the compare match output mode, the CHxOREF signal (Channel x Output Reference signal) is defined by setting the CHxOM bits. The CHxOREF signal has several types of output function. These include, keeping the original level by setting the CHxOM field to 0x00, set to 0 by setting the CHxOM field to 0x01, set to 1 by setting the CHxOM field to 0x02 or signal toggle by setting the CHxOM field to 0x03 when the counter value matches the content of the CHxCCR register.

The PWM mode 1 and PWM mode 2 outputs are also another kind of CHxOREF output which is setup by setting the CHxOM field to 0x06/0x07. In these modes, the CHxOREF signal level is changed according to the counting direction and the relationship between the counter value and the CHxCCR content. With regard to a more detailed description refer to the relative bits definition.

Another special function of the CHxOREF signal is a forced output which can be achieved by setting the CHxOM field to 0x04/0x05. Here the output can be forced to an inactive/active level irrespective of the comparison condition between the counter and the CHxCCR values.

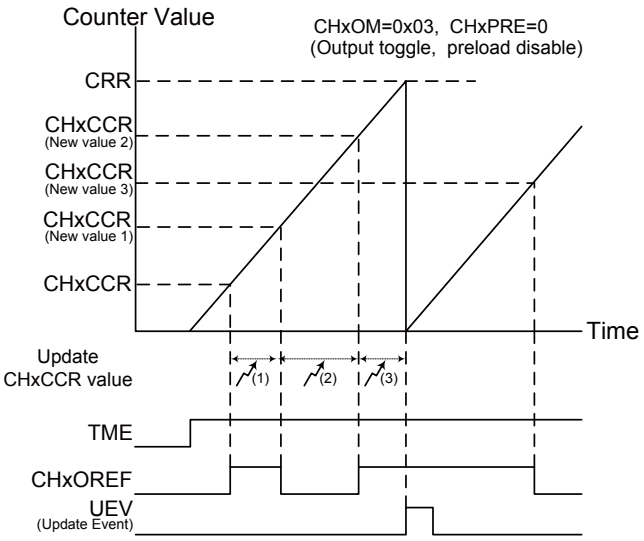


Figure 49. Toggle Mode Channel Output Reference Signal (CHxPRE=0)

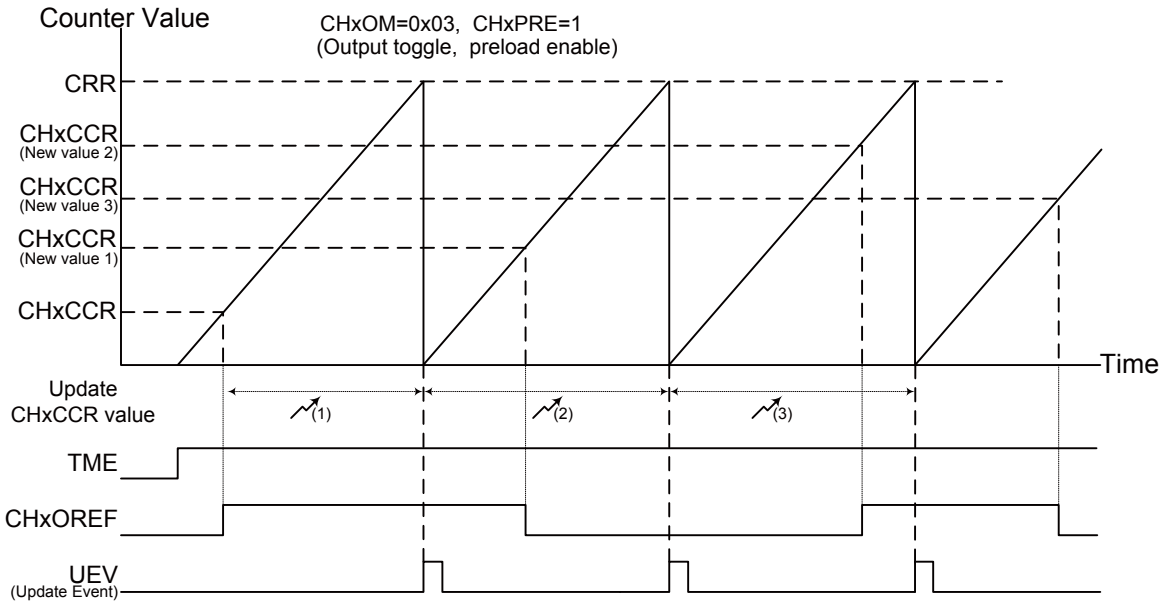


Figure 50. Toggle Mode Channel Output Reference Signal (CHxPRE=1)

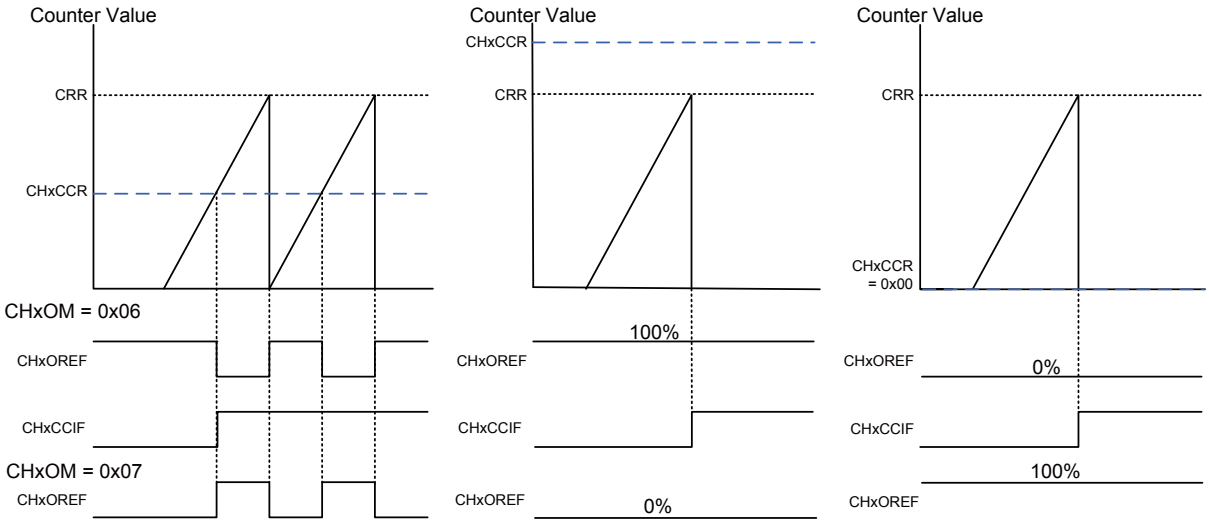


Figure 51. PWM Mode Channel Output Reference Signal and Counter in Up-counting Mode

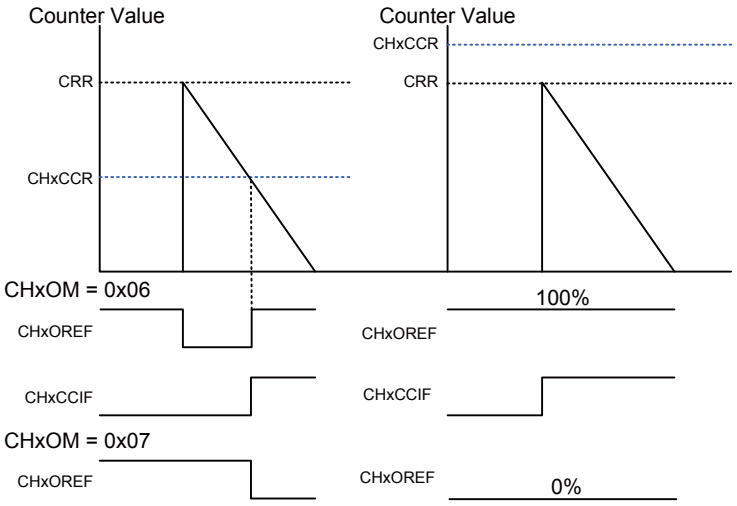


Figure 52. PWM Mode Channel Output Reference Signal and Counter in Down-counting Mode

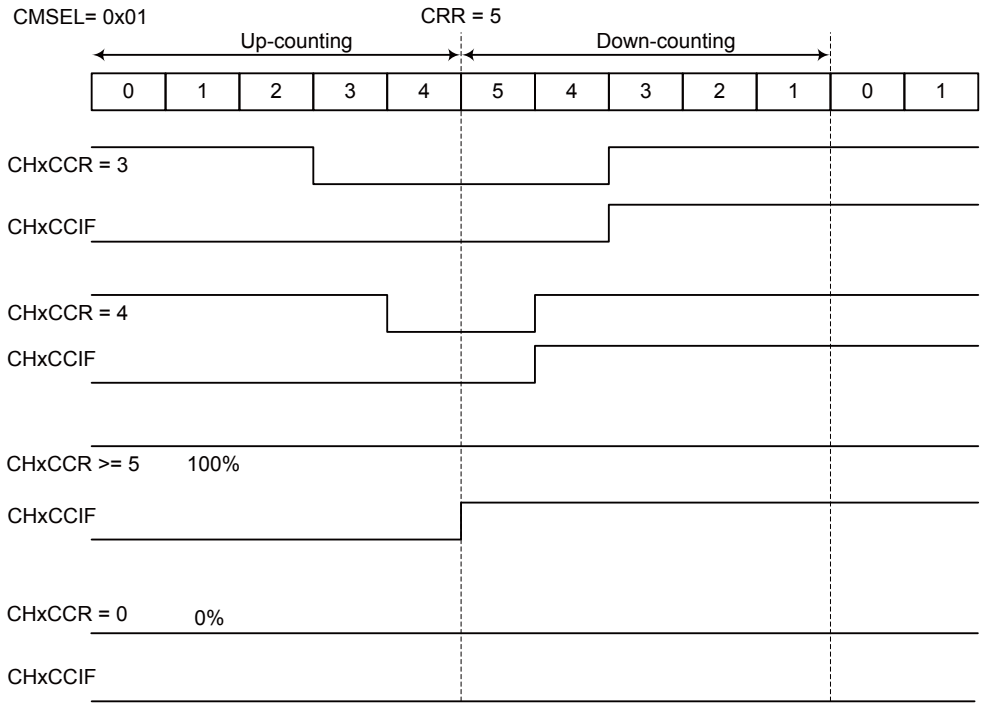


Figure 53. PWM Mode 1 Channel Output Reference Signal and Counter in Center-aligned Counting Mode

Update Management

The Update event is used to update the CRR, the PSCR and the CHxCCR values from the actual registers to the corresponding shadow registers. An update event occurs when the counter overflows or underflows, the UEVG bit is set or the slave restart mode is triggered.

The UEVDIS bit in the CNTCFR register can determine whether the update event occurs or not. When the update event occurs, the corresponding update event interrupt will be generated depending upon whether the update event interrupt generation function is enabled or not by configuring the UGDIS bit in the CNTCFR register. For more detail description, refer to the UEVDIS and UGDIS bit definition in the CNTCFR register.

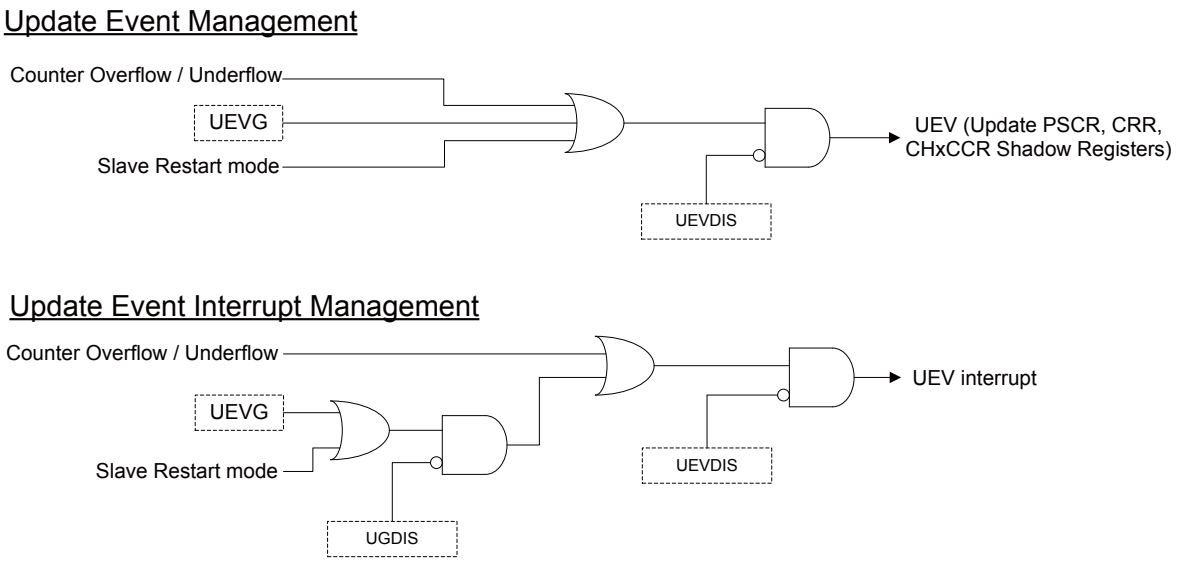


Figure 54. Update Event Setting Diagram

Quadrature Decoder

The Quadrature Decoder function uses two quadrantal inputs TI0 and TI1 derived from the GTn_CH0 and GTn_CH1 pins respectively to interact to generate the counter value. The DIR bit is modified by hardware automatically during each input source transition. The counter is countering on TI0 edges only, TI1 edges only or both TI0 and TI1 edges. The selection is made by setting the SMSEL field to 0x01, 0x02 or 0x03. The mechanism for changing the counter direction is shown in the following table. The Quadrature decoder can be regarded as an external clock with a directional selection. This means that the counter counts continuously in the interval between 0 and the counter-reload value. Therefore, users must configure the CRR register before the counter starts to count.

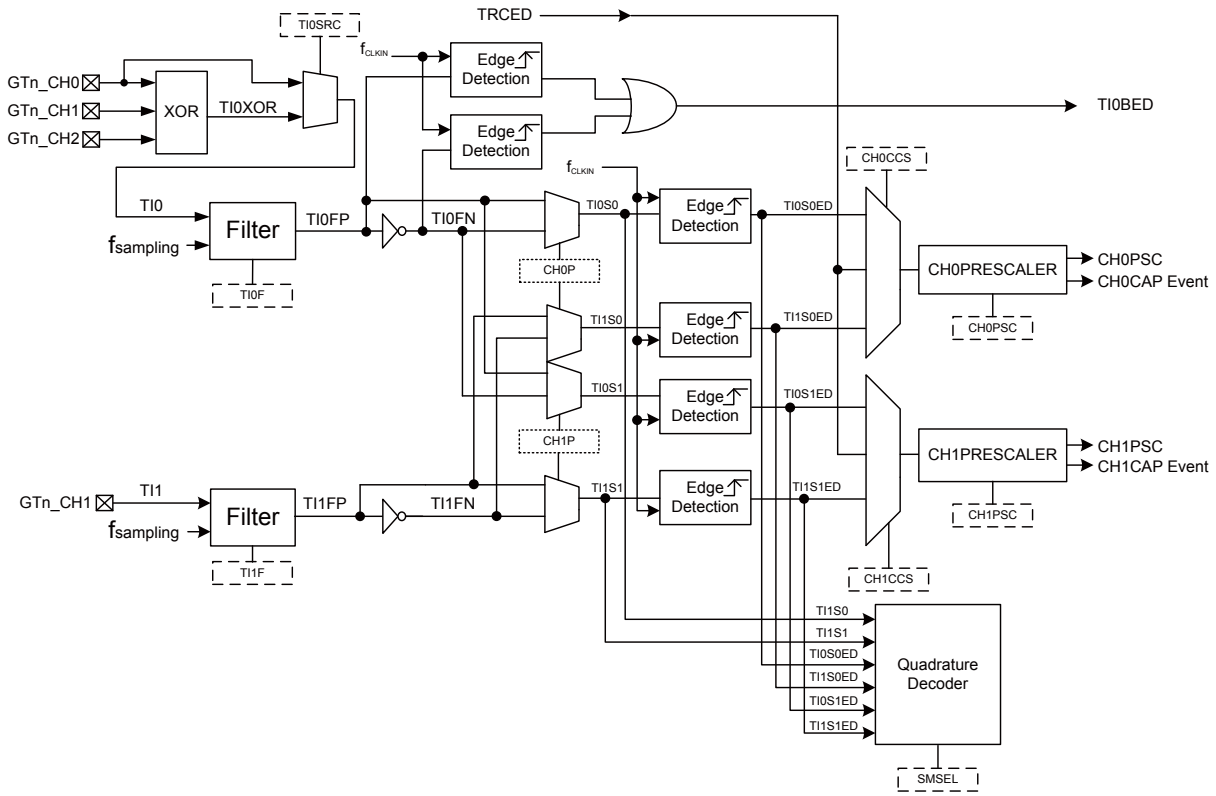


Figure 55. Input Stage and Quadrature Decoder Block Diagram

Table 29. Counting Direction and Encoding Signals

Counting mode	Level	TI0S0		TI1S1	
		Rising	Falling	Rising	Falling
Counting on TI0 only (SMSEL=0x01)	TI1S1=High	Down	Up	—	—
	TI1S1=Low	Up	Down	—	—
Counting on TI1 only (SMSEL=0x02)	TI0S0=High	—	—	Up	Down
	TI0S0=Low	—	—	Down	Up
Counting on TI0 and TI1 (SMSEL=0x03)	TI1S1=High	Down	Up	X	X
	TI1S1=Low	Up	Down	X	X
	TI0S0=High	X	X	Up	Down
	TI0S0=Low	X	X	Down	Up

NOTE: "—" → means "no counting"; "X" → impossible

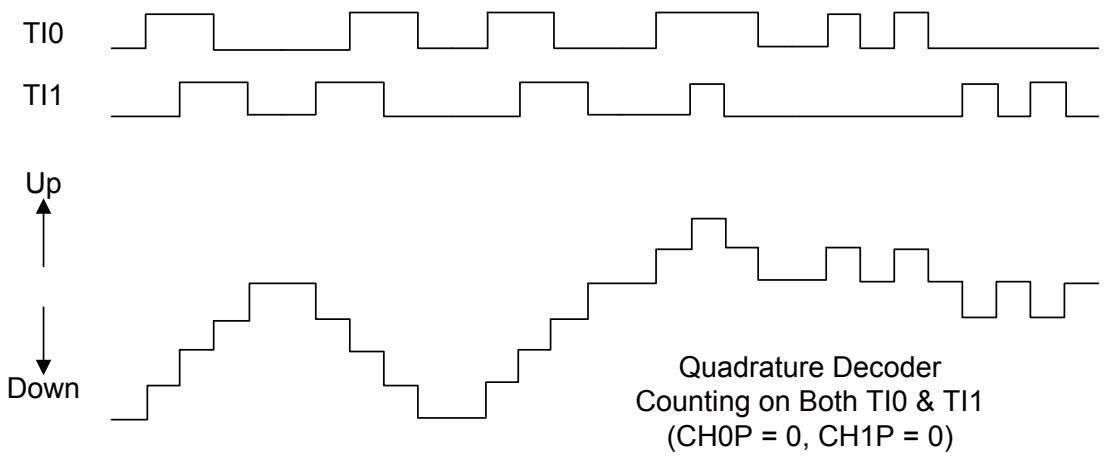


Figure 56. Both TI0 and TI1 Quadrature Decoder Counting

Digital Filter

The digital filters are embedded in the input stage and clock controller block for the GTn_CH0~GTn_CH3 and GTn_ETI pins respectively. The digital filter in the GPTM is an N-event counter where N refers to how many valid transitions are necessary to output a filtered signal. The N value can be 0, 2, 4, 5, 6 or 8 according to the user selection for each filter.

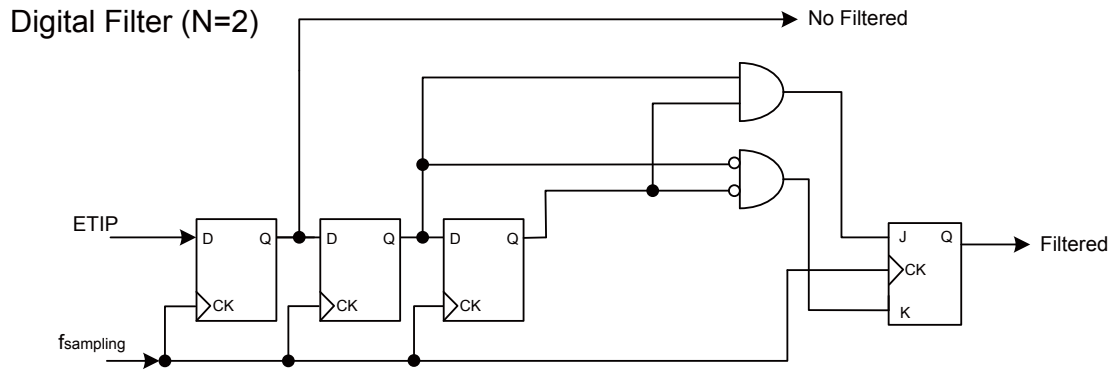


Figure 57. GTn_ETI Pin Digital Filter Diagram with N=2

Clearing CHxOREF when ETIF is high

The CHxOREF signal can be forced to 0 when the ETIF signal is set to a high level by setting the REFxCE bit to 1 in the CHxOCFR register. The CHxOREF signal will not return to its active level until the next update event occurs.

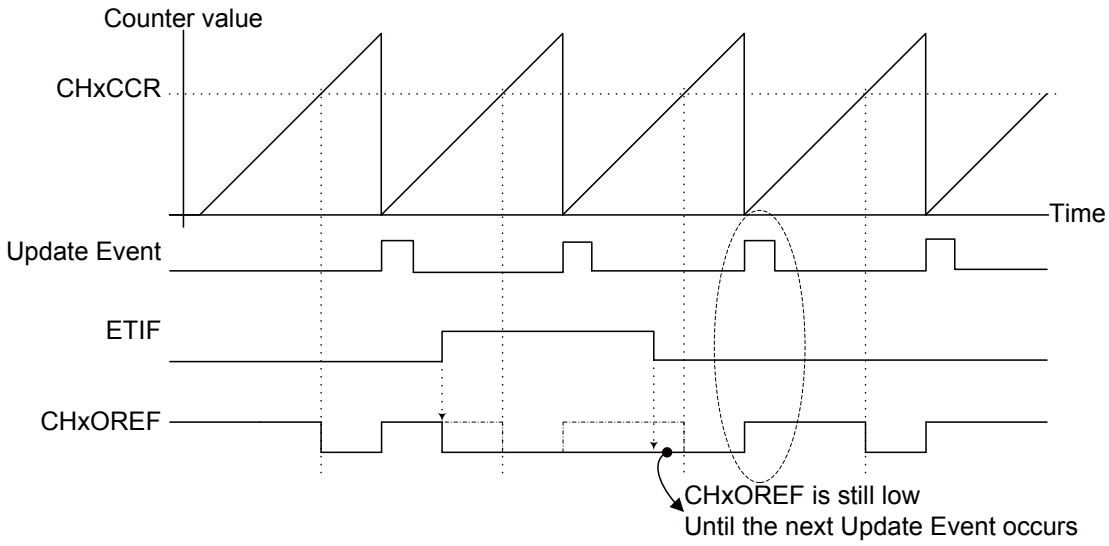


Figure 58. Clearing CHxOREF by ETIF

Single Pulse Mode

Once the timer is set to operate in the single pulse mode, it is not necessary to set the timer enable bit TME in the CTR register to 1 to enable the counter. The trigger to generate a pulse can be sourced from the STI signal rising edge or by setting the TME bit to 1 using software. Setting the TME bit to 1 or a trigger from the STI signal rising edge can generate a pulse and then keep the TME bit at a high state until the update event occurs or the TME bit is written to 0 by software. If the TME bit is cleared to 0 using software, the counter will be stopped and its value held. If the TME bit is automatically cleared to 0 by a hardware update event, the counter will be reinitialized.

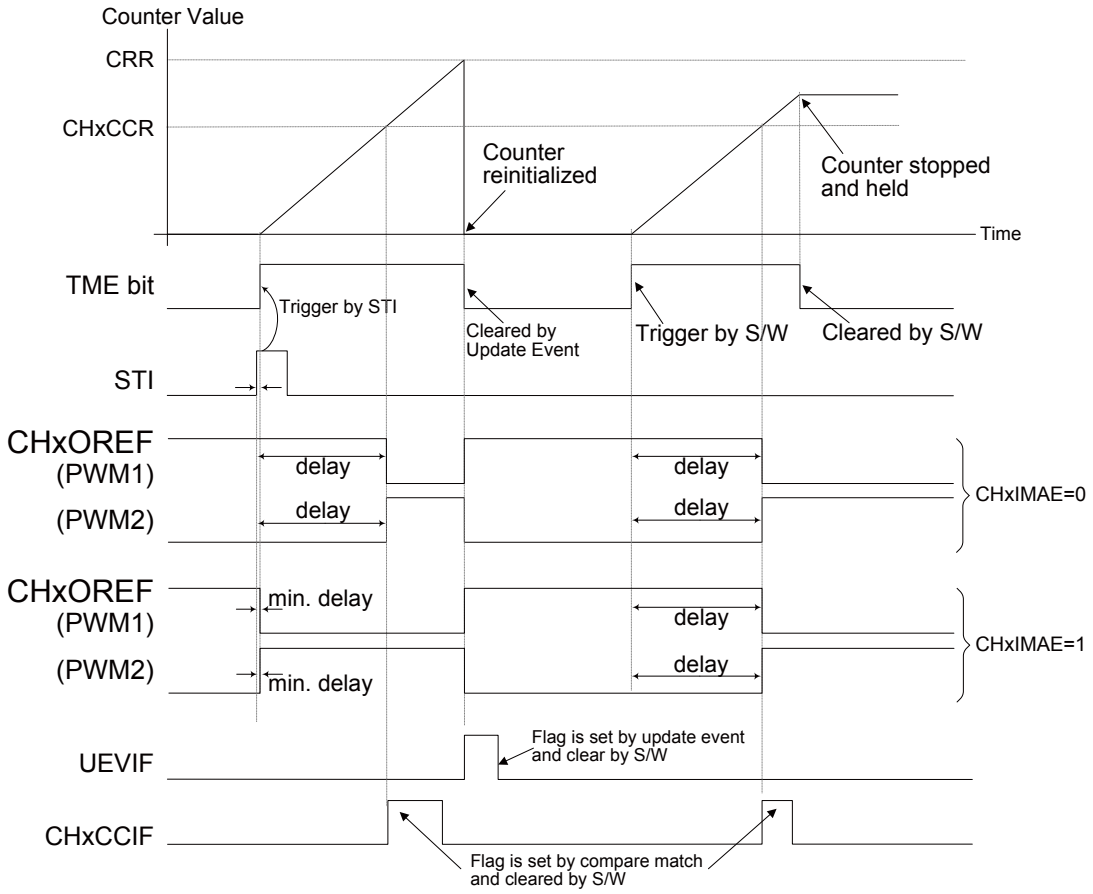


Figure 59. Single Pulse Mode

In the Single Pulse mode, the STI active edge which sets the TME bit to 1 will enable the counter. However, there exist several clock delays to perform the comparison result between the counter value and the CHxCCR value. In order to reduce the delay to a minimum value, the user can set the CHxIMAE bit in each CHxOCFR register. After a STI rising edge trigger occurs in the single pulse mode, the CHxOREF signal will immediately be forced to the state which the CHxOREF signal will change to as the compare match event occurs without taking the comparison result into account. The CHxIMAE bit is available only when the output channel is configured to operate in the PWM1 or PWM2 output mode and the trigger source is derived from the STI signal.

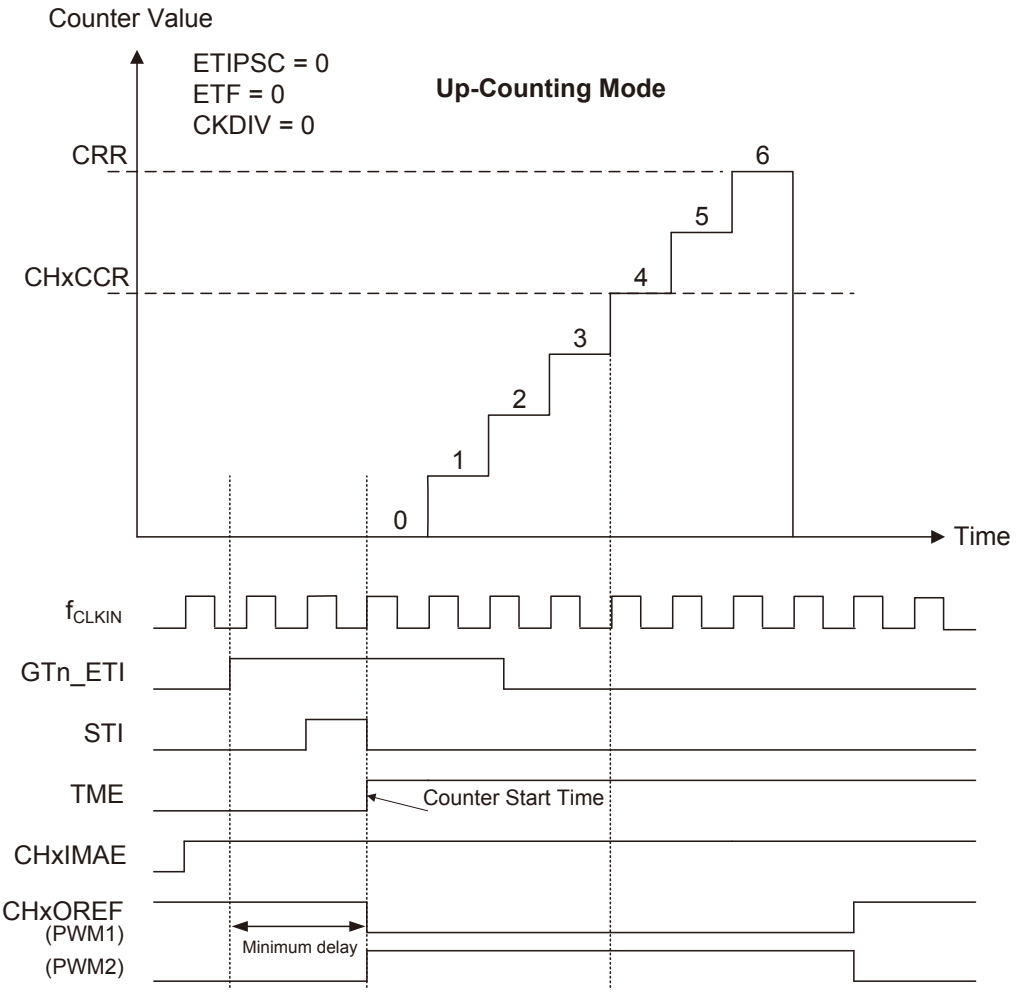


Figure 60. Immediate Active Mode Minimum Delay

Timer Interconnection

The timers can be internally connected together for timer chaining or synchronization. This can be implemented by configuring one timer to operate in the Master mode while configuring another timer to be in the Slave mode. The following figures present several examples of trigger selection for the master and slave modes.

Using one timer to trigger another timer start or stop counting

- Configure GPTM0 as the master mode to send its channel 0 Output Reference signal CH0OREF as a trigger output (MMSEL=0x04)
- Configure GPTM0 CH0OREF waveform
- Configure GPTM1 to receive its input trigger source from the GPTM0 trigger output (TRSEL=0x09)
- Configure GPTM1 to operate in the pause mode (SMSEL=0x05)
- Enable GPTM1 by writing 1 to the TME bit
- Enable GPTM0 by writing 1 to the TME bit

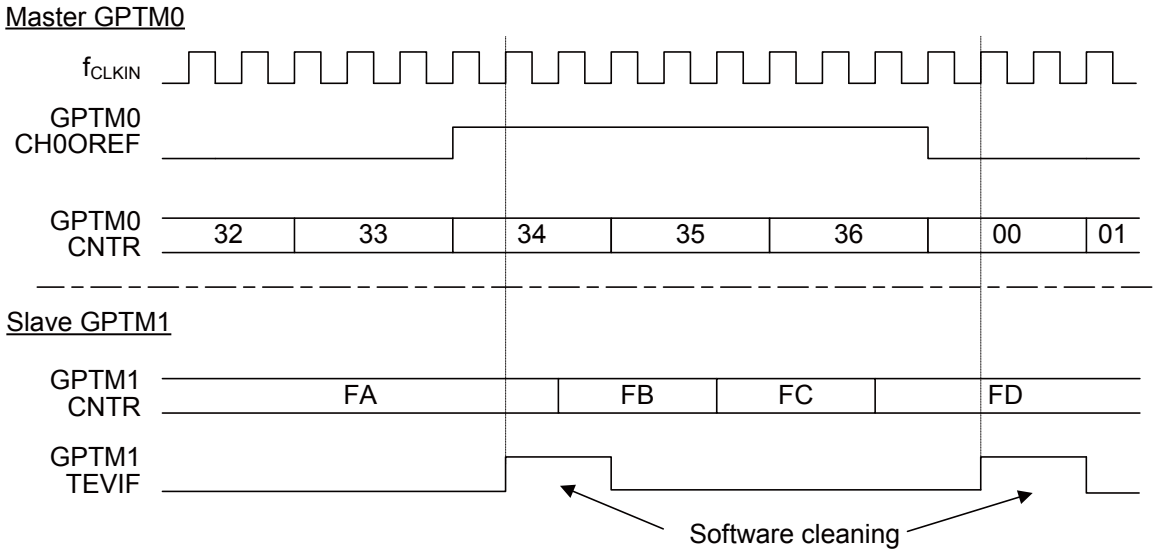


Figure 61. Pausing GPTM1 using the GPTM0 CH0OREF Signal

Using one timer to trigger another timer start counting

- Configure GPTM0 to operate in the master mode to send its Update Event UEV as the trigger output (MMSEL=0x02)
- Configure the GPTM0 period by setting the CHxCRR register
- Configure GPTM1 to get the input trigger source from the GPTM0 trigger output (TRSEL=0x09)
- Configure GPTM1 to be in the slave trigger mode (SMSEL=0x06)
- Start GPTM0 by writing 1 to the TME bit

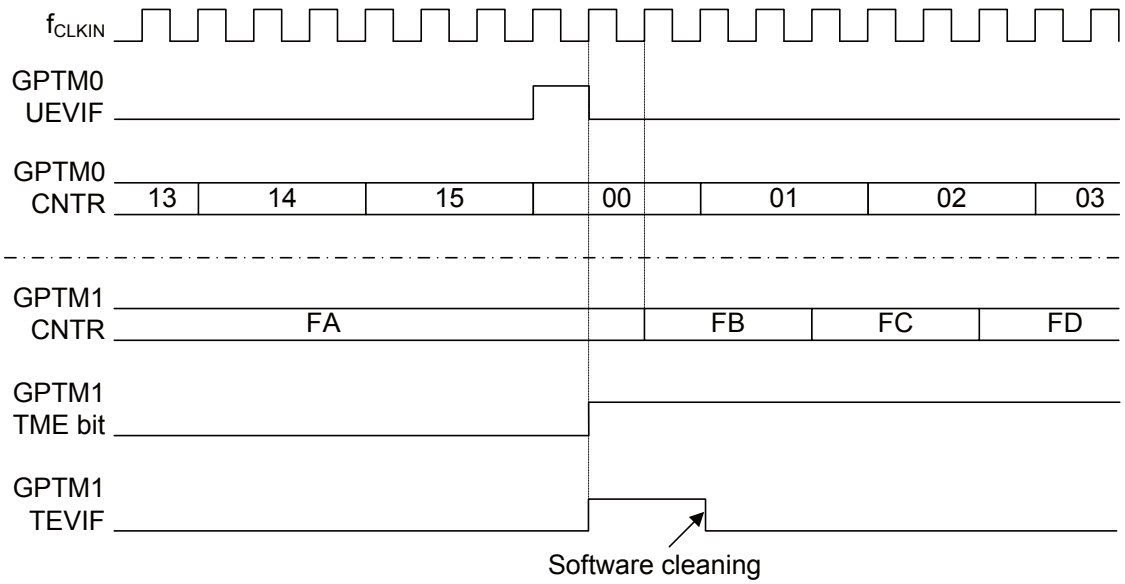


Figure 62. Triggering GPTM1 with GPTM0 Update Event

Starting two timers synchronously in response to an external trigger

- Configure GPTM0 to operate in the master mode to send its enable signal as a trigger output (MMSEL=0x01)
- Configure GPTM0 slave mode to receive its input trigger source from GTn_CH0 pin (TRSEL=0x01)
- Configure GPTM0 to be in the slave trigger mode (SMSEL=0x06)
- Enable the GPTM0 master timer synchronization function by setting the TSE bit in the MDCFR register to 1 to synchronize the slave timer
- Configure GPTM1 to receive its input trigger source from the GPTM0 trigger output (TRSEL=0x09)
- Configure GPTM1 to be in the slave trigger mode (SMSEL=0x06)

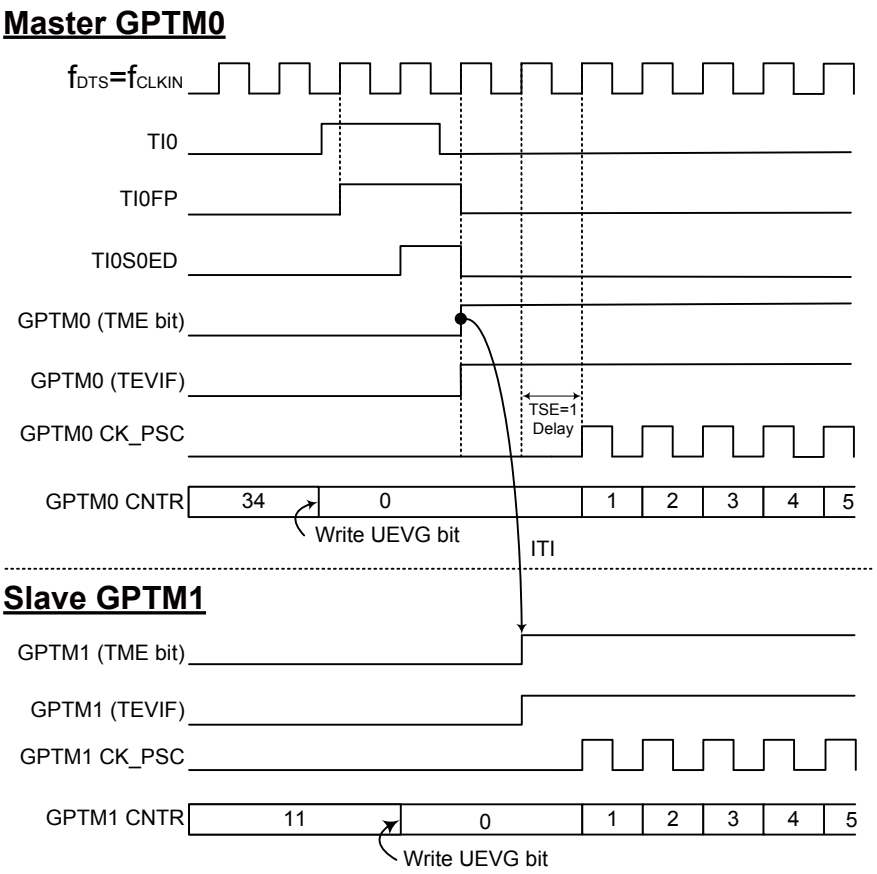


Figure 63. Trigger GPTM0 and GPTM1 with the GPTM0 CH0 Input

Trigger ADC Start

To interconnect with the Analog-to-Digital Converter, the GPTM can output the MTO signal or the channel output GTn_CHx (x=0~3) signal to be used as the Analog-to-Digital Converter input trigger signal.

PDMA Request

The GPTM supports the interface for PDMA data transfer. There are certain events which can generate the PDMA requests if the corresponding enable control bits are set to 1 to enable the PDMA access. These events are the GPTM update events, trigger events and channel capture/compare events. When the PDMA request is generated from the GPTM channel, it can be derived from the channel capture/compare event or the GPTM update event selected by the channel PDMA selection bit, CHCCDS, for all channels. For more detailed PDMA configuring information, refer to the corresponding section in the PDMA chapter.

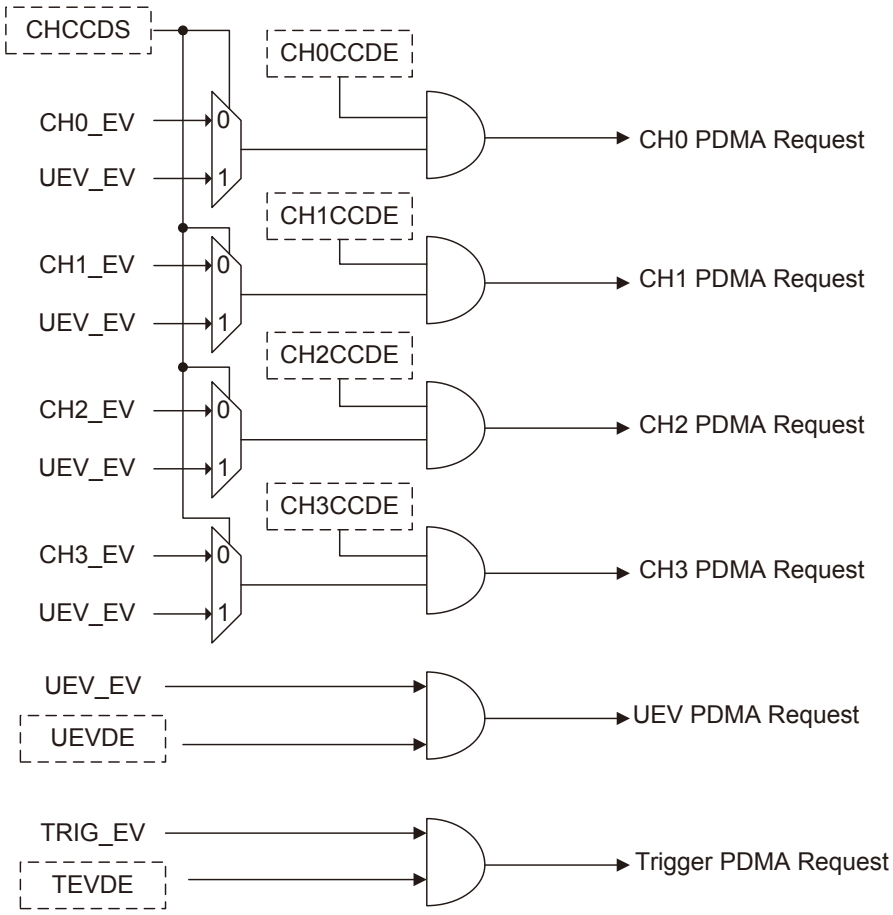


Figure 64. GPTM PDMA Mapping Diagram

Register Map

The following table shows the GPTM registers and reset values.

Table 30. GPTM Register Map

Register	Offset	Description	Reset Value
GPTMn Base Address=0x4006_E000 (0); 0x4006_F000 (1)			
CNTCFR	0x000	Timer Counter Configuration Register	0x0000_0000
MDCFR	0x004	Timer Mode Configuration Register	0x0000_0000
TRCFR	0x008	Timer Trigger Configuration Register	0x0000_0000
CTR	0x010	Timer Control Register	0x0000_0000
CH0ICFR	0x020	Channel 0 Input Configuration Register	0x0000_0000
CH1ICFR	0x024	Channel 1 Input Configuration Register	0x0000_0000
CH2ICFR	0x028	Channel 2 Input Configuration Register	0x0000_0000
CH3ICFR	0x02C	Channel 3 Input Configuration Register	0x0000_0000
CH0OCFR	0x040	Channel 0 Output Configuration Register	0x0000_0000
CH1OCFR	0x044	Channel 1 Output Configuration Register	0x0000_0000
CH2OCFR	0x048	Channel 2 Output Configuration Register	0x0000_0000
CH3OCFR	0x04C	Channel 3 Output Configuration Register	0x0000_0000
CHCTR	0x050	Channel Control Register	0x0000_0000
CHPOLR	0x054	Channel Polarity Configuration Register	0x0000_0000
DICTR	0x074	Timer PDMA/Interrupt Control Register	0x0000_0000
EVGR	0x078	Timer Event Generator Register	0x0000_0000
INTSR	0x07C	Timer Interrupt Status Register	0x0000_0000
CNTR	0x080	Timer Counter Register	0x0000_0000
PSCR	0x084	Timer Prescaler Register	0x0000_0000
CRR	0x088	Timer Counter Reload Register	0x0000_FFFF
CH0CCR	0x090	Channel 0 Capture/Compare Register	0x0000_0000
CH1CCR	0x094	Channel 1 Capture/Compare Register	0x0000_0000
CH2CCR	0x098	Channel 2 Capture/Compare Register	0x0000_0000
CH3CCR	0x09C	Channel 3 Capture/Compare Register	0x0000_0000

Register Descriptions

Timer Counter Configuration Register – CNTCFR

This register specifies the GPTM counter configuration.

Offset: 0x000

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							DIR
Type/Reset								RW 0
	23	22	21	20	19	18	17	16
	Reserved							CMSEL
Type/Reset							RW 0	RW 0
	15	14	13	12	11	10	9	8
	Reserved							CKDIV
Type/Reset							RW 0	RW 0
	7	6	5	4	3	2	1	0
	Reserved						UGDIS	UEVDIS
Type/Reset							RW 0	RW 0

Bits	Field	Descriptions
[24]	DIR	Counting Direction 0: Up-counting 1: Down-counting **Note:** This bit is read only when the Timer is configured to be in the Center-aligned counting mode or when used as a Quadrature decoder.
[17:16]	CMSEL	Counter Mode Selection 00: Edge-aligned counting mode. Normal up-counting and down-counting available for this mode. Counting direction is defined by the DIR bit. 01: Center-aligned counting mode 1. The counter counts up and down alternatively. The compare match interrupt flag is set during the down-counting period. 10: Center-aligned counting mode 2. The counter counts up and down alternatively. The compare match interrupt flag is set during the up-counting period. 11: Center-aligned counting mode 3. The counter counts up and down alternatively. The compare match interrupt flag is set during the up-counting or down-counting period.
[9:8]	CKDIV	Clock Division These two bits define the frequency ratio between the timer clock (f_{CLKIN}) and the dead-time clock (f_{DTS}). The dead-time clock is also used for digital filter sampling clock. 00: $f_{DTS}=f_{CLKIN}$ 01: $f_{DTS}=f_{CLKIN}/2$ 10: $f_{DTS}=f_{CLKIN}/4$ 11: Reserved

Bits	Field	Descriptions
[1]	UGDIS	Update event interrupt generation disable control 0: Any of the following events will generate an update PDMA request or interrupt – Counter overflow/underflow – Setting the UEVG bit – Update generation through the slave mode 1: Only counter overflow/underflow generates an update PDMA request or interrupt
[0]	UEVDIS	Update event Disable control 0: Enable the update event request by one of following events – Counter overflow/underflow – Setting the UEVG bit – Update generation through the slave mode 1: Disable the update event (However the counter and the prescaler are reinitialized if the UEVG bit is set or if a hardware restart is received from the slave mode)

Timer Mode Configuration Register – MDCFR

This register specifies the GPTM master and slave mode selection and single pulse mode.

Offset: 0x004

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							SPMSET
Type/Reset								RW 0
	23	22	21	20	19	18	17	16
	Reserved					MMSEL		
Type/Reset						RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
	Reserved					SMSEL		
Type/Reset						RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	Reserved							TSE
Type/Reset								RW 0

Bits	Field	Descriptions
[24]	SPMSET	Single Pulse Mode Setting 0: Counter counts normally irrespective of whether the update event occurred or not 1: Counter stops counting at the next update event and then the TME bit is cleared by hardware

Bits	Field	Descriptions
[18:16]	MMSEL	Master Mode Selection Master mode selection is used to select the MTO signal source which is used to synchronize the other slave timer.

MMSEL [2:0]	Mode	Descriptions
000	Reset Mode	The MTO in the Reset mode is an output derived from one of the following cases: 1. Software setting UEVG bit 2. Slave has trigger input when used in slave restart mode
001	Enable Mode	The Counter Enable signal is used as the trigger output.
010	Update Mode	The update event is used as the trigger output according to one of the following cases when the UEVDIS bit is cleared to 0: 1. Counter overflow/underflow 2. Software setting UEVG 3. Slave has trigger input when used in slave Restart mode
011	Capture/Compare Mode	When a Channel 0 capture or compare match event occurs, it will generate a positive pulse used as the master trigger output.
100	Compare output 0	The Channel 0 Output reference signal named CH0OREF is used as the trigger output.
101	Compare output 1	The Channel 1 Output reference signal named CH1OREF is used as the trigger output.
110	Compare output 2	The Channel 2 Output reference signal named CH2OREF is used as the trigger output.
111	Compare output 3	The Channel 3 Output reference signal named CH3OREF is used as the trigger output.

Bits	Field	Descriptions

[10:8] SMSEL Slave Mode Selection

SMSEL [2:0]	Mode	Descriptions
000	Disable mode	The prescaler is clocked directly by the internal clock.
001	Quadrature Decoder mode 1	The counter uses the clock pulse generated from the interact between the TI0 and TI1 signals to drive the counter prescaler. A transition of the TI0 edge is used in this mode depending upon the TI1 level.
010	Quadrature Decoder mode 2	The counter uses the clock pulse generated from the interaction between the TI0 and TI1 signals to drive the counter prescaler. A transition of the TI1 edge is used in this mode depending upon the TI0 level.
011	Quadrature Decoder mode 3	The counter uses the clock pulse generated from the interaction between the TI0 and TI1 signals to drive the counter prescaler. A transition of one channel edge is used in the quadrature decoder mode 3 depending upon the other channel level.
100	Restart Mode	The counter value restarts from 0 or the CRR shadow register value depending upon the counting direction mode on the rising edge of the STI signal. The registers will also be updated.
101	Pause Mode	The counter starts to count when the selected trigger input STI is high. The counter stops counting on the instant, not being reset, when the STI signal changes its state to a low level. Both the counter start and stop control are determined by the STI signal.
110	Trigger Mode	The counter starts to count from the original value in the counter on the rising edge of the selected trigger input STI. Only the counter start control is determined by the STI signal.
111	STIED	The rising edge of the selected trigger signal STI will clock the counter.

[0] TSE Timer Synchronization Enable
0: No action
1: Master timer (current timer) will generate a delay to synchronize its slave timer through the MTO signal

Timer Trigger Configuration Register – TRCFR

This register specifies the GPTM external clock setting and the trigger source selection.

Offset: 0x008

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							ECME
Type/Reset								RW 0
	23	22	21	20	19	18	17	16
	Reserved							ETIPOL
Type/Reset								RW 0
	15	14	13	12	11	10	9	8
	Reserved			ETIPSC			ETF	
Type/Reset			RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	Reserved						TRSEL	
Type/Reset					RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[24]	ECME	External Clock Mode Enable 0: External clock mode is disabled 1: External clock mode is enabled The following two settings have the same effect: 1. Setting the ECME bit to 1 2. Setting SMSEL=0x111 with STI connected to ETIF (TRSEL=0x011)
[16]	ETIPOL	External Trigger Polarity 0: GTn_ETI active at high level or rising edge 1: GTn_ETI active at low level or falling edge
[13:12]	ETIPSC	External Trigger Prescaler A prescaler can be enabled to reduce the ETIP frequency. 00: Prescaler OFF 01: ETIP frequency divided by 2 10: ETIP frequency divided by 4 11: ETIP frequency divided by 8

Bits	Field	Descriptions
[11:8]	ETF	External Trigger Filter These bits define the frequency divided ratio that is used to sample the GTn_ETI signal. The digital filter in the GPTM is a N-event counter where N means how many valid transitions are necessary to output a filtered signal. 0000: No filter, the sampling clock is f_{DTS} 0001: $f_{SAMPLING}=f_{CLKIN}$, N=2 0010: $f_{SAMPLING}=f_{CLKIN}$, N=4 0011: $f_{SAMPLING}=f_{CLKIN}$, N=8 0100: $f_{SAMPLING}=f_{DTS}/2$, N=6 0101: $f_{SAMPLING}=f_{DTS}/2$, N=8 0110: $f_{SAMPLING}=f_{DTS}/4$, N=6 0111: $f_{SAMPLING}=f_{DTS}/4$, N=8 1000: $f_{SAMPLING}=f_{DTS}/8$, N=6 1001: $f_{SAMPLING}=f_{DTS}/8$, N=8 1010: $f_{SAMPLING}=f_{DTS}/16$, N=5 1011: $f_{SAMPLING}=f_{DTS}/16$, N=6 1100: $f_{SAMPLING}=f_{DTS}/16$, N=8 1101: $f_{SAMPLING}=f_{DTS}/32$, N=5 1110: $f_{SAMPLING}=f_{DTS}/32$, N=6 1111: $f_{SAMPLING}=f_{DTS}/32$, N=8
[3:0]	TRSEL	Trigger Source Selection These bits are used to select the trigger input (STI) for counter synchronizing. 0000: Software Trigger by setting the UEVG bit 0001: Filtered input of channel 0 (TI0S0) 0010: Filtered input of channel 1 (TI1S1) 0011: External Trigger input (ETIF) 1000: Channel 0 Edge Detector (TI0BED) 1001: Internal Timing Module Trigger 0 (ITI0) 1010: Internal Timing Module Trigger 1 (ITI1) 1011: Internal Timing Module Trigger 2 (ITI2) Others: Default 0 **Note:** These bits must be updated only when they are not in use, i.e. the slave mode is disabled by setting the SMSEL field to 0x00.

Table 31. GPTM Internal Trigger Connection

Slave Timing Module	ITI0	ITI1	ITI2
GPTM0	GPTM1	MCTM0	Reserved
GPTM1	GPTM0	MCTM0	Reserved

Timer Counter Register – CTR

This register specifies the timer enable bit (TME), CRR buffer enable bit (CRBE) and Channel PDMA selection bit (CHCCDS).

Offset: 0x010

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							CHCCDS
Type/Reset								RW 0
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved						CRBE	TME
Type/Reset							RW 0	RW 0

Bits	Field	Descriptions
[16]	CHCCDS	Channel PDMA event selection 0: Channel PDMA request derived from the channel capture/compare event 1: Channel PDMA request derived from the Update event
[1]	CRBE	Counter-Reload register Buffer Enable 0: Counter reload register can be updated immediately 1: Counter reload register can not be updated until the update event occurs
[0]	TME	Timer Enable bit 0: GPTM off 1: GPTM on – GPTM functions normally When the TME bit is cleared to 0, the counter is stopped and the GPTM consumes no power in any operation mode except for the single pulse mode and the slave trigger mode. In these two modes the TME bit can automatically be set to 1 by hardware which permits all the GPTM registers to function normally.

Channel 0 Input Configuration Register – CH0ICFR

This register specifies the channel 0 input mode configuration.

Offset: 0x020

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	TI0SRC	Reserved						
Type/Reset	RW 0							
	23	22	21	20	19	18	17	16
	Reserved				CH0PSC		CH0CCS	
Type/Reset					RW 0	RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved				TI0F			
Type/Reset					RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[31]	TI0SRC	Channel 0 Input Source TI0 Selection 0: The GTn_CH0 pin is connected to channel 0 input TI0 1: The XOR operation output of the GTn_CH0, GTn_CH1, and GTn_CH2 pins are connected to the channel 0 input TI0
[19:18]	CH0PSC	Channel 0 Capture Input Source Prescaler Setting These bits define the effective events of the channel 0 capture input. Note that the prescaler is reset once the Channel 0 Capture/Compare Enable bit, CH0E, in the Channel Control register named CHCTR is cleared to 0. 00: No prescaler, channel 0 capture input signal is chosen for each active event 01: Channel 0 Capture input signal is chosen for every 2 events 10: Channel 0 Capture input signal is chosen for every 4 events 11: Channel 0 Capture input signal is chosen for every 8 events
[17:16]	CH0CCS	Channel 0 Capture/Compare Selection 00: Channel 0 is configured as an output 01: Channel 0 is configured as an input derived from the TI0 signal 10: Channel 0 is configured as an input derived from the TI1 signal 11: Channel 0 is configured as an input which comes from the TRCED signal derived from the Trigger Controller **Note:** The CH0CCS field can be accessed only when the CH0E bit is cleared to 0.

Bits	Field	Descriptions
[3:0]	TI0F	Channel 0 Input Source TI0 Filter Setting These bits define the frequency divided ratio used to sample the TI0 signal. The Digital filter in the GPTM is an N-event counter where N is defined as how many valid transitions are necessary to output a filtered signal. 0000: No filter, the sampling clock is f_{DTS} 0001: $f_{SAMPLING}=f_{CLKIN}$, N=2 0010: $f_{SAMPLING}=f_{CLKIN}$, N=4 0011: $f_{SAMPLING}=f_{CLKIN}$, N=8 0100: $f_{SAMPLING}=f_{DTS}/2$, N=6 0101: $f_{SAMPLING}=f_{DTS}/2$, N=8 0110: $f_{SAMPLING}=f_{DTS}/4$, N=6 0111: $f_{SAMPLING}=f_{DTS}/4$, N=8 1000: $f_{SAMPLING}=f_{DTS}/8$, N=6 1001: $f_{SAMPLING}=f_{DTS}/8$, N=8 1010: $f_{SAMPLING}=f_{DTS}/16$, N=5 1011: $f_{SAMPLING}=f_{DTS}/16$, N=6 1100: $f_{SAMPLING}=f_{DTS}/16$, N=8 1101: $f_{SAMPLING}=f_{DTS}/32$, N=5 1110: $f_{SAMPLING}=f_{DTS}/32$, N=6 1111: $f_{SAMPLING}=f_{DTS}/32$, N=8

Channel 1 Input Configuration Register – CH1ICFR

This register specifies the channel 1 input mode configuration.

Offset: 0x024

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved					CH1PSC		CH1CCS
Type/Reset					RW 0	RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved				TI1F			
Type/Reset					RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[19:18]	CH1PSC	Channel 1 Capture Input Source Prescaler Setting These bits define the effective events of the channel 1 capture input. Note that the prescaler is reset once the Channel 1 Capture/Compare Enable bit, CH1E, in the Channel Control register named CHCTR is cleared to 0. 00: No prescaler, channel 1 capture input signal is chosen for each active event 01: Channel 1 Capture input signal is chosen for every 2 events 10: Channel 1 Capture input signal is chosen for every 4 events 11: Channel 1 Capture input signal is chosen for every 8 events
[17:16]	CH1CCS	Channel 1 Capture/Compare Selection 00: Channel 1 is configured as an output 01: Channel 1 is configured as an input derived from the TI1 signal 10: Channel 1 is configured as an input derived from the TI0 signal 11: Channel 1 is configured as an input which comes from the TRCED signal derived from the Trigger Controller **Note:** The CH1CCS field can be accessed only when the CH1E bit is cleared to 0.

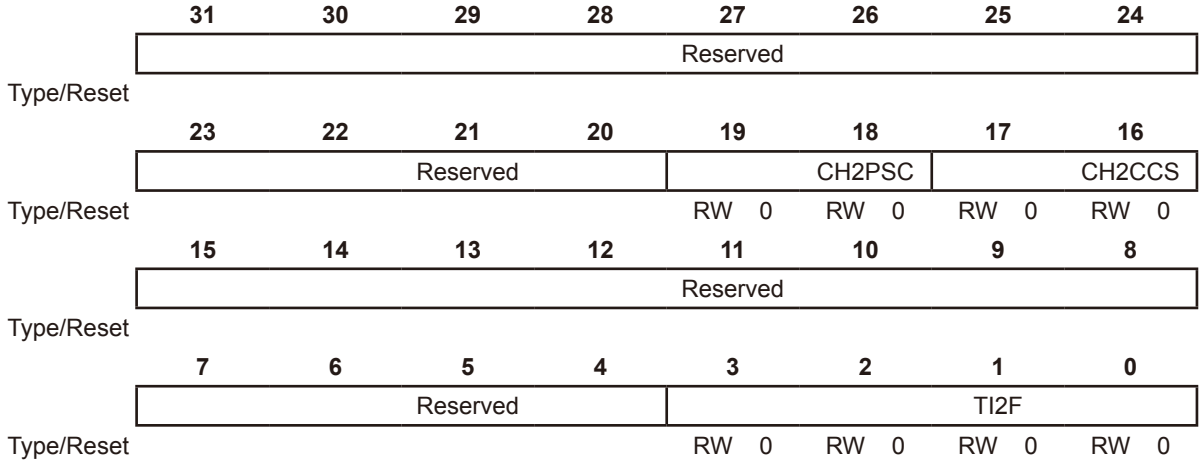
Bits	Field	Descriptions
[3:0]	TI1F	Channel 1 Input Source TI1 Filter Setting These bits define the frequency divided ratio used to sample the TI1 signal. The Digital filter in the GPTM is an N-event counter where N is defined as how many valid transitions are necessary to output a filtered signal. 0000: No filter, the sampling clock is f_{DTS} 0001: $f_{SAMPLING}=f_{CLKIN}$, N=2 0010: $f_{SAMPLING}=f_{CLKIN}$, N=4 0011: $f_{SAMPLING}=f_{CLKIN}$, N=8 0100: $f_{SAMPLING}=f_{DTS}/2$, N=6 0101: $f_{SAMPLING}=f_{DTS}/2$, N=8 0110: $f_{SAMPLING}=f_{DTS}/4$, N=6 0111: $f_{SAMPLING}=f_{DTS}/4$, N=8 1000: $f_{SAMPLING}=f_{DTS}/8$, N=6 1001: $f_{SAMPLING}=f_{DTS}/8$, N=8 1010: $f_{SAMPLING}=f_{DTS}/16$, N=5 1011: $f_{SAMPLING}=f_{DTS}/16$, N=6 1100: $f_{SAMPLING}=f_{DTS}/16$, N=8 1101: $f_{SAMPLING}=f_{DTS}/32$, N=5 1110: $f_{SAMPLING}=f_{DTS}/32$, N=6 1111: $f_{SAMPLING}=f_{DTS}/32$, N=8

Channel 2 Input Configuration Register – CH2ICFR

This register specifies the channel 2 input mode configuration.

Offset: 0x028

Reset value: 0x0000_0000



Bits	Field	Descriptions
[19:18]	CH2PSC	Channel 2 Capture Input Source Prescaler Setting These bits define the effective events of the channel 2 capture input. Note that the prescaler is reset once the Channel 2 Capture/Compare Enable bit, CH2E, in the Channel Control register named CHCTR is cleared to 0. 00: No prescaler, channel 2 capture input signal is chosen for each active event 01: Channel 2 Capture input signal is chosen for every 2 events 10: Channel 2 Capture input signal is chosen for every 4 events 11: Channel 2 Capture input signal is chosen for every 8 events
[17:16]	CH2CCS	Channel 2 Capture/Compare Selection 00: Channel 2 is configured as an output 01: Channel 2 is configured as an input derived from the TI2 signal 10: Channel 2 is configured as an input derived from the TI3 signal 11: Channel 2 is configured as an input which comes from the TRCED signal derived from the Trigger Controller **Note:** The CH2CCS field can be accessed only when the CH2E bit is cleared to 0.

Bits	Field	Descriptions
[3:0]	TI2F	Channel 2 Input Source TI2 Filter Setting These bits define the frequency divided ratio used to sample the TI2 signal. The Digital filter in the GPTM is an N-event counter where N is defined as how many valid transitions are necessary to output a filtered signal. 0000: No filter, the sampling clock is f_{DTS} 0001: $f_{SAMPLING}=f_{CLKIN}$, N=2 0010: $f_{SAMPLING}=f_{CLKIN}$, N=4 0011: $f_{SAMPLING}=f_{CLKIN}$, N=8 0100: $f_{SAMPLING}=f_{DTS}/2$, N=6 0101: $f_{SAMPLING}=f_{DTS}/2$, N=8 0110: $f_{SAMPLING}=f_{DTS}/4$, N=6 0111: $f_{SAMPLING}=f_{DTS}/4$, N=8 1000: $f_{SAMPLING}=f_{DTS}/8$, N=6 1001: $f_{SAMPLING}=f_{DTS}/8$, N=8 1010: $f_{SAMPLING}=f_{DTS}/16$, N=5 1011: $f_{SAMPLING}=f_{DTS}/16$, N=6 1100: $f_{SAMPLING}=f_{DTS}/16$, N=8 1101: $f_{SAMPLING}=f_{DTS}/32$, N=5 1110: $f_{SAMPLING}=f_{DTS}/32$, N=6 1111: $f_{SAMPLING}=f_{DTS}/32$, N=8

Channel 3 Input Configuration Register – CH3ICFR

This register specifies the channel 3 input mode configuration.

Offset: 0x02C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved					CH3PSC		CH3CCS
Type/Reset					RW 0	RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved				TI3F			
Type/Reset					RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[19:18]	CH3PSC	Channel 3 Capture Input Source Prescaler Setting These bits define the effective events of the channel 3 capture input. Note that the prescaler is reset once the Channel 3 Capture/Compare Enable bit, CH3E, in the Channel Control register named CHCTR is cleared to 0. 00: No prescaler, channel 3 capture input signal is chosen for each active event 01: Channel 3 Capture input signal is chosen for every 2 events 10: Channel 3 Capture input signal is chosen for every 4 events 11: Channel 3 Capture input signal is chosen for every 8 events
[17:16]	CH3CCS	Channel 3 Capture/Compare Selection 00: Channel 3 is configured as an output 01: Channel 3 is configured as an input derived from the TI3 signal 10: Channel 3 is configured as an input derived from the TI2 signal 11: Channel 3 is configured as an input which comes from the TRCED signal derived from the Trigger Controller **Note:** The CH3CCS field can be accessed only when the CH3E bit is cleared to 0.

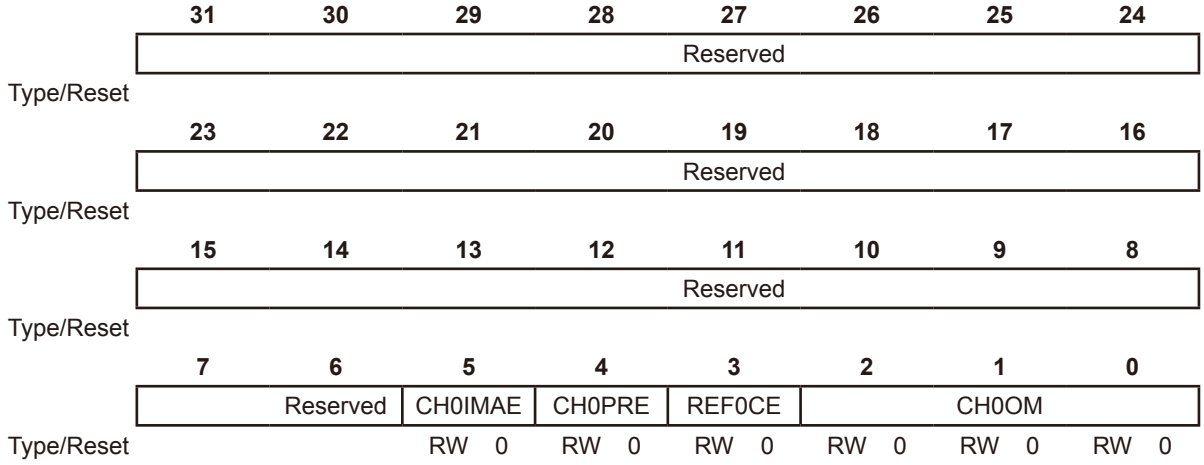
Bits	Field	Descriptions
[3:0]	TI3F	Channel 3 Input Source TI3 Filter Setting These bits define the frequency divided ratio used to sample the TI3 signal. The Digital filter in the GPTM is an N-event counter where N is defined as how many valid transitions are necessary to output a filtered signal. 0000: No filter, the sampling clock is f_{DTS} 0001: $f_{SAMPLING}=f_{CLKIN}$, N=2 0010: $f_{SAMPLING}=f_{CLKIN}$, N=4 0011: $f_{SAMPLING}=f_{CLKIN}$, N=8 0100: $f_{SAMPLING}=f_{DTS}/2$, N=6 0101: $f_{SAMPLING}=f_{DTS}/2$, N=8 0110: $f_{SAMPLING}=f_{DTS}/4$, N=6 0111: $f_{SAMPLING}=f_{DTS}/4$, N=8 1000: $f_{SAMPLING}=f_{DTS}/8$, N=6 1001: $f_{SAMPLING}=f_{DTS}/8$, N=8 1010: $f_{SAMPLING}=f_{DTS}/16$, N=5 1011: $f_{SAMPLING}=f_{DTS}/16$, N=6 1100: $f_{SAMPLING}=f_{DTS}/16$, N=8 1101: $f_{SAMPLING}=f_{DTS}/32$, N=5 1110: $f_{SAMPLING}=f_{DTS}/32$, N=6 1111: $f_{SAMPLING}=f_{DTS}/32$, N=8

Channel 0 Output Configuration Register – CH0OCFR

This register specifies the channel 0 output mode configuration.

Offset: 0x040

Reset value: 0x0000_0000



Bits	Field	Descriptions
[5]	CH0IMAE	Channel 0 Immediate Active Enable 0: No action 1: Single pulse Immediate Active Mode is enabled The CH0OREF will be forced to the compare matched level immediately after an available trigger event occurs irrespective of the result of the comparison between the CNTR and the CH0CCR values. The effective duration ends automatically at the next overflow or underflow event. **Note:** The CH0IMAE bit is available only if the channel 0 is configured to be operated in the PWM mode 1 or the PWM mode 2.
[4]	CH0PRE	Channel 0 Capture/Compare Register (CH0CCR) Preload Enable 0: CH0CCR preload function is disabled The CH0CCR register can be immediately assigned a new value when the CH0PRE bit is cleared to 0 and the updated CH0CCR value is used immediately. 1: CH0CCR preload function is enabled The new CH0CCR value will not be transferred to its shadow register until the update event occurs.
[3]	REF0CE	Channel 0 Reference Output Clear Enable 0: CH0OREF performed normally and is not affected by the ETIF signal 1: CH0OREF is forced to 0 on the high level of the ETIF signal derived from the GTn_ETI pin

Bits	Field	Descriptions
[2:0]	CH0OM	Channel 0 Output Mode Setting These bits define the functional types of the output reference signal CH0OREF. 000: No Change 001: Output 0 on compare match 010: Output 1 on compare match 011: Output toggles on compare match 100: Force inactive – CH0OREF is forced to 0 101: Force active – CH0OREF is forced to 1 110: PWM mode 1 – During up-counting, channel 0 is at the active level when CNTR<CH0CCR or else at an inactive level. – During down-counting, channel 0 at the inactive level when CNTR>CH0CCR or else at an active level. 111: PWM mode 2 – During up-counting, channel 0 is at the inactive level when CNTR<CH0CCR or else at an active level. – During down-counting, channel 0 is at the active level when CNTR>CH0CCR or else at an inactive level.

Channel 1 Output Configuration Register – CH1OCFR

This register specifies the channel 1 output mode configuration.

Offset: 0x044

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
		Reserved	CH1IMAE	CH1PRE	REF1CE	CH1OM		
Type/Reset			RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[5]	CH1IMAE	Channel 1 Immediate Active Enable 0: No action 1: Single pulse Immediate Active Mode is enabled The CH1OREF will be forced to the compare matched level immediately after an available trigger event occurs irrespective of the result of the comparison between the CNTR and the CH1CCR values. The effective duration ends automatically at the next overflow or underflow event. **Note:** The CH1IMAE bit is available only if the channel 1 is configured to be operated in the PWM mode 1 or the PWM mode 2.
[4]	CH1PRE	Channel 1 Capture/Compare Register (CH1CCR) Preload Enable 0: CH1CCR preload function is disabled The CH1CCR register can be immediately assigned a new value when the CH1PRE bit is cleared to 0 and the updated CH1CCR value is used immediately. 1: CH1CCR preload function is enabled The new CH1CCR value will not be transferred to its shadow register until the update event occurs.
[3]	REF1CE	Channel 1 Reference Output Clear Enable 0: CH1OREF performed normally and is not affected by the ETIF signal 1: CH1OREF is forced to 0 on the high level of the ETIF signal derived from the GTn_ETI pin

Bits	Field	Descriptions
[2:0]	CH1OM	Channel 1 Output Mode Setting These bits define the functional types of the output reference signal CH1OREF. 000: No Change 001: Output 0 on compare match 010: Output 1 on compare match 011: Output toggles on compare match 100: Force inactive – CH1OREF is forced to 0 101: Force active – CH1OREF is forced to 1 110: PWM mode 1 – During up-counting, channel 1 is at the active level when CNTR<CH1CCR or else at an inactive level. – During down-counting, channel 1 is at the inactive level when CNTR>CH1CCR or else at an active level. 111: PWM mode 2 – During up-counting, channel 1 is at the inactive level when CNTR<CH1CCR or else at an active level. – During down-counting, channel 1 is at the active level when CNTR>CH1CCR or else at an inactive level.

Channel 2 Output Configuration Register – CH2OCFR

This register specifies the channel 2 output mode configuration.

Offset: 0x048

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
		Reserved	CH2IMAE	CH2PRE	REF2CE	CH2OM		
Type/Reset			RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[5]	CH2IMAE	Channel 2 Immediate Active Enable 0: No action 1: Single pulse Immediate Active Mode is enabled The CH2OREF will be forced to the compare matched level immediately after an available trigger event occurs irrespective of the result of the comparison between the CNTR and the CH2CCR values. The effective duration ends automatically at the next overflow or underflow event. **Note:** The CH2IMAE bit is available only if the channel 2 is configured to be operated in the PWM mode 1 or the PWM mode 2.
[4]	CH2PRE	Channel 2 Capture/Compare Register (CH2CCR) Preload Enable 0: CH2CCR preload function is disabled The CH2CCR register can be immediately assigned a new value when the CH2PRE bit is cleared to 0 and the updated CH2CCR value is used immediately. 1: CH2CCR preload function is enabled The new CH2CCR value will not be transferred to its shadow register until the update event occurs.
[3]	REF2CE	Channel 2 Reference Output Clear Enable 0: CH2OREF performed normally and is not affected by the ETIF signal 1: CH2OREF is forced to 0 on the high level of the ETIF signal derived from the GTn_ETI pin

Bits	Field	Descriptions
[2:0]	CH2OM	Channel 2 Output Mode Setting These bits define the functional types of the output reference signal CH2OREF. 000: No Change 001: Output 0 on compare match 010: Output 1 on compare match 011: Output toggles on compare match 100: Force inactive – CH2OREF is forced to 0 101: Force active – CH2OREF is forced to 1 110: PWM mode 1 – During up-counting, channel 2 is at the active level when CNTR<CH2CCR or else at an inactive level. – During down-counting, channel 2 is at the inactive level when CNTR>CH2CCR or else at an active level. 111: PWM mode 2 – During up-counting, channel 2 is at the inactive level when CNTR<CH2CCR or else at an active level. – During down-counting, channel 2 is at the active level when CNTR>CH2CCR or else at an inactive level.

Channel 3 Output Configuration Register – CH3OCFR

This register specifies the channel 3 output mode configuration.

Offset: 0x04C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
		Reserved	CH3IMAE	CH3PRE	REF3CE	CH3OM		
Type/Reset			RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[5]	CH3IMAE	Channel 3 Immediate Active Enable 0: No action 1: Single pulse Immediate Active Mode is enabled The CH3OREF will be forced to the compare matched level immediately after an available trigger event occurs irrespective of the result of the comparison between the CNTR and the CH3CCR values. The effective duration ends automatically at the next overflow or underflow event. **Note:** The CH3IMAE bit is available only if the channel 3 is configured to be operated in the PWM mode 1 or the PWM mode 2.
[4]	CH3PRE	Channel 3 Capture/Compare Register (CH3CCR) Preload Enable 0: CH3CCR preload function is disabled The CH3CCR register can be immediately assigned a new value when the CH3PRE bit is cleared to 0 and the updated CH3CCR value is used immediately. 1: CH3CCR preload function is enabled The new CH3CCR value will not be transferred to its shadow register until the update event occurs.
[3]	REF3CE	Channel 3 Reference Output Clear Enable 0: CH3OREF performed normally and is not affected by the ETIF signal 1: CH3OREF is forced to 0 on the high level of the ETIF signal derived from the GTn_ETI pin

Bits	Field	Descriptions
[2:0]	CH3OM	Channel 3 Output Mode Setting These bits define the functional types of the output reference signal CH3OREF 000: No Change 001: Output 0 on compare match 010: Output 1 on compare match 011: Output toggles on compare match 100: Force inactive – CH3OREF is forced to 0 101: Force active – CH3OREF is forced to 1 110: PWM mode 1 – During up-counting, channel 3 is at the active level when CNTR<CH3CCR or else at an inactive level. – During down-counting, channel 3 is at the inactive level when CNTR>CH3CCR or else at an active level. 111: PWM mode 2 – During up-counting, channel 3 is at the inactive level when CNTR<CH3CCR or else at an active level. – During down-counting, channel 3 is at the active level when CNTR>CH3CCR or else at an inactive level.

Channel Control Register – CHCTR

This register contains the channel capture input or compare output function enable control bits.

Offset: 0x050

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved	CH3E	Reserved	CH2E	Reserved	CH1E	Reserved	CH0E
Type/Reset		RW 0		RW 0		RW 0		RW 0

Bits	Field	Descriptions
[6]	CH3E	Channel 3 Capture/Compare Enable – Channel 3 is configured as an input (CH3CCS=0x01/0x02/0x03) 0: Input Capture Mode disabled 1: Input Capture Mode enabled – Channel 3 is configured as an output (CH3CCS=0x00) 0: Off – Channel 3 output signal CH3O is not active 1: On – Channel 3 output signal CH3O generated on the corresponding output pin
[4]	CH2E	Channel 2 Capture/Compare Enable – Channel 2 is configured as an input (CH2CCS=0x01/0x02/0x03) 0: Input Capture Mode disabled 1: Input Capture Mode enabled – Channel 2 is configured as an output (CH2CCS=0x00) 0: Off – Channel 2 output signal CH2O is not active 1: On – Channel 2 output signal CH2O generated on the corresponding output pin
[2]	CH1E	Channel 1 Capture/Compare Enable – Channel 1 is configured as an input (CH1CCS=0x01/0x02/0x03) 0: Input Capture Mode disabled 1: Input Capture Mode enabled – Channel 1 is configured as an output (CH1CCS=0x00) 0: Off – Channel 1 output signal CH1O is not active 1: On – Channel 1 output signal CH1O generated on the corresponding output pin
[0]	CH0E	Channel 0 Capture/Compare Enable – Channel 0 is configured as an input (CH0CCS=0x01/0x02/0x03) 0: Input Capture Mode disabled 1: Input Capture Mode enabled – Channel 0 is configured as an output (CH0CCS=0x00) 0: Off – Channel 0 output signal CH0O is not active 1: On – Channel 0 output signal CH0O generated on the corresponding output pin

Channel Polarity Configuration Register – CHPOLR

This register contains the channel capture input or compare output polarity control.

Offset: 0x054

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								

	7	6	5	4	3	2	1	0
	Reserved	CH3P	Reserved	CH2P	Reserved	CH1P	Reserved	CH0P
Type/Reset		RW 0		RW 0		RW 0		RW 0

Bits	Field	Descriptions
[6]	CH3P	Channel 3 Capture/Compare Polarity – When Channel 3 is configured as an input 0: capture event occurs on a Channel 3 rising edge 1: capture event occurs on a Channel 3 falling edge – When Channel 3 is configured as an output (CH3CCS=0x00) 0: Channel 3 Output active high 1: Channel 3 Output active low
[4]	CH2P	Channel 2 Capture/Compare Polarity – When Channel 2 is configured as an input 0: capture event occurs on a Channel 2 rising edge 1: capture event occurs on a Channel 2 falling edge – When Channel 2 is configured as an output (CH2CCS=0x00) 0: Channel 2 Output active high 1: Channel 2 Output active low
[2]	CH1P	Channel 1 Capture/Compare Polarity – When Channel 1 is configured as an input 0: capture event occurs on a Channel 1 rising edge 1: capture event occurs on a Channel 1 falling edge – Channel 1 is configured as an output (CH1CCS=0x00) 0: Channel 1 Output active high 1: Channel 1 Output active low
[0]	CH0P	Channel 0 Capture/Compare Polarity – When Channel 0 is configured as an input 0: capture event occurs on a Channel 0 rising edge 1: capture event occurs on a Channel 0 falling edge – When Channel 0 is configured as an output (CH0CCS=0x00) 0: Channel 0 Output active high 1: Channel 0 Output active low

Timer PDMA/Interrupt Control Register – DICTR

This register contains the timer PDMA and interrupt enable control bits.

Offset: 0x074

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved					TEVDE	Reserved	UEVDE
Type/Reset						RW 0		RW 0
	23	22	21	20	19	18	17	16
	Reserved				CH3CCDE	CH2CCDE	CH1CCDE	CH0CCDE
Type/Reset					RW 0	RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
	Reserved					TEVIE	Reserved	UEVIE
Type/Reset						RW 0		RW 0
	7	6	5	4	3	2	1	0
	Reserved				CH3CCIE	CH2CCIE	CH1CCIE	CH0CCIE
Type/Reset					RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[26]	TEVDE	Trigger event PDMA Request Enable 0: Trigger PDMA request disabled 1: Trigger PDMA request enabled
[24]	UEVDE	Update event PDMA Request Enable 0: Update event PDMA request disabled 1: Update event PDMA request enabled
[19]	CH3CCDE	Channel 3 Capture/Compare PDMA Request Enable 0: Channel 3 PDMA request disabled 1: Channel 3 PDMA request enabled
[18]	CH2CCDE	Channel 2 Capture/Compare PDMA Request Enable 0: Channel 2 PDMA request disabled 1: Channel 2 PDMA request enabled
[17]	CH1CCDE	Channel 1 Capture/Compare PDMA Request Enable 0: Channel 1 PDMA request disabled 1: Channel 1 PDMA request enabled
[16]	CH0CCDE	Channel 0 Capture/Compare PDMA Request Enable 0: Channel 0 PDMA request disabled 1: Channel 0 PDMA request enabled
[10]	TEVIE	Trigger event Interrupt Enable 0: Trigger event interrupt disabled 1: Trigger event interrupt enabled
[8]	UEVIE	Update event Interrupt Enable 0: Update event interrupt disabled 1: Update event interrupt enabled

Bits	Field	Descriptions
[3]	CH3CCIE	Channel 3 Capture/Compare Interrupt Enable 0: Channel 3 interrupt disabled 1: Channel 3 interrupt enabled
[2]	CH2CCIE	Channel 2 Capture/Compare Interrupt Enable 0: Channel 2 interrupt disabled 1: Channel 2 interrupt enabled
[1]	CH1CCIE	Channel 1 Capture/Compare Interrupt Enable 0: Channel 1 interrupt disabled 1: Channel 1 interrupt enabled
[0]	CH0CCIE	Channel 0 Capture/Compare Interrupt Enable 0: Channel 0 interrupt disabled 1: Channel 0 interrupt enabled

Timer Event Generator Register – EVGR

This register contains the software event generation bits.

Offset: 0x078

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved					TEVG	Reserved	UEVG
Type/Reset						WO 0		WO 0
	7	6	5	4	3	2	1	0
	Reserved				CH3CCG	CH2CCG	CH1CCG	CH0CCG
Type/Reset					WO 0	WO 0	WO 0	WO 0

Bits	Field	Descriptions
[10]	TEVG	Trigger Event Generation The trigger event TEV can be generated by setting this bit. It is cleared by hardware automatically. 0: No action 1: TEVIF flag is set
[8]	UEVG	Update Event Generation The update event UEV can be generated by setting this bit. It is cleared by hardware automatically. 0: No action 1: Reinitialize the counter The counter value returns to 0 or the CRR preload value, depending on the counter mode in which the current timer is being used. An update operation of any related registers will also be performed. For more detail descriptions, refer to the corresponding section.
[3]	CH3CCG	Channel 3 Capture/Compare Generation A Channel 3 capture/compare event can be generated by setting this bit. It is cleared by hardware automatically. 0: No action 1: Capture/compare event is generated on channel 3 If Channel 3 is configured as an input, the counter value is captured into the CH3CCR register and then the CH3CCIF bit is set. If Channel 3 is configured as an output, the CH3CCIF bit is set.

Bits	Field	Descriptions
[2]	CH2CCG	Channel 2 Capture/Compare Generation A Channel 2 capture/compare event can be generated by setting this bit. It is cleared by hardware automatically. 0: No action 1: Capture/compare event is generated on channel 2 If Channel 2 is configured as an input, the counter value is captured into the CH2CCR register and then the CH2CCIF bit is set. If Channel 2 is configured as an output, the CH2CCIF bit is set.
[1]	CH1CCG	Channel 1 Capture/Compare Generation A Channel 1 capture/compare event can be generated by setting this bit. It is cleared by hardware automatically. 0: No action 1: Capture/compare event is generated on channel 1 If Channel 1 is configured as an input, the counter value is captured into the CH1CCR register and then the CH1CCIF bit is set. If Channel 1 is configured as an output, the CH1CCIF bit is set.
[0]	CH0CCG	Channel 0 Capture/Compare Generation A Channel 0 capture/compare event can be generated by setting this bit. It is cleared by hardware automatically. 0: No action 1: Capture/compare event is generated on channel 0 If Channel 0 is configured as an input, the counter value is captured into the CH0CCR register and then the CH0CCIF bit is set. If Channel 0 is configured as an output, the CH0CCIF bit is set.

Timer Interrupt Status Register – INTSR

This register stores the timer interrupt status.

Offset: 0x07C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved					TEVIF	Reserved	UEVIF
Type/Reset						RW 0		RW 0
	7	6	5	4	3	2	1	0
	CH3OCF	CH2OCF	CH1OCF	CH0OCF	CH3CCIF	CH2CCIF	CH1CCIF	CH0CCIF
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[10]	TEVIF	Trigger Event Interrupt Flag This flag is set by hardware on a trigger event and is cleared by software. 0: No trigger event occurs 1: Trigger event occurs
[8]	UEVIF	Update Event Interrupt Flag. This bit is set by hardware on an update event and is cleared by software. 0: No update event occurs 1: Update event occurs **Note:** The update event is derived from the following conditions: – The counter overflows or underflows – The UEVG bit is set with UEVDIS=0 – A STI rising edge is received in slave restart mode with UEVDIS=0
[7]	CH3OCF	Channel 3 Over-Capture Flag This flag is set by hardware and cleared by software. 0: No over-capture event is detected 1: Capture event occurs again when the CH3CCIF bit is already set and it is not yet cleared by software
[6]	CH2OCF	Channel 2 Over-Capture Flag This flag is set by hardware and cleared by software. 0: No over-capture event is detected 1: Capture event occurs again when the CH2CCIF bit is already set and it is not cleared yet by software
[5]	CH1OCF	Channel 1 Over-Capture Flag This flag is set by hardware and cleared by software. 0: No over-capture event is detected 1: Capture event occurs again when the CH1CCIF bit is already set and it is not cleared yet by software

Bits	Field	Descriptions
[4]	CH0OCF	Channel 0 Over-Capture Flag This flag is set by hardware and cleared by software. 0: No over-capture event is detected 1: Capture event occurs again when the CH0CCIFbit is already set and it is not yet cleared by software
[3]	CH3CCIF	Channel 3 Capture/Compare Interrupt Flag – Channel 3 is configured as an output: 0: No match event occurs 1: The contents of the counter CNTR have matched the contents of the CH3CCR register This flag is set by hardware when the counter value matches the CH3CCR value with exception in some center-aligned counting mode. It is cleared by software. – Channel 3 is configured as an input: 0: No input capture occurs 1: Input capture occurs This bit is set by hardware on a capture event. It is cleared by software or by reading the CH3CCR register.
[2]	CH2CCIF	Channel 2 Capture/Compare Interrupt Flag – Channel 2 is configured as an output: 0: No match event occurs 1: The contents of the counter CNTR have matched the contents of the CH2CCR register This flag is set by hardware when the counter value matches the CH2CCR value with exception in some center-aligned counting mode. It is cleared by software. – Channel 2 is configured as an input: 0: No input capture occurs 1: Input capture occurs. This bit is set by hardware on a capture event. It is cleared by software or by reading the CH2CCR register.
[1]	CH1CCIF	Channel 1 Capture/Compare Interrupt Flag –Channel 1 is configured as an output: 0: No match event occurs 1: The contents of the counter CNTR have matched the contents of the CH1CCR register This flag is set by hardware when the counter value matches the CH1CCR value with exception in some center-aligned counting mode. It is cleared by software. – Channel 1 is configured as an input: 0: No input capture occurs 1: Input capture occurs This bit is set by hardware on a capture event. It is cleared by software or by reading the CH1CCR register.
[0]	CH0CCIF	Channel 0 Capture/Compare Interrupt Flag – Channel 0 is configured as an output: 0: No match event occurs 1: The contents of the counter CNTR have matched the content of the CH0CCR register This flag is set by hardware when the counter value matches the CH0CCR value with exception in some center-aligned counting mode. It is cleared by software. – Channel 0 is configured as an input: 0: No input capture occurs 1: Input capture occurs This bit is set by hardware on a capture event. It is cleared by software or by reading the CH0CCR register.

Timer Counter Register – CNTR

This register stores the timer counter value.

Offset: 0x080

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	CNTV							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	CNTV							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	CNTV	Counter Value.

Timer Prescaler Register – PSCR

This register specifies the timer prescaler value to generate the counter clock.

Offset: 0x084

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	PSCV							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	PSCV							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	PSCV	Prescaler Value These bits are used to specify the prescaler value to generate the counter clock frequency f_{CK_CNT}. $f_{CK\_CNT} = \frac{f_{CK\_PSC}}{PSCV[15:0]+1}$, where the f_{CK_PSC} is the prescaler clock source.

Timer Counter Reload Register – CRR

This register specifies the timer counter reload value.

Offset: 0x088

Reset value: 0x0000_FFFF

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	CRV							
Type/Reset	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1
	7	6	5	4	3	2	1	0
	CRV							
Type/Reset	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1

Bits	Field	Descriptions
[15:0]	CRV	Counter Reload Value The CRV is the reload value which is loaded into the actual counter register.

Channel 0 Capture/Compare Register – CH0CCR

This register specifies the timer channel 0 capture/compare value.

Offset: 0x090

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	CH0CCV							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	CH0CCV							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	CH0CCV	Channel 0 Capture/Compare Value – When Channel 0 is configured as an output The CH0CCR value is compared with the counter value and the comparison result is used to trigger the CH0OREF output signal. – When Channel 0 is configured as an input The CH0CCR register stores the counter value captured by the last channel 0 capture event.

Channel 1 Capture/Compare Register – CH1CCR

This register specifies the timer channel 1 capture/compare value.

Offset: 0x094

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	CH1CCV							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	CH1CCV							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	CH1CCV	Channel 1 Capture/Compare Value – When Channel 1 is configured as an output The CH1CCR value is compared with the counter value and the comparison result is used to trigger the CH1OREF output signal. – When Channel 1 is configured as an input The CH1CCR register stores the counter value captured by the last channel 1 capture event.

Channel 2 Capture/Compare Register – CH2CCR

This register specifies the timer channel 2 capture/compare value.

Offset: 0x098

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	CH2CCV							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	CH2CCV							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	CH2CCV	Channel 2 Capture/Compare Value – When Channel 2 is configured as an output The CH2CCR value is compared with the counter value and the comparison result is used to trigger the CH2OREF output signal. – When Channel 2 is configured as an input The CH2CCR register stores the counter value captured by the last channel 2 capture event.

Channel 3 Capture/Compare Register – CH3CCR

This register specifies the timer channel 3 capture/compare value.

Offset: 0x09C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	CH3CCV							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	CH3CCV							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	CH3CCV	Channel 3 Capture/Compare Value – When Channel 3 is configured as an output The CH3CCR value is compared with the counter value and the comparison result is used to trigger the CH3OREF output signal. – When Channel 3 is configured as an input The CH3CCR register stores the counter value captured by the last channel 3 capture event.

15 Basic Function Timer (BFTM)

Introduction

The Basic Function Timer Module, BFTM, is a 32-bit up-counting counter designed to measure time intervals, generate one shot pulses or generate repetitive interrupts. The BFTM can operate in two modes which are repetitive and one shot modes. The repetitive mode restarts the counter at each compare match event which is generated by the internal comparator. The BFTM also supports a one shot mode which will force the counter to stop counting when a compare match event occurs.

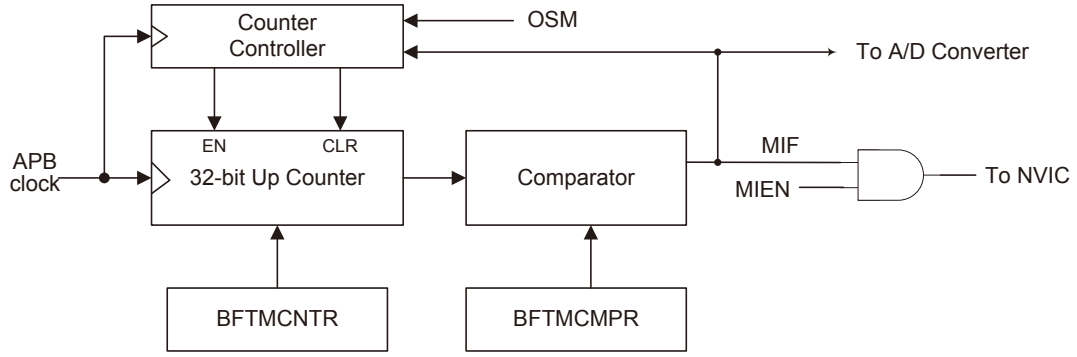


Figure 65. BFTM Block Diagram

Features

- 32-bit up-counting counter
- Compare Match function
- Includes debug mode
- Clock source: APB clock
- Counter value can be R/W on the fly
- One shot mode: counter stops counting when compare match occurs
- Repetitive mode: counter restarts when compare match occurs
- Compare Match interrupt enable/disable control

Functional Descriptions

The BFTM is a 32-bit up-counting counter which is driven by the APB clock, PCLK. The counter value can be changed or read at any time even when the timer is counting. The BFTM supports two operating modes known as the repetitive mode and one shot mode allowing the measurement of time intervals or the generation of periodic time durations.

Repetitive Mode

The BFTM counts up from zero to a specific compare value which is pre-defined by the BFTMnCMPR register. When the BFTM operates in the repetitive mode and the counter reaches a value equal to the specific compare value in the BFTMnCMPR register, the timer will generate a compare match event signal, MIFn. When this occurs, the counter will be reset to 0 and resume its counting operation. When the MIFn signal is generated, a BFTM compare match interrupt will also be generated periodically if the compare match interrupt is enabled by setting the corresponding interrupt control bit, MIENn, to 1. The counter value will remain unchanged and the counter will stop counting if it is disabled by clearing the CENn bit to 0.

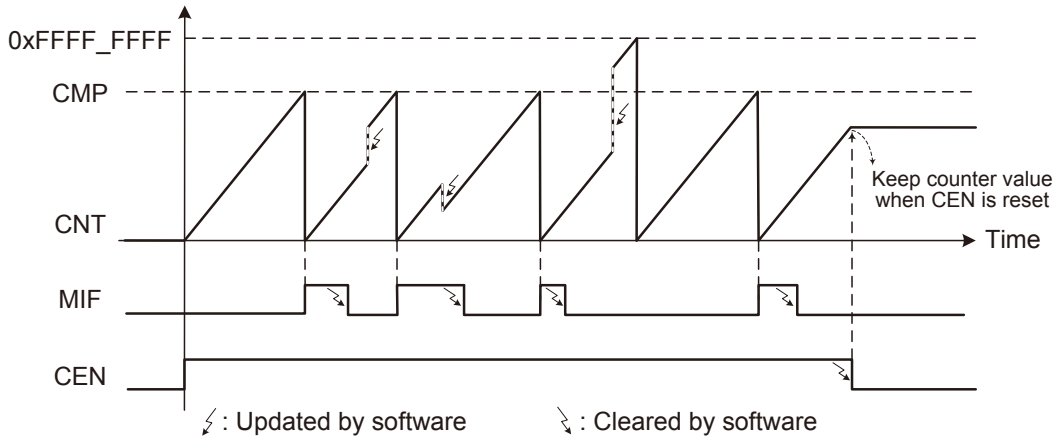


Figure 66. BFTM – Repetitive Mode

One Shot Mode

By setting the OSMn bit in BFTMnCR register to 1, the BFTM will operate in the one shot mode. The BFTM starts to count when the CENn bit is set to 1 by the application program. The counter value will remain unchanged if the CENn bit is cleared to 0 by the application program. However, the counter value will be reset to 0 and stop counting when the CENn bit is cleared automatically to 0 by the internal hardware when a counter compare match event occurs.

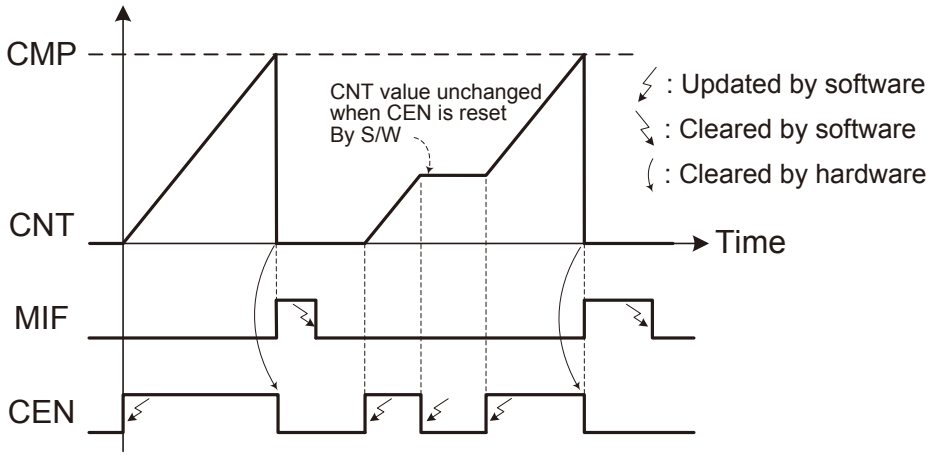


Figure 67. BFTM – One Shot Mode

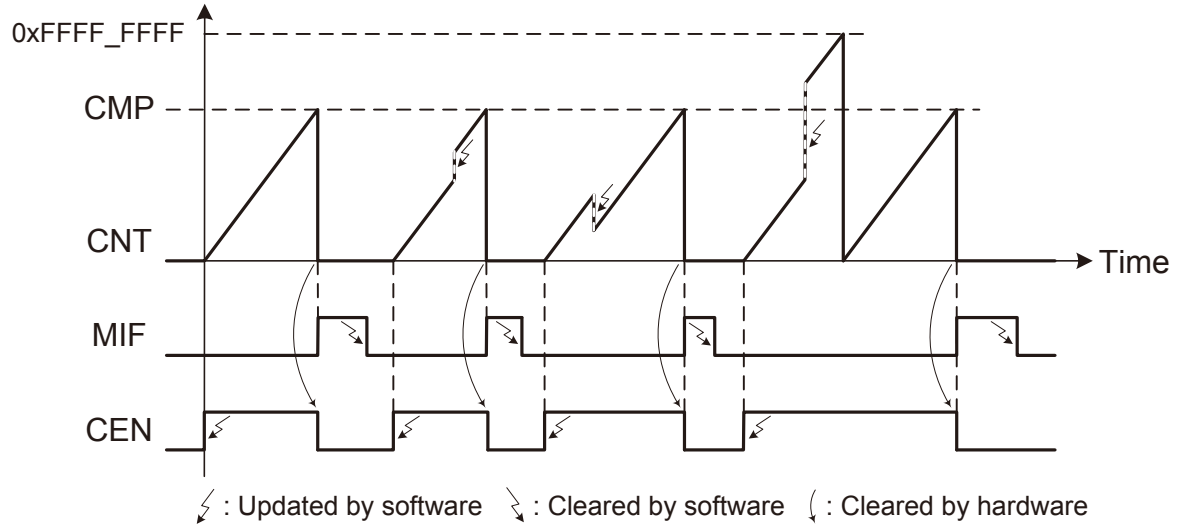


Figure 68. BFTM – One Shot Mode Counter Updating

Trigger ADC Start

When a BFTM compare match event occurs, a compare match interrupt flag, MIFn, will be generated which can be used as an A/D Converter input trigger source.

Register Map

The following table shows the BFTM registers and their reset values.

Table 32. BFTM Register Map

Register	Offset	Description	Reset Value
BFTM0 Base Address=0x4007_6000 BFTM1 Base Address=0x4007_7000			
BFTMnCR	0x000	BFTMn Control Register	0x0000_0000
BFTMnSR	0x004	BFTMn Status Register	0x0000_0000
BFTMnCNTR	0x008	BFTMn Counter Value Register	0x0000_0000
BFTMnCMPR	0x00C	BFTMn Compare Value Register	0xFFFF_FFFF

Register Descriptions

BFTMn Control Register – BFTMnCR, n=0~1

This register specifies the overall BFTMn control bits.

Offset: 0x000

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved					CENn	OSMn	MIENn
Type/Reset						RW 0	RW 0	RW 0

Bits	Field	Descriptions
[2]	CENn	BFTMn Counter Enable Control 0: BFTM is disabled 1: BFTM is enabled When this bit is set to 1, the BFTM counter will start to count. The counter will stop counting and the counter value will remain unchanged when the CENn bit is cleared to 0 by the application program regardless of whether it is in the repetitive or one shot mode. However, in the one shot mode, the counter will stop counting and be reset to 0 when the CENn bit is cleared to 0 by the timer hardware circuitry which results from a compare match event.
[1]	OSMn	BFTMn One Shot Mode Selection 0: Counter operates in repetitive mode 1: Counter operates in one shot mode
[0]	MIENn	BFTM n Compare Match Interrupt Enable Control 0: Compare Match Interrupt is disabled 1: Compare Match Interrupt is enabled

BFTMn Status Register – BFTMnSR, n=0~1

This register specifies the BFTMn status.

Offset: 0x004

Reset value: 0x0000_0004

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved							MIFn
Type/Reset								W0C 0

Bits	Field	Descriptions
[0]	MIFn	BFTMn Compare Match Interrupt Flag 0: No compare match event occurs 1: Compare match event occurs When the counter value, CNTn, is equal to the compare register value, CMPn, a compare match event will occur and the corresponding interrupt flag, MIFn will be set. The MIFn bit is cleared to 0 by writing 0.

BFTMn Counter Register – BFTMnCNTR, n=0~1

This register specifies the BFTMn counter value.

Offset: 0x008

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	CNTn							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	CNTn							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	CNTn							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	CNTn							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[31:0]	CNTn	BFTMn Counter Register A 32-bit BFTMn counter value is stored in this field which can be read or written on-the-fly.

BFTMn Compare Value Register – BFTMnCMPR, n=0~1

The register specifies the BFTMn compare value.

Offset: 0x00C

Reset value: 0xFFFF_FFFF

	31	30	29	28	27	26	25	24
	CMPn							
Type/Reset	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1
	23	22	21	20	19	18	17	16
	CMPn							
Type/Reset	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1
	15	14	13	12	11	10	9	8
	CMPn							
Type/Reset	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1
	7	6	5	4	3	2	1	0
	CMPn							
Type/Reset	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1

Bits	Field	Descriptions
[31:0]	CMPn	BFTMn Compare Value Register This register specifies a 32-bit BFTMn compare value which is used for comparison with the BFTMn counter value.

16 Motor Control Timer (MCTM)

Introduction

The Motor Control Timer consists of one 16-bit up/down-counter, four 16-bit Capture/Compare Registers (CCRs), one 16-bit Counter-Reload Register (CRR), one 8-bit Repetition Counter (REPR) and several control/status registers. It can be used for a variety of purposes which include general time measurement, input signal pulse width measurement, output waveform generation for signals such as single pulse generation or PWM generation, including dead time insertion. The MCTM supports an encoder interface using a quadrature decoder with two inputs.

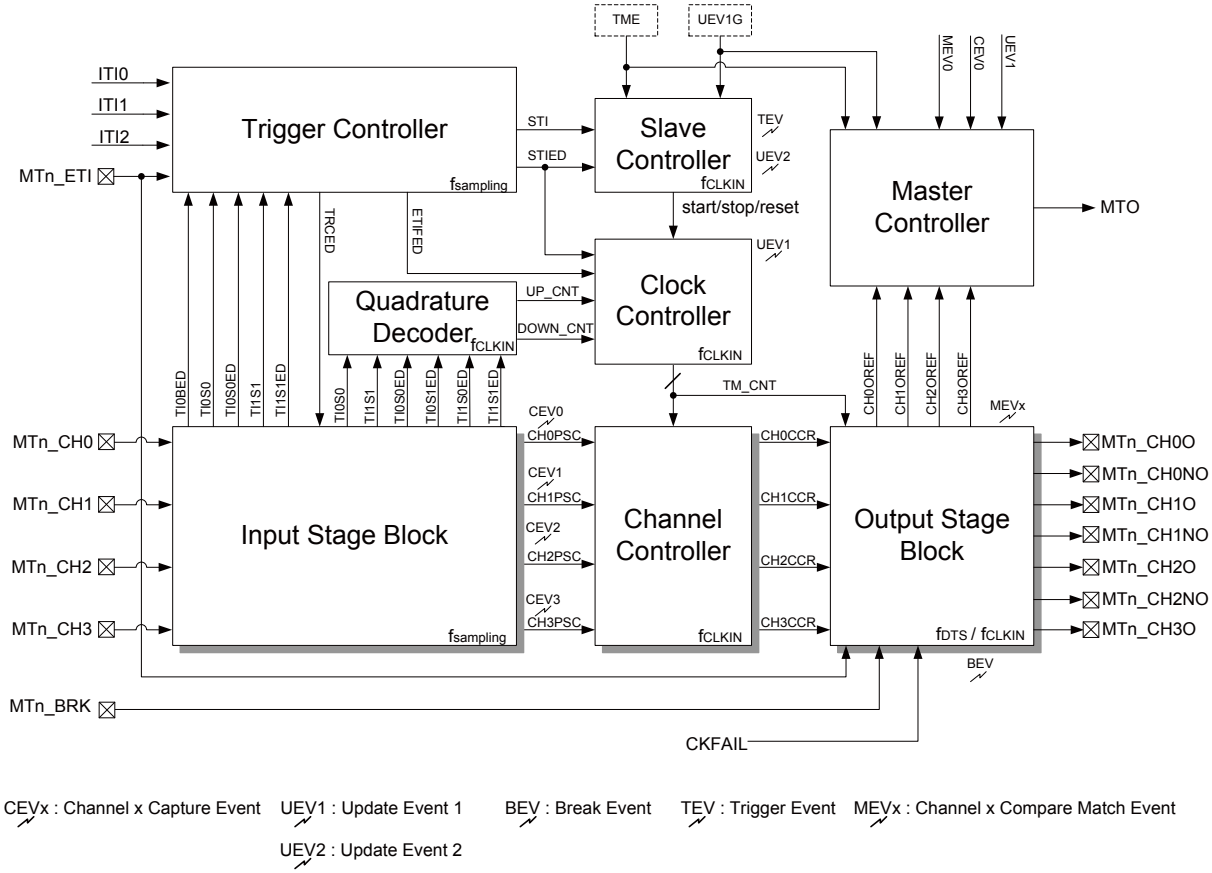


Figure 69. MCTM Block Diagram

Features

- 16-bit up/down auto-reload counter
- 16-bit programmable prescaler that allows division the counter clock frequency by any factor between 1 and 65536
- Up to 4 independent channels for:
  - Input Capture function
  - Compare Match Output
  - PWM waveform Generation – Edge-aligned and Center-aligned Counting Modes
  - Single Pulse Mode Output
- Complementary Outputs with programmable dead-time insertion
- Encoder interface controller with two inputs using quadrature decoder
- Repetition counter updates timer registers only after a given number of counter cycles
- Synchronization circuit controls the timer with external signals and can interconnect several timers together
- Interrupt/PDMA generation on the following events:
  - Update event 1
  - Update event 2
  - Trigger event
  - Input capture event
  - Output compare match
  - Break event – only interrupt
- MCTM Master/Slave mode controller
- Supports 3-phase motor control and hall sensor interface
- Break input to assert the timer output signals in reset state or in a known state

Functional Descriptions

Counter Modes

Up-counting

In this mode the counter counts continuously from 0 to the counter-reload value, which is defined in the CRR register, in a count-up direction. Once the counter reaches the counter-reload value, the Timer Module generates an overflow event and the counter restarts to count once again from 0. This action will continue repeatedly. The counting direction bit DIR in the CNTCFR register should be set to 0 for the up-counting mode.

When an update event 1 is generated by setting the UEV1G bit in the EVGR register to 1, the counter value will also be initialised to 0.

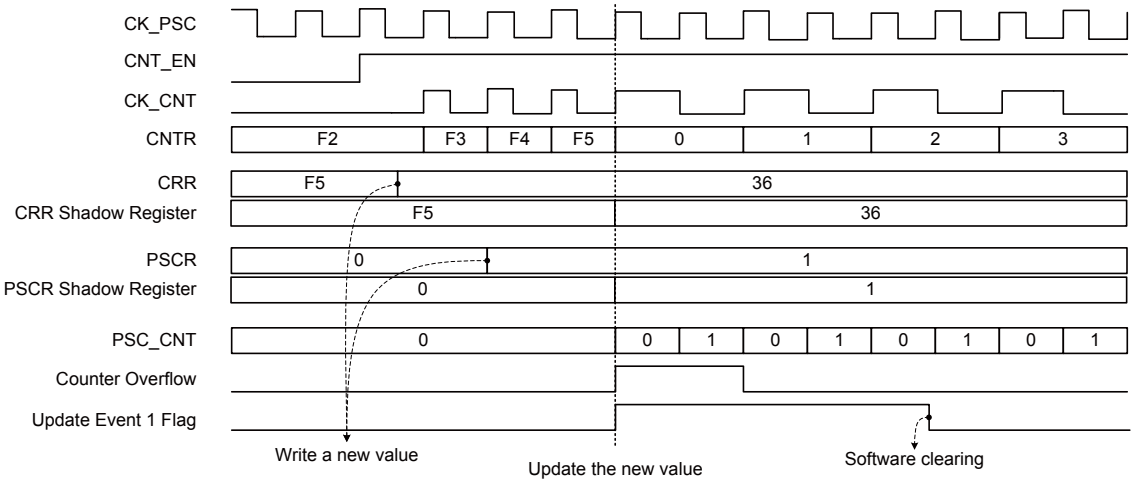


Figure 70. Up-counting Example

Down-counting

In this mode the counter counts continuously from the counter-reload value, which is defined in the CRR register, to 0 in a count-down direction. Once the counter reaches 0, the Timer module generates an underflow event and the counter restarts to count once again from the counter-reload value. This action will continue repeatedly. The counting direction bit DIR in the CNTCFR register should be set to 1 for the down-counting mode.

When an update event 1 is generated by setting the UEV1G bit in the EVGR register to 1, the counter value will also be initialised to the counter-reload value.

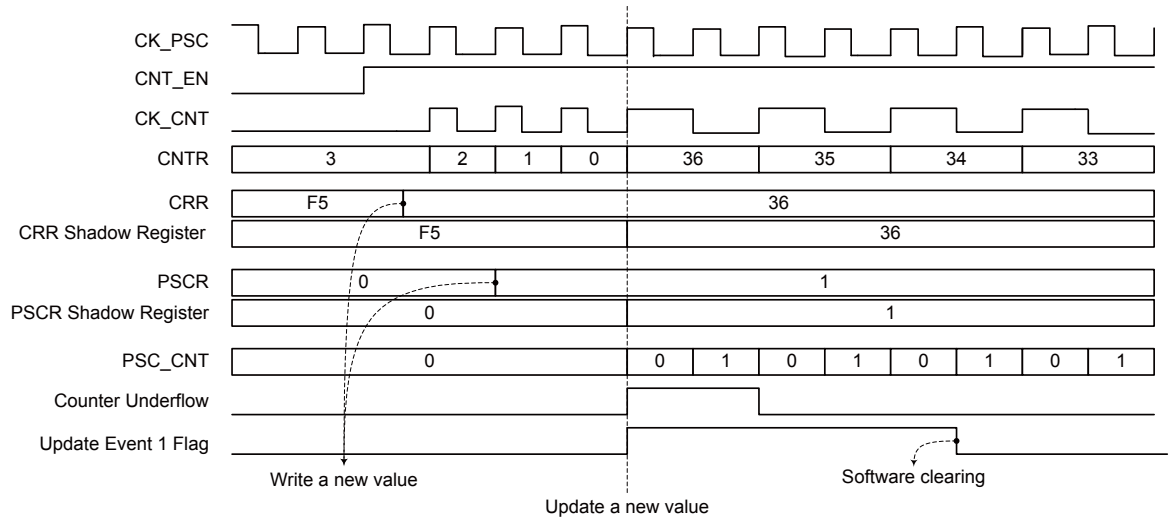


Figure 71. Down-counting Example

Center-aligned Counting

In the center-aligned counting mode, the counter counts up from 0 to the counter-reload value and then counts down to 0 alternatively. The Timer Module generates an overflow event when the counter counts to the counter-reload value in the up-counting mode and generates an underflow event when the counter counts to 0 in the down-counting mode. The counting direction bit DIR in the CNTCFR register is read-only and indicates the count direction when in the center-aligned counting mode. The count direction is updated by hardware automatically.

Setting the UEV1G bit in the EVGR register will initialise the counter value to 0 irrespective of whether the counter is counting up or down in the center-aligned counting mode.

The UEV1IF bit in the INTSR register can be set to 1 according to the CMSEL field setting in the CNTCFR register. When CMSEL=0x01, an underflow event will set the UEV1IF bit to 1. When CMSEL=0x10, an overflow event will set the UEV1IF bit to 1. When CMSEL=0x11, either underflow or overflow event will set the UEV1IF bit to 1.

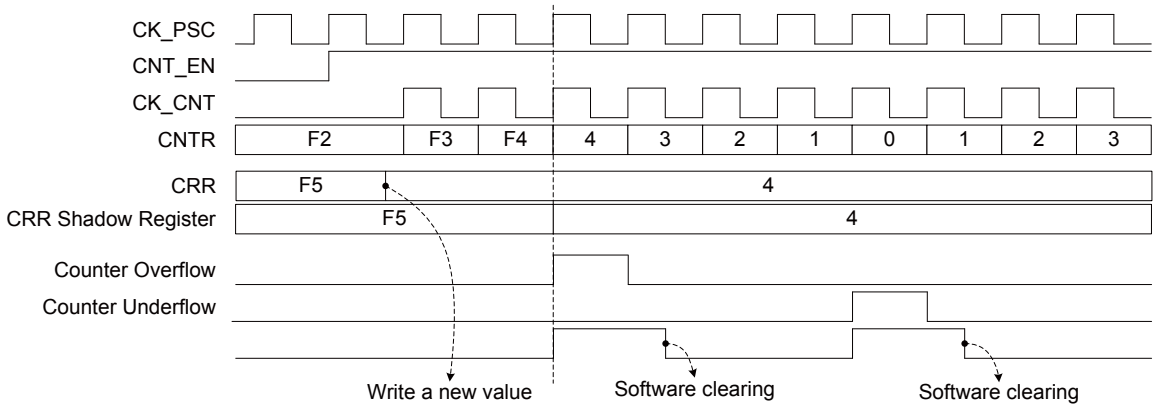


Figure 72. Center-aligned Counting Example

Repetition Down-counter Operation

The update event 1 is usually generated at each overflow or underflow event occurrence. However, when the repetition operation is active by assigning a non-zero value into the REPR register, the update event is only generated if the REPR counter has reached zero. The REPR value is decreased when the following conditions occur:

- At each counter overflow in the up-counting mode
- At each counter underflow in the down-counting mode
- At each counter overflow and at each counter underflow in the center-aligned counting mode

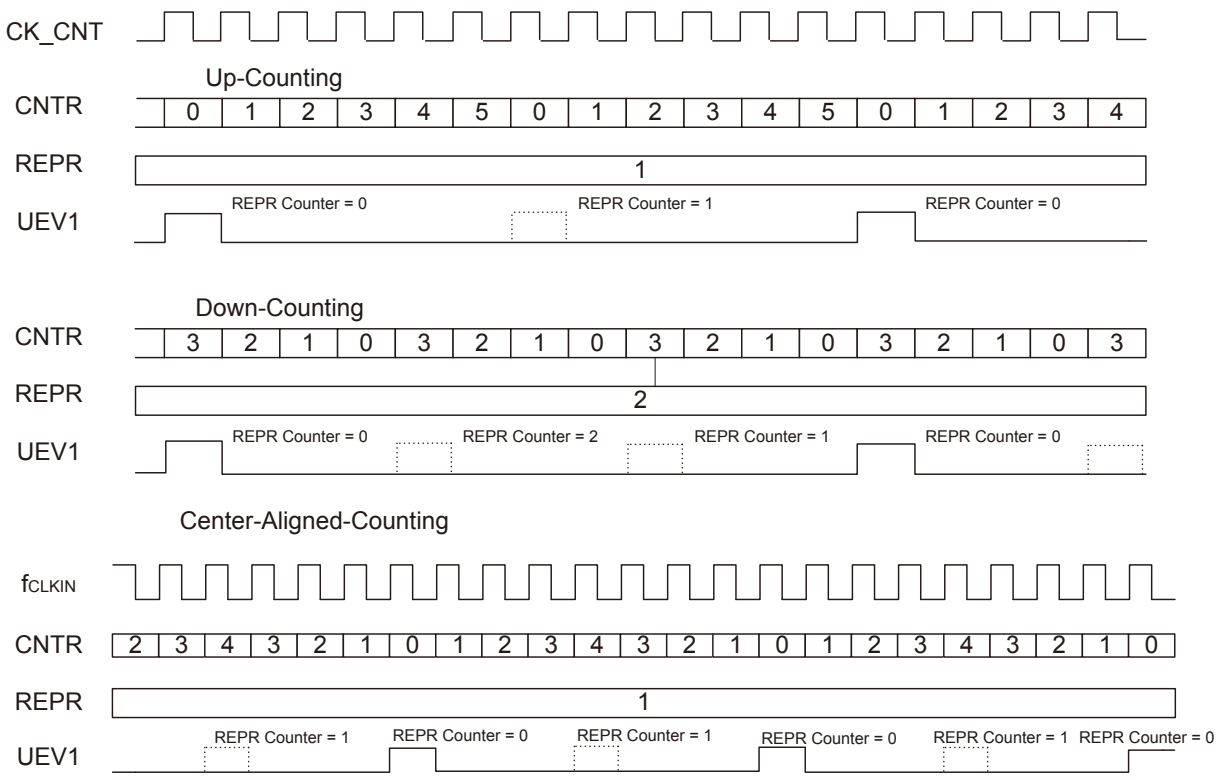


Figure 73. Update Event Dependent Repetition Mechanism Example

Clock Controller

The following describes the Timer Module clock controller which determines the internal prescaler counter clock source.

■ Internal APB clock f_{CLKIN}:

The default internal clock source is the APB clock f_{CLKIN} which is used to drive the counter prescaler when the slave mode is disabled. When the slave mode selection bits SMSEL are set to 0x4, 0x5 or 0x6, the internal APB clock f_{CLKIN} is the counter prescaler driving clock source.

■ Quadrature Decoder:

To select the Quadrature Decoder mode the SMSEL field should be set to 0x1, 0x2 or 0x3 in the MDCFR register. The Quadrature Decoder function uses the two input conditions of the MTn_CH0 and MTn_CH1 pins to generate the clock pulses to drive the counter prescaler. The counting direction bit DIR is modified by hardware automatically at each transition on the input source signal.

■ STIED:

The counter prescaler can count during each rising edge of the STI signal. This mode can be selected by setting the SMSEL field to 0x7 in the MDCFR register. Here the counter will act as an event counter. The input event, known as STI here, can be selected by setting the TRSEL field to an available value except the value of 0x0. When the STI signal is selected as the clock source, the internal edge detection circuitry will generate a clock pulse during each STI signal rising edge to drive the counter prescaler. It is important to note that if the TRSEL field is set to 0x0 to select the software UEV1G bit as the trigger source, then when the SMSEL field is set to 0x7, the counter will be updated instead of counting.

■ ETIFED:

The counter prescaler can be driven to count during each rising edge on ETIF. This mode can be selected by setting the ECME bit in the TRCFR register to 1. The other way to select the ETIF signal as the clock source is to set the SMSEL field to 0x7 and the TRSEL field to 0x3 respectively. When the clock source is selected to come from the ETIF signal, the Trigger Controller including the edge detection circuitry will generate a clock pulse during each ETIF signal rising edge to clock the counter prescaler.

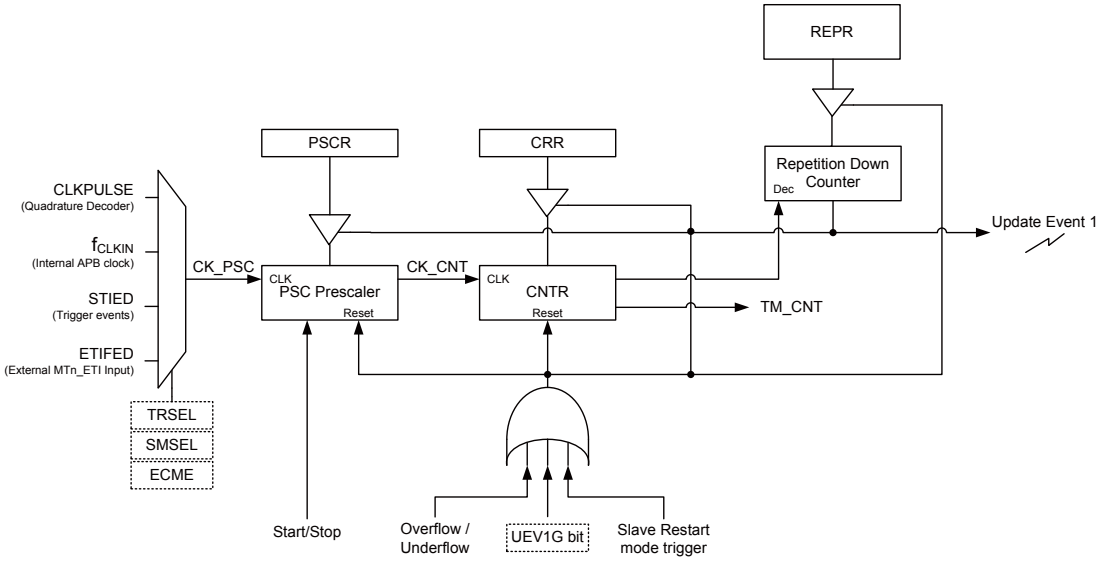


Figure 74. MCTM Clock Selection Source

Trigger Controller

The trigger controller is used to select the trigger source and setup the trigger level and edge trigger conditions. The active polarity of the external trigger input signal MTn_ETI can be configured by the External Trigger Polarity control bit, ETIPOL, in the MCTM Trigger Configuration Register TRCFR. The frequency of the external trigger input can be divided by configuring the related bits, which are the External Trigger Prescaler control bits, ETIPSC, in the TRCFR register. The trigger signal can also be filtered by configuring the External Trigger Filter ETF selection bits in the TRCFR register if a filtered signal is necessary for specific applications. For the internal trigger input, it can be selected by the Trigger Selection bits, TRSEL, in the TRCFR register. For all the trigger sources except the UEV1G bit software trigger, the internal edge detection circuitry will generate a clock pulse at each trigger signal rising edge to activate some MCTM functions which are triggered by a trigger signal rising edge.

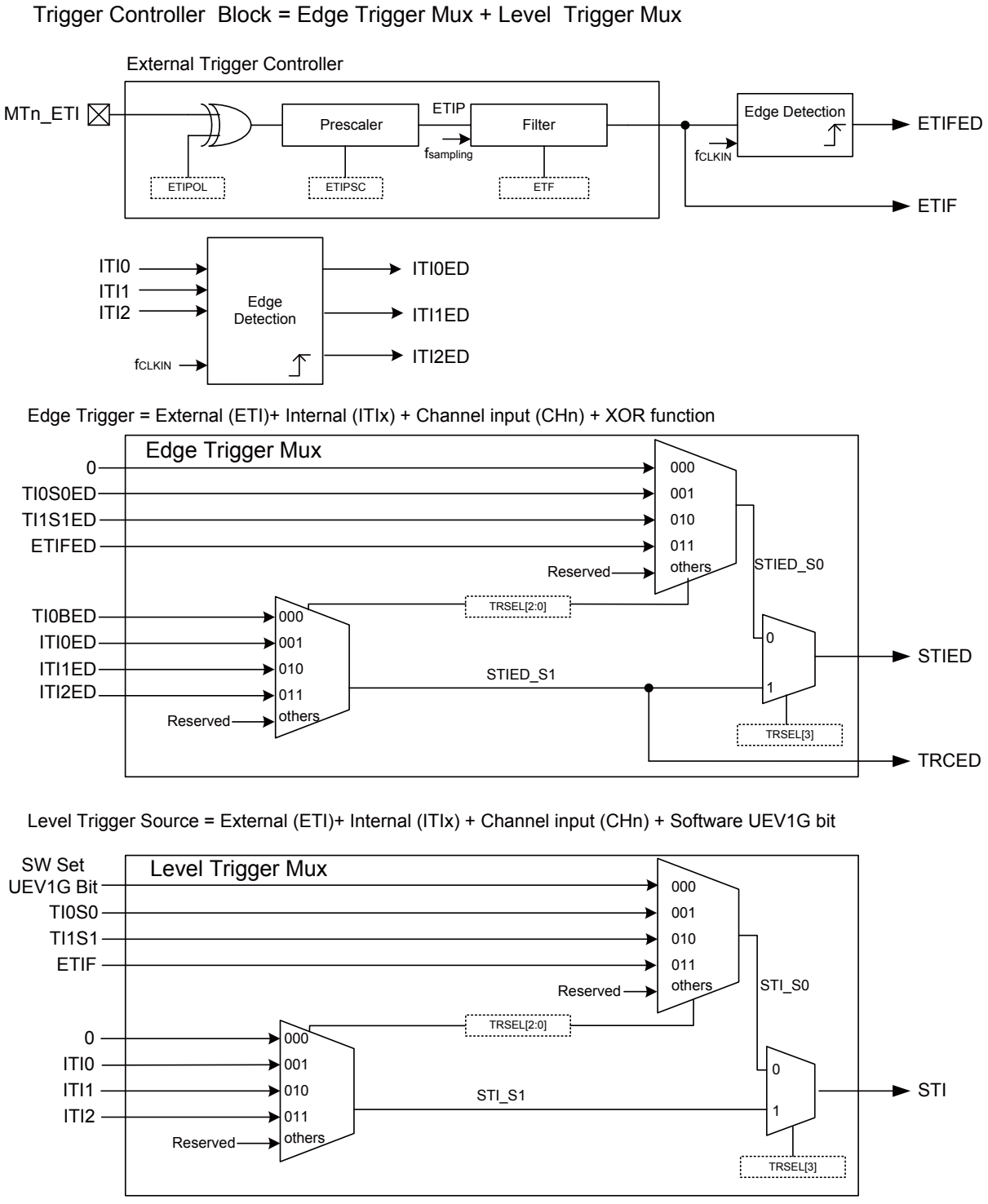


Figure 75. Trigger Control Block

Slave Controller

The MCTM can be synchronised with an internal/external trigger in several modes including the Restart mode, the Pause mode and the Trigger mode which are selected by the SMSEL field in the MDCFR register. The trigger input of these modes comes from the STI signal which is selected by the TRSEL field in the TRCFR register. The operation modes in the Slave Controller are described in the accompanying sections.

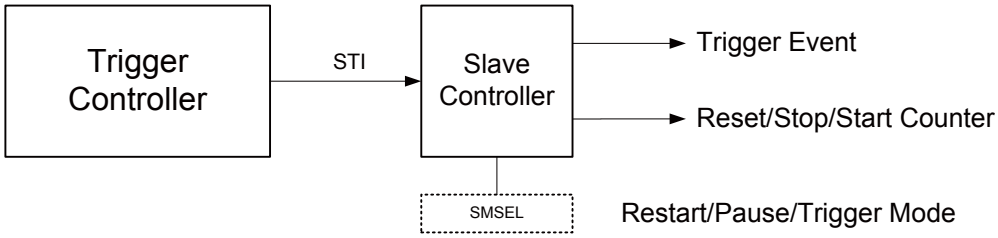


Figure 76. Slave Controller Diagram

Restart Mode

The counter and its prescaler can be reinitialised in response to an STI signal rising edge. If the UEV1DIS bit is set to 1 to disable the update event, then no update event will be generated, however the counter and prescaler are still reinitialised when an STI rising edge occurs. If the UEV1DIS bit in the CNTCFR register is cleared to enable the update event, then an update event will be generated together with the STI rising edge and all the preloaded registers will be updated.

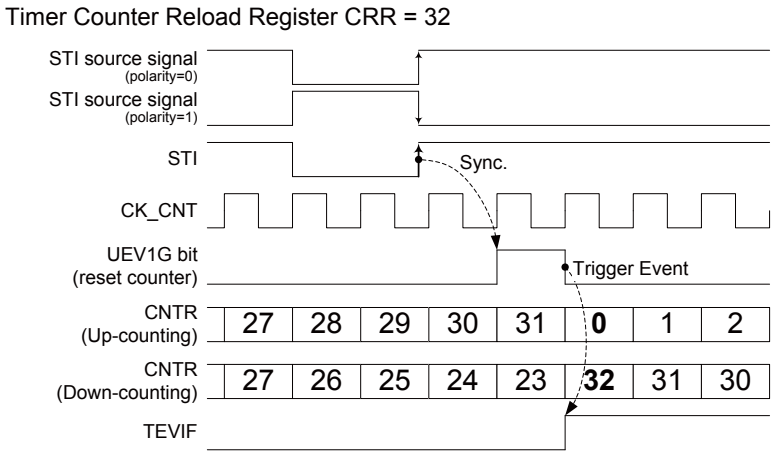


Figure 77. MCTM in Restart Mode

Pause Mode

In the Pause Mode, the selected STI input signal level is used to control the counter start/stop operation. The counter starts to count when the selected STI signal is at a high level and stops counting when the STI signal is changed to a low level. When the counter stops, it will maintain its present value and not be reset. Since the Pause function depends upon the STI level to control the counter stop/start operation, the selected STI trigger signal can not be derived from the TI0BED signal.

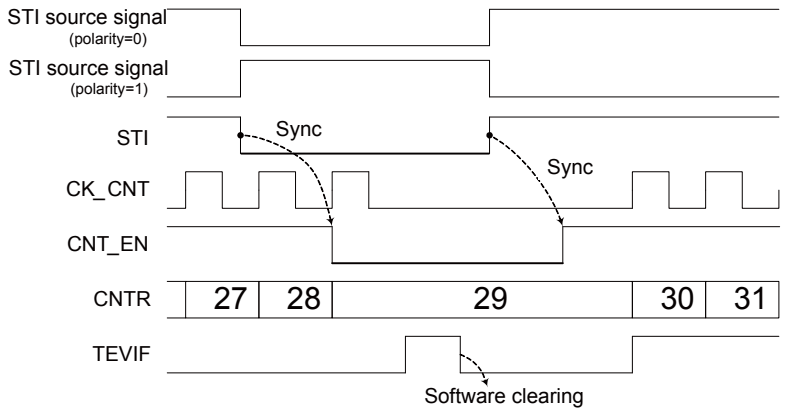


Figure 78. MCTM in Pause Mode

Trigger Mode

After the counter is disabled to count, the counter can resume counting when an STI rising edge signal occurs. When an STI rising edge occurs, the counter will start to count from the current value in the counter. Note that if the STI signal is selected to be sourced from the UEV1G bit software trigger, the counter will not resume counting. When software triggering using the UEV1G bit is selected as the STI source signal, there will be no clock pulse generated which can be used to make the counter resume counting. Note that the STI signal is only used to enable the counter to resume counting and has no effect to stop counting.

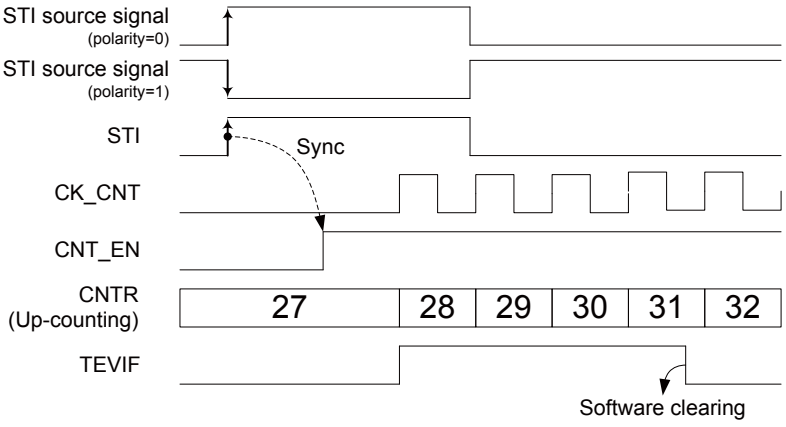


Figure 79. MCTM in Trigger Mode

Master Controller

The MCTMs and GPTMs can be linked together internally for timer synchronisation or chaining. When one MCTM is configured to be in the Master Mode, the MCTM Master Controller will generate a Master Trigger Output (MTO) signal which can reset, start, stop the Slave counter or be a clock source of the Slave counter. This can be selected by the MMSEL field in the MDCFR register to trigger or drive another MCTM or GPTM which should be configured in the Slave Mode.

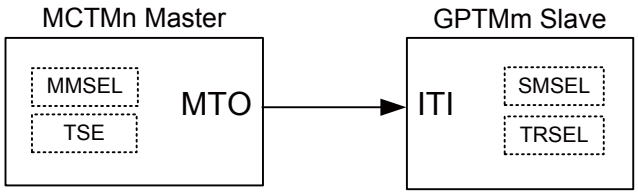


Figure 80. Master MCTMn and Slave GPTM Connection

The Master Mode Selection bits, MMSEL, in the MDCFR register are used to select the MTO source for synchronising another slave MCTM or GPTM.

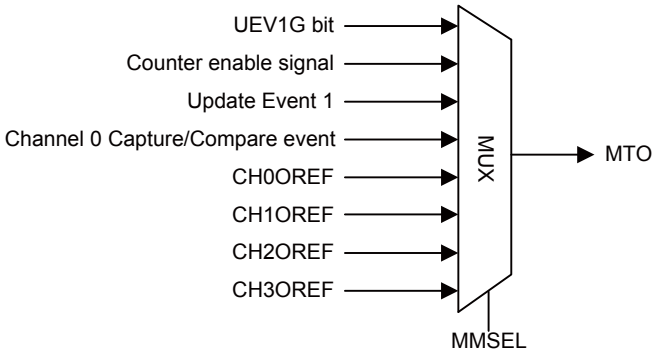


Figure 81. MTO selection

For example, setting the MMSEL field to 0x5 is to select the CH1OREF signal as the MTO signal to synchronise another slave MCTM or GPTM. For a more detailed description, refer to the related MMSEL field definitions in the MDCFR register.

Channel Controller

The MCTM has four independent channels which can be used as capture inputs or compare match outputs. Each capture input or compare match output channel is composed of a preload register and a shadow register. Data access of the APB bus is always implemented through the read/write preload register.

When used in the input capture mode, the counter value is captured into the CHxCCR shadow register first and then transferred into the CHxCCR preload register when the capture event occurs.

When used in the compare match output mode, the contents of the CHxCCR preload register is copied into the associated shadow register, the counter value is then compared with the register value.

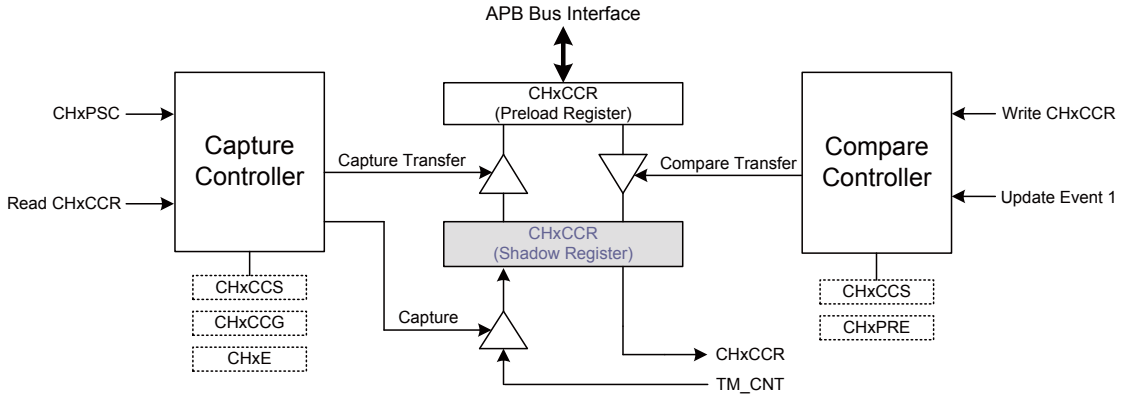


Figure 82. Capture/Compare Block Diagram

Capture Counter Value Transferred to CHxCCR

When the channel is used as a capture input, the counter value is captured into the Channel Capture/Compare Register (CHxCCR) when an effective input signal transition occurs. Once the capture event occurs, the CHxCCIF flag in the INTSR register is set accordingly. If the CHxCCIF bit is already set, i.e., the flag has not yet been cleared by software, and another capture event on this channel occurs, the corresponding channel Over-Capture flag, named CHxOCF, will be set.

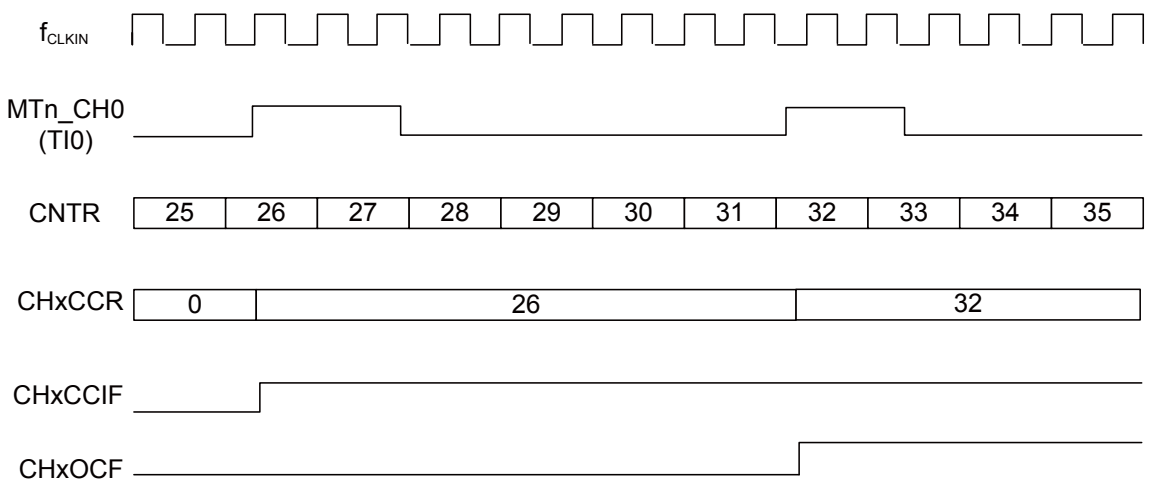


Figure 83. Input Capture Mode

Pulse Width Measurement

The input capture mode can be also used for pulse width measurement from signals on the MTn_CHx pins, TIx. The following example shows how to configure the MCTM when operated in the input capture mode to measure the high pulse width and the input period on the MTn_CH0 pin using channel 0 and channel 1. The basic steps are shown as follows.

- Configure the capture channel 0 (CH0CCS=0x1) to select the TI0 signal as the capture input
- Configure the CH0P bit to 0 to choose the rising edge of the TI0 input as the active polarity
- Configure the capture channel 1 (CH1CCS=0x2) to select the TI0 signal as the capture input
- Set the CH1P bit to 1 to choose the falling edge of the TI0 input as the active polarity
- Setup the TRSEL bits to 0x0001 to select TI0S0 as the trigger input
- Configure the Slave controller to operate in the Restart mode by setting the SMSEL field in the MDCFR register to 0x4
- Enable the input capture mode by setting the CH0E and CH1E bits in the CHCTR register to 1

As the following diagram shows, the high pulse width on the MTn_CH0 pin will be captured into the CH1CCR register while the input period will be captured into the CH0CCR register after an input capture operation.

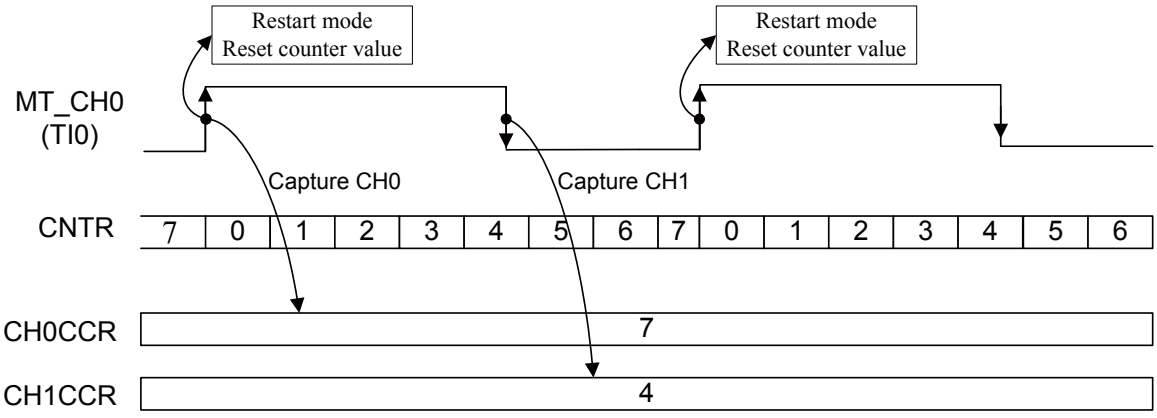


Figure 84. PWM Pulse Width Measurement Example

Input Stage

The input stage consists of a digital filter, a channel polarity selection, edge detection and a channel prescaler. The channel 0 input signal, TI0, can be chosen to come from the MTn_CH0 signal or the Excusive-OR function of the MTn_CH0, MTn_CH1 and MTn_CH2 signals. The channel input signal, TIx, is sampled by a digital filter to generate a filtered input signal TIxFP. Then the channel polarity and the edge detection block can generate a TIxSxED signal for the input capture function. The effective input event number can be set by the channel input prescaler register CHxPSC.

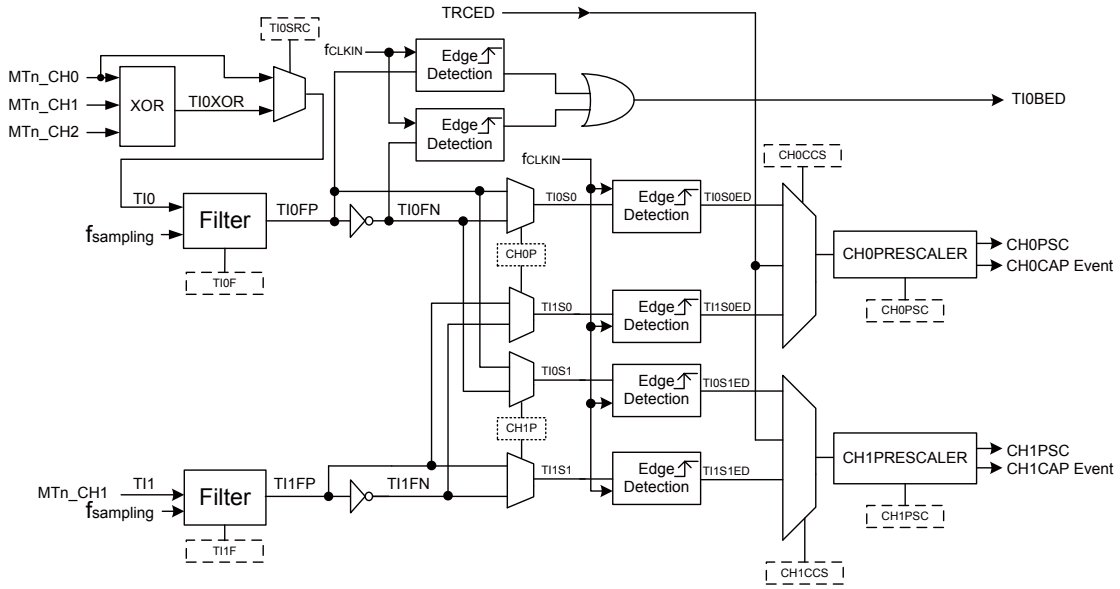


Figure 85. Channel 0 and Channel 1 Input Stage

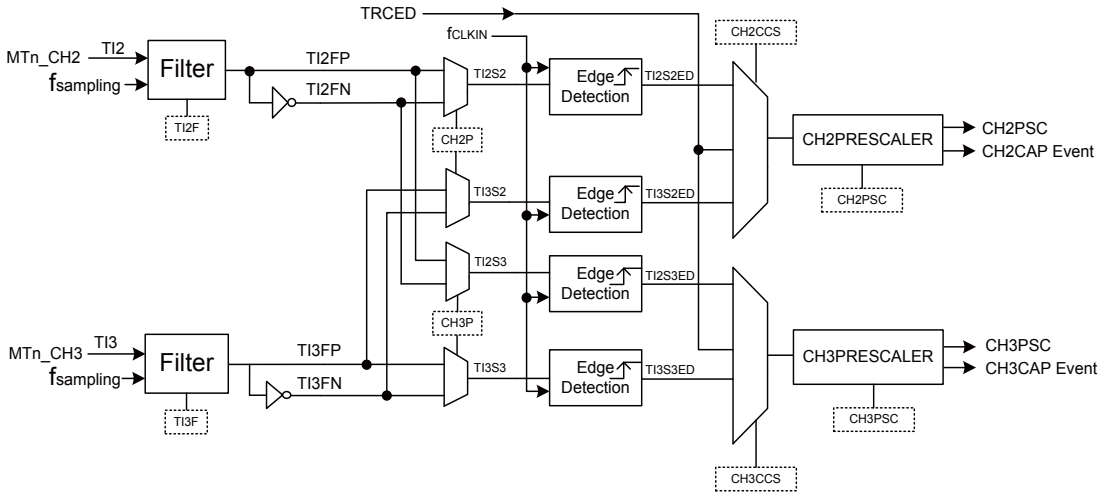


Figure 86. Channel 2 and Channel 3 Input Stage

Output Stage

The MCTM supports complementary outputs for channels 0, 1 and 2 with dead time insertion. The MCTM channel 3 output function is almost the same as that of GPTM channel 3 except for the break function.

The channel outputs, CHxO and CHxNO, are referenced to the CHxOREF signal. These channel outputs generate a wide variety of wide waveforms according to the configuration values of corresponding control bits, as shown by the dashed box in the diagram.

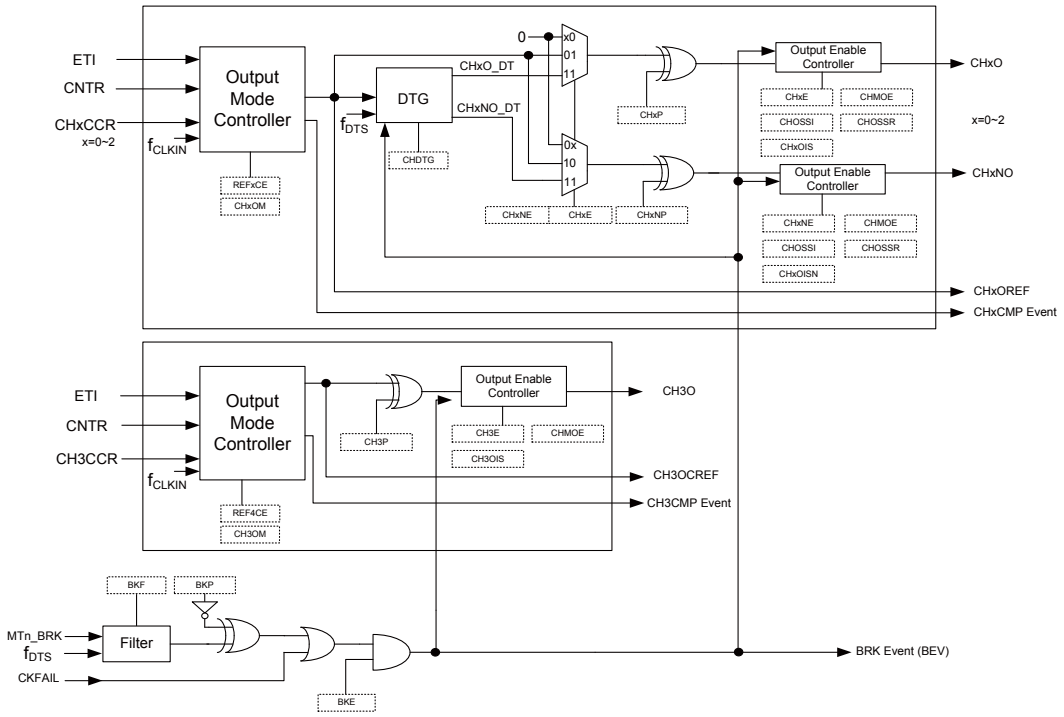


Figure 87. Output Stage Block Diagram

Channel Output Reference Signal

When the MCTM is used in the compare match output mode, the CHxOREF signal (Channel x Output Reference signal) is defined by the CHxOM bits setup. The CHxOREF signal has several types of output function which defines what happens to the output when the counter value matches the contents of the CHxCCR register. In addition to the low, high and toggle CHxOREF output types, there are also PWM mode 1 and PWM mode 2 outputs. In these modes, the CHxOREF signal level is changed according to the count direction and the relationship between the counter value and the CHxCCR content. There are also two modes which will force the output into an inactive or active state irrespective of the CHxCCR content or counter values. With regard to a more detailed description refer to the relative bits definition.

The accompanying table shows a summary of the output type setup.

Table 33. Compare Match Output Setup

CHxOM value	Compare Match Level
0x00	No change
0x01	Clear Output to 0
0x02	Set Output to 1
0x03	Toggle Output
0x04	Force Inactive Level
0x05	Force Active Level
0x06	PWM Mode 1
0x07	PWM Mode 2

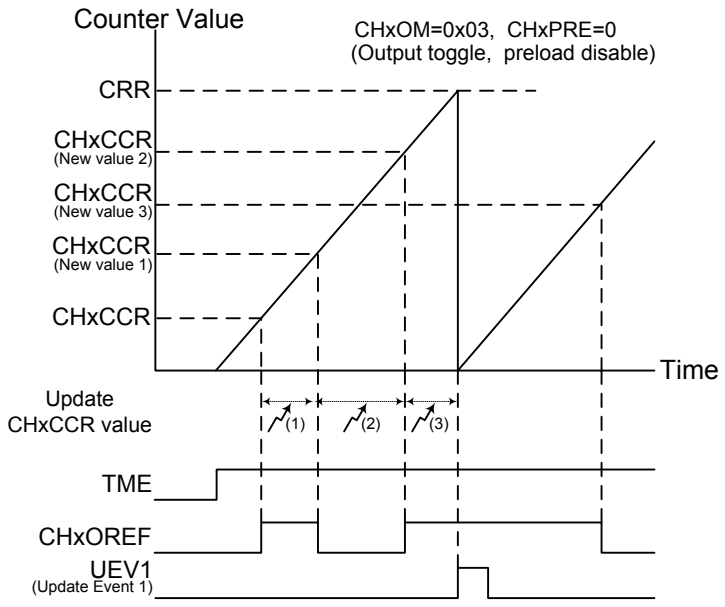


Figure 88. Toggle Mode Channel Output Reference Signal – CHxPRE=0

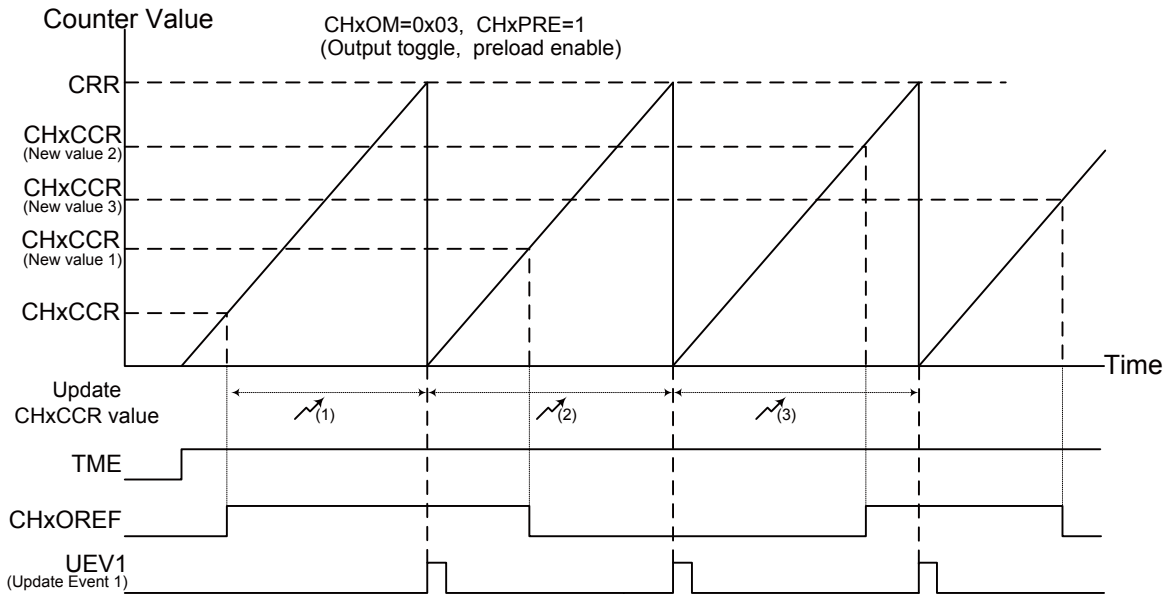


Figure 89. Toggle Mode Channel Output Reference Signal – CHxPRE=1

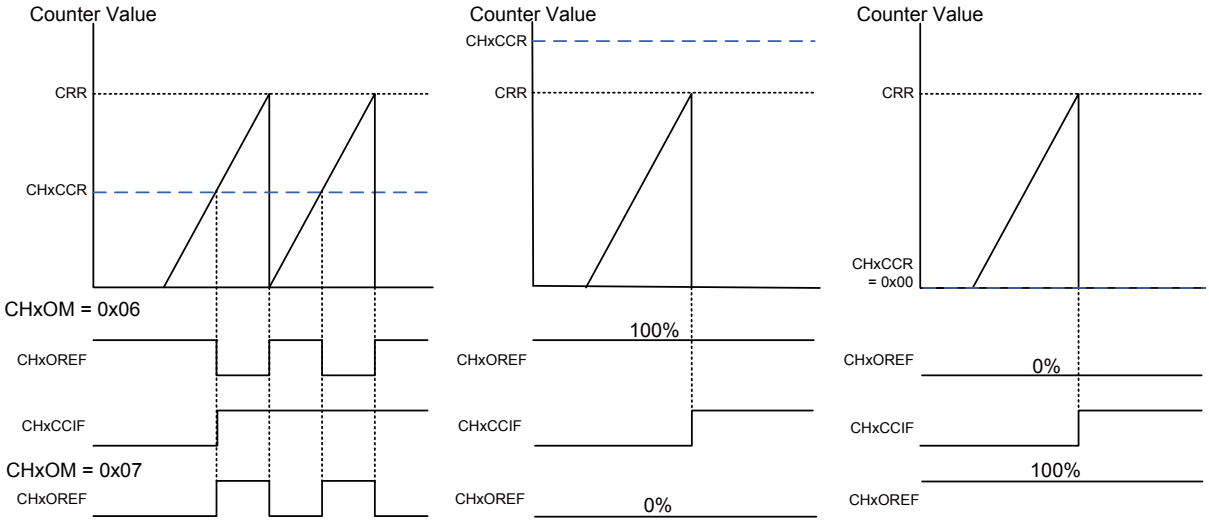


Figure 90. PWM Mode Channel Output Reference Signal and Counter in Up-counting Mode

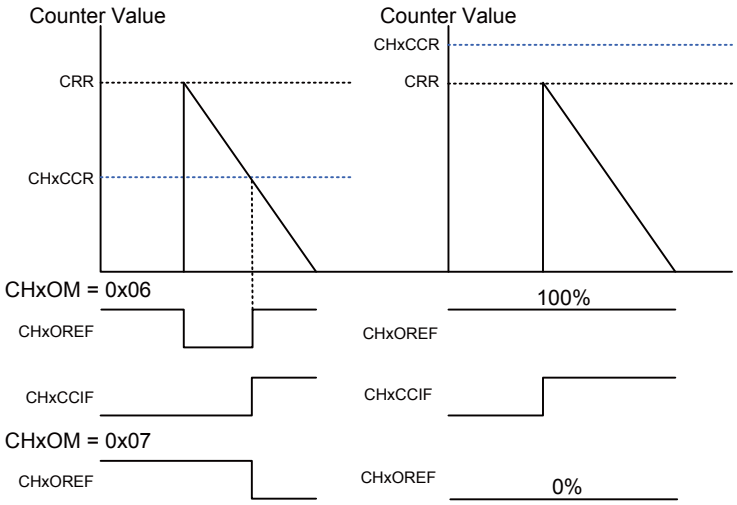


Figure 91. PWM Mode Channel Output Reference Signal and Counter in Down-counting Mode

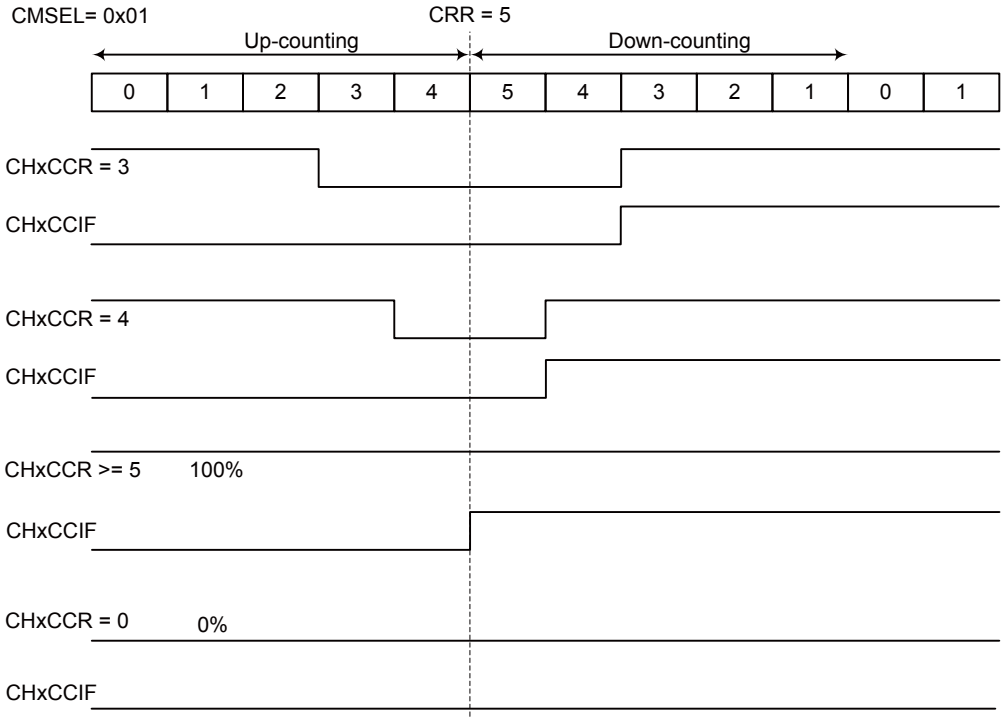


Figure 92. PWM Mode 1 Channel Output Reference Signal and Counter in Center-aligned Counting Mode

Dead Time Generator

An 8-bit dead time generator function is included for channels 0~2. The dead time insertion is enabled by setting both the CHxE and CHxNE bits. The relationship between the CHxO and CHxNO signals with respect to the CHxOREF signal is as follows:

- The CHxO signal is the same as the CHxOREF signal except for the rising edge which is delayed with a dead time relative to the reference signal rising edge
- The CHxNO is the opposite of the CHxOREF signal except for the rising edge which is delayed with a dead time relative to the reference signal falling edge

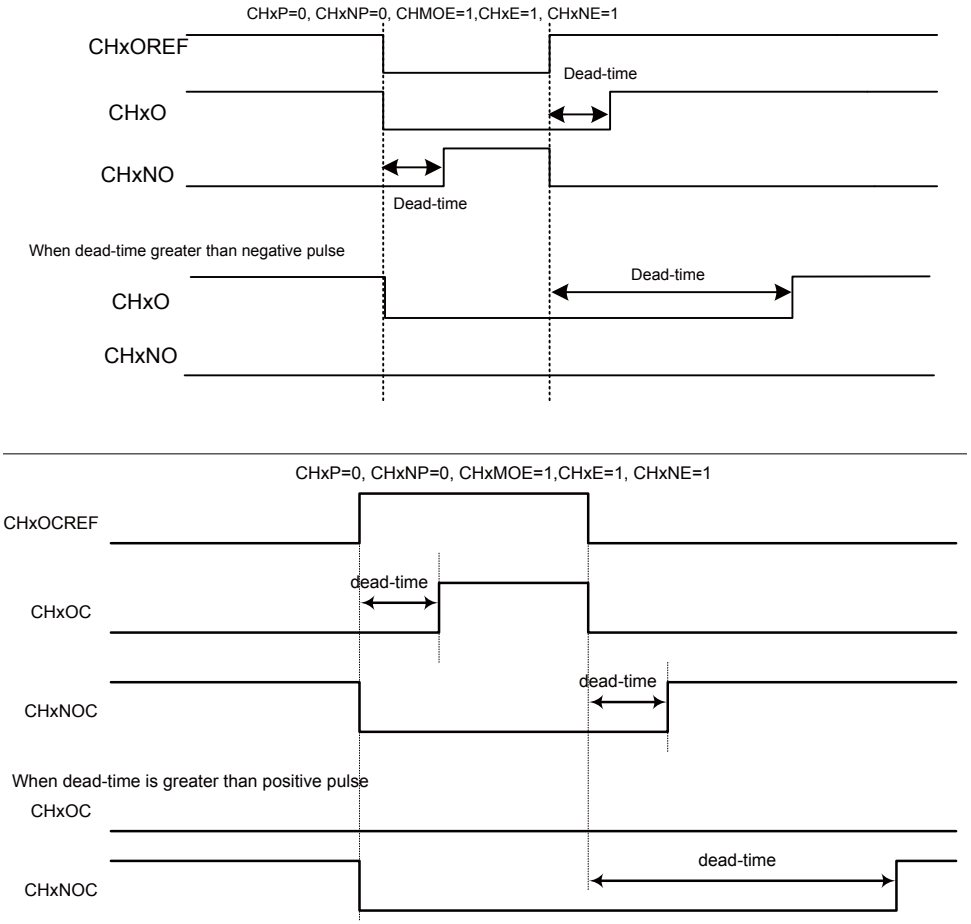


Figure 93. Dead-time Insertion Performed for Complementary Outputs

If the delay is greater than the width of the active output of CHxO or CHxNO, then the corresponding PWM pulses will not be generated.

Break Function

The MCTM includes a break function. When the MTn_BRK input has an active level or the Clock Monitor Circuitry detects a clock failure event, a break event will be generated if the break function is enabled. Meanwhile, each channel output will be forced to a reset state, an inactive or idle state. Moreover, a break event can also be generated by the software asserting the BRKG bit in the EVGR register even if the break function is disabled.

The MTn_BRK input signal can be enabled by setting the BKE bit in the CHBRKCTR register. The break input polarity can be selected by setting the BKP bit in CHBRKCTR register. The BKE and BKP bits can be modified at the same time.

The digital filters are embedded in the input stage and clock controller block for the break signal. The input filter of the MT_BRK signal can be enabled by setting the BKF bits in the CHBRKCTR register. The digital filter is an N-event counter where N refers to how many valid transitions are necessary to output a filtered signal.

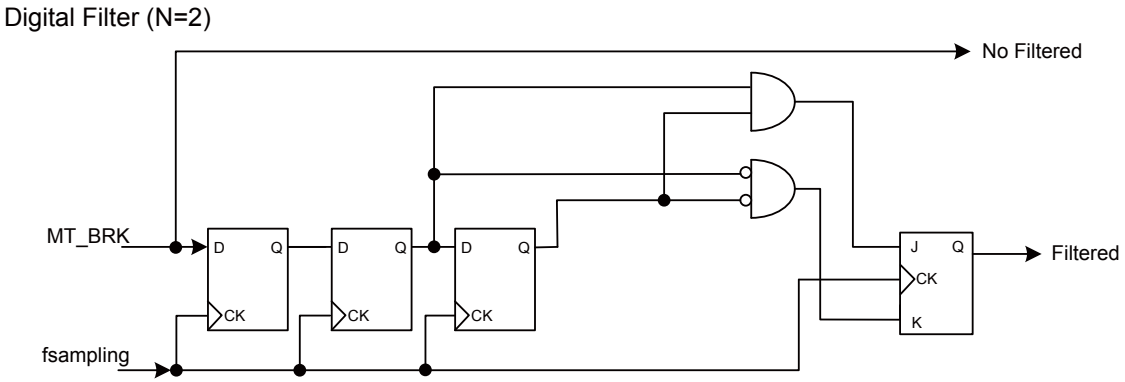


Figure 94. MT_BRK Pin Digital Filter Diagram with N=2

When using the break function, the channel output enable signals and output levels are changed depending on several control bits which include the CHMOE, CHOSSI, CHOSSR, CHxOIS and CHxOISN bits. Once a break event occurs, the output enable bit CHMOE will be cleared asynchronously. The break interrupt flag, BRKIF, will be set and then an interrupt will be generated if the break function interrupt is enabled by setting the BRKIE bit to 1. The channel output behavior is as described below:

- If complementary outputs are used, the channel outputs a level signal first which can be selected to be either a disable or inactive level, selected by configuring the CHOSSI bit in the CHBRKCTR register. After the dead-time duration, the outputs will be changed to the idle state. The idle state is determined by the CHxOIS/CHxOISN bits in the CHBRKCFR register.
- If complementary outputs are not used (Channel 3), the channel will output an idle state.

The main output enable control bit, CHMOE can not be set until the break event is cleared.

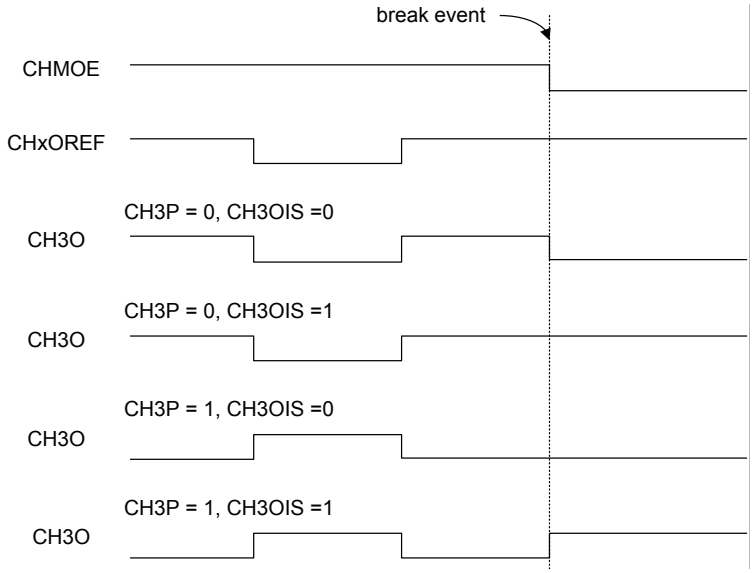


Figure 95. Channel 3 Output with a Break Event Occurrence

The accompanying diagram shows that the complementary output states when a break event occurs where the complementary outputs are enabled by setting both the CHxE and CHxNE bits to 1.

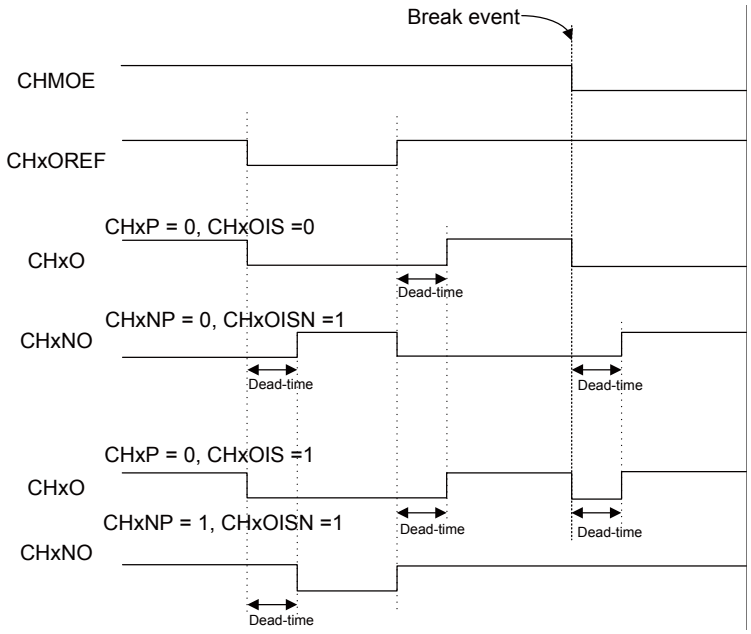


Figure 96. Channel 0~2 Complementary Outputs with a Break Event Occurrence

The accompanying diagram shows the output states in the case of the output being enabled by setting the CHxE bit to 1 and the complementary output being disabled by clearing the CHxNE to 0 when a break event occurs.

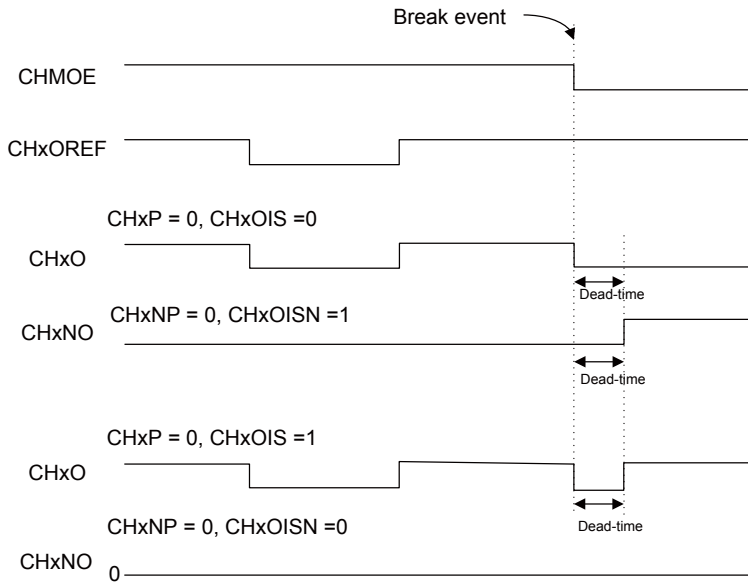


Figure 97. Channel 0~2 Only One Output Enabled when Fault Event Occurs

The CHxO and CHxNO complementary outputs should not be set to an active level at the same time. The hardware will protect the MCTM circuitry to force only one channel output to be in the active state.

Example: Both CHxOIS and CHxOISN are set to active levels after a break event; only the CHxO waveform is generated.

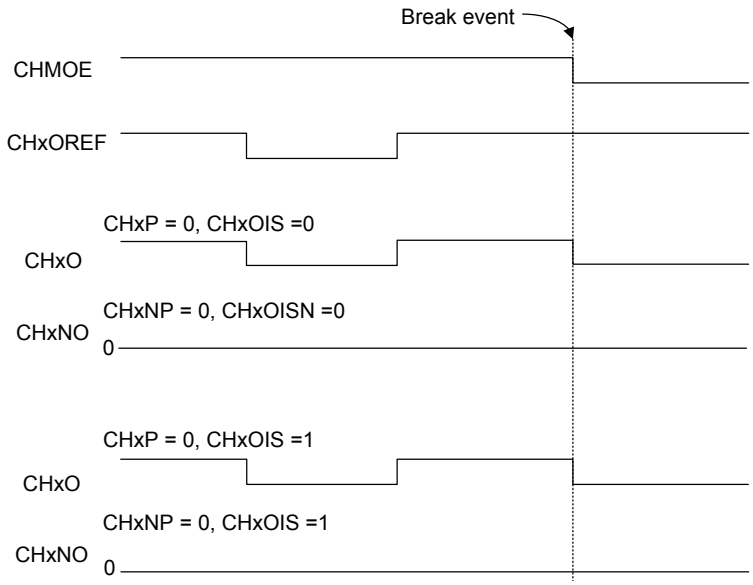


Figure 98. Hardware Protection When Both CHxO and CHxNO Are in Active Condition

CHMOE can be set automatically by update event 1 if the automatic output enable function is enabled by setting the CHAOE bit in the CHBRKCTR register to 1.

Channel Complementary Output with Break Function

The Channel complementary outputs, CHxO and CHxNO, are enabled by a combination of the CHxE, CHxNE, CHMOE, CHOSSR, CHOSSI control bits.

Table 34. Output Control Bits for Complementary Output with a Break Event Occurrence

Control bit					Output status	
CHMOE	CHOSSI	CHOSSR	CHxE	CHxNE	MT_CHx Pin output state	MT_CHxN Pin output state
1 (Run)	x	0	0	0	Output disabled – floating – not driven by the timer MT_CHx(Note 1)=floating MT_CHx_OEN(Note 2)=1	Output disabled – floating – not driven by the timer MT_CHxN=floating MT_CHxN_OEN=1
		0	0	1	Output disable – floating – not driven by the timer MT_CHx_OEN=1	Output enbaled MT_CHxN=CHx_OREF xor CHxNP MT_CHxN_OEN=0
		0	1	0	Output enabled MT_CHx=CHx_OREF xor CHxP MT_CHx_OEN=0	Output disabled – floating – not driven by the timer MT_CHxN=floating MT_CHxN_OEN=1
		0	1	1	Output enabled MT_CHx=CHx_OREF xor CHxP + dead-time MT_CHx_OEN=0	Output enabled MT_CHxN=not CHx_OREF xor CHxNP + dead-time MT_CHxN_OEN=0
		1	0	0	Output disabled – floating – not driven by the timer MT_CHx=floating MT_CHx_OEN=1	Output disabled – floating – not driven by the timer MT_CHxN=floating MT_CHxN_OEN=1
		1	0	1	Off-State MT_CHx=CHxP MT_CHx_OEN=0	Output enabled MT_CHxN=CHx_OREF xor CHxNP MT_CHxN_OEN=0
		1	1	0	Output enbaled MT_CHx=CHx_OCREF xor CHxP MT_CHx_OEN=0	Off-State MT_CHxN=CHxNP MT_CHxN_OEN=0
		1	1	1	Output enabled MT_CHx=CHx_OREF xor CHxP + dead-time MT_CHx_OEN=0	Output enabled MT_CHxN=not CHx_OREF xor CHxNP + dead-time MT_CHxN_OEN=0
0 (Idle)	0	x	0	0	Output disabled – floating MT_CHx=floating, MT_CHxN=floating MT_CHx_OEN=1, MT_CHxN_OEN=1	
	0		0	1		
	0		1	0		
	0		1	1		
	1		0	0		
	1		0	1	Before dead-time: Off state MT_CHx=CHxP, MT_CHxN=CHxNP MT_CHx_OEN=0, MT_CHxN_OEN=0 After dead-time: Output enabled MT_CHx=CHxOIS, MT_CHxN=CHxOISN MT_CHx_OEN=0, MT_CHxN_OEN=0	
	1		1	0		
	1		1	1		

Note: 1. The MT_CHx pin is the MCTM I/O Pin.

2. The MT_CHx_OEN and MT_CHxN_OEN signals are the MCTM I/O pin output enable combinational logic control signals which are active low.

Update Management

The update events are categorised into two different types which are the update event 1, UEV1, and update event 2, UEV2. The update event 1 is used to update the CRR, the PSCR and the CHxCCR values from the actual registers to the corresponding shadow registers. An update event 1 occurs when the counter overflows or underflows, the UEV1G bit is set or the slave restart mode is triggered. The update event 2 is used to update the CHxE, CHxNE and CHxOM control bits. An update event 2 is generated when a rising edge on the STI occurs or the corresponding software update control bit is set.

Update Event 1

The UEV1DIS bit in the CNTCFR register can determine whether an update event 1 occurs or not. When the update event 1 occurs, the corresponding update event interrupt will be generated depending upon whether the update event 1 interrupt generation function is enabled or not by configuring the UGDIS bit in the CNTCFR register. For a more detailed description, refer to the UEV1DIS and UGDIS bit definition in the CNTCFR register.

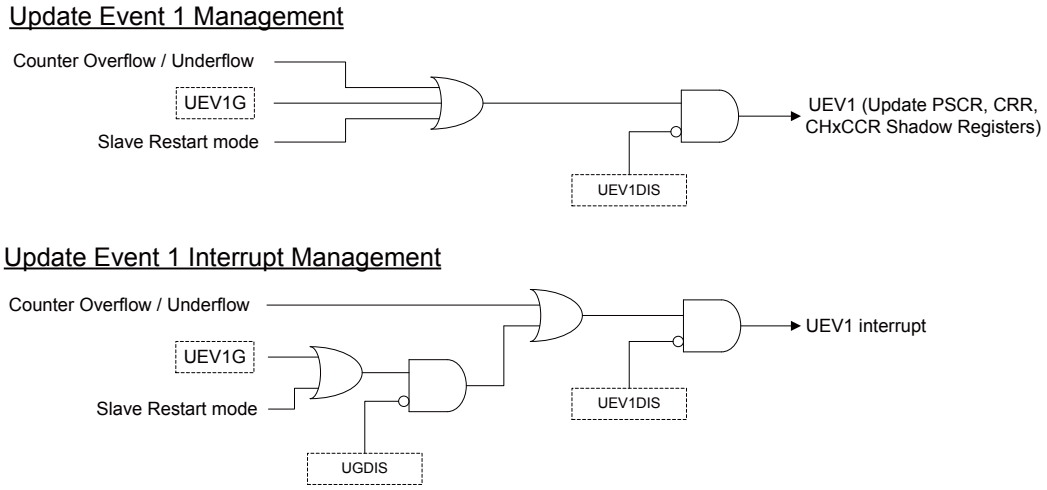


Figure 99. Update Event 1 Setup Diagram

Update Event 2

The CHxE, CHxNE, CHxOM control bits for the complementary outputs can be preloaded by setting the COMPRE bit in the CTR register. Here the shadow bits of the CHxE, CHxNE, CHxOM will be updated when an update event 2 occurs.

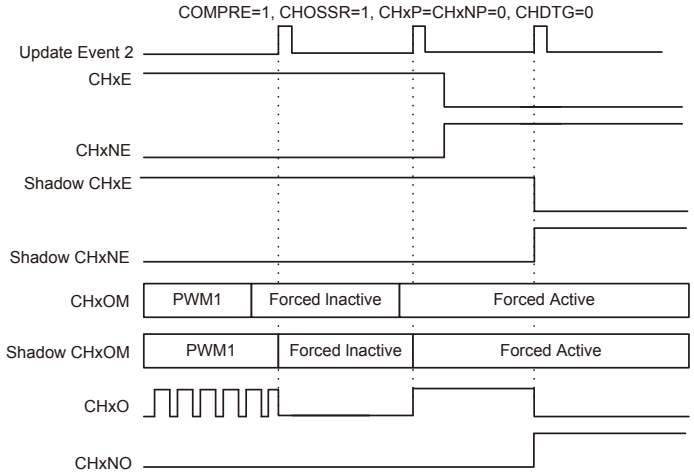


Figure 100. CHxE, CHxNE and CHxOM Updated by Update Event 2

An update event 2 can be generated by setting the software update bit, UEV2G, in the EVGR register or by the rising edge of the STI signal if the COMUS bit is set in the CTR register.

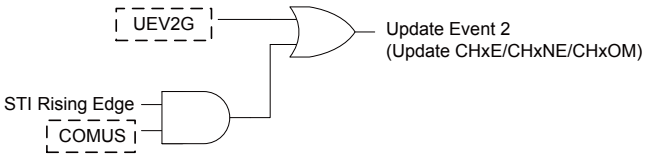


Figure 101. Update Event 2 Setup Diagram

Quadrature Decoder

The Quadrature Decoder function uses two quadrantal inputs TI0 and TI1 derived from the MTx_CH0 and MTx_CH1 pins respectively which interact to generate the counter value. The DIR bit is modified by hardware automatically during each input source transition. The counter is countering on TI0 edges only, TI1 edges only or both TI0 and TI1 edges. The selection is made by setting the SMSEL field to 0x01, 0x02 or 0x03. The mechanism for changing the counter direction is shown in the following table. The Quadrature decoder can be regarded as an external clock with a directional selection. This means that the counter counts continuously in the interval between 0 and the counter-reload value. The application program must therefore configure the CRR register before the counter starts to count.

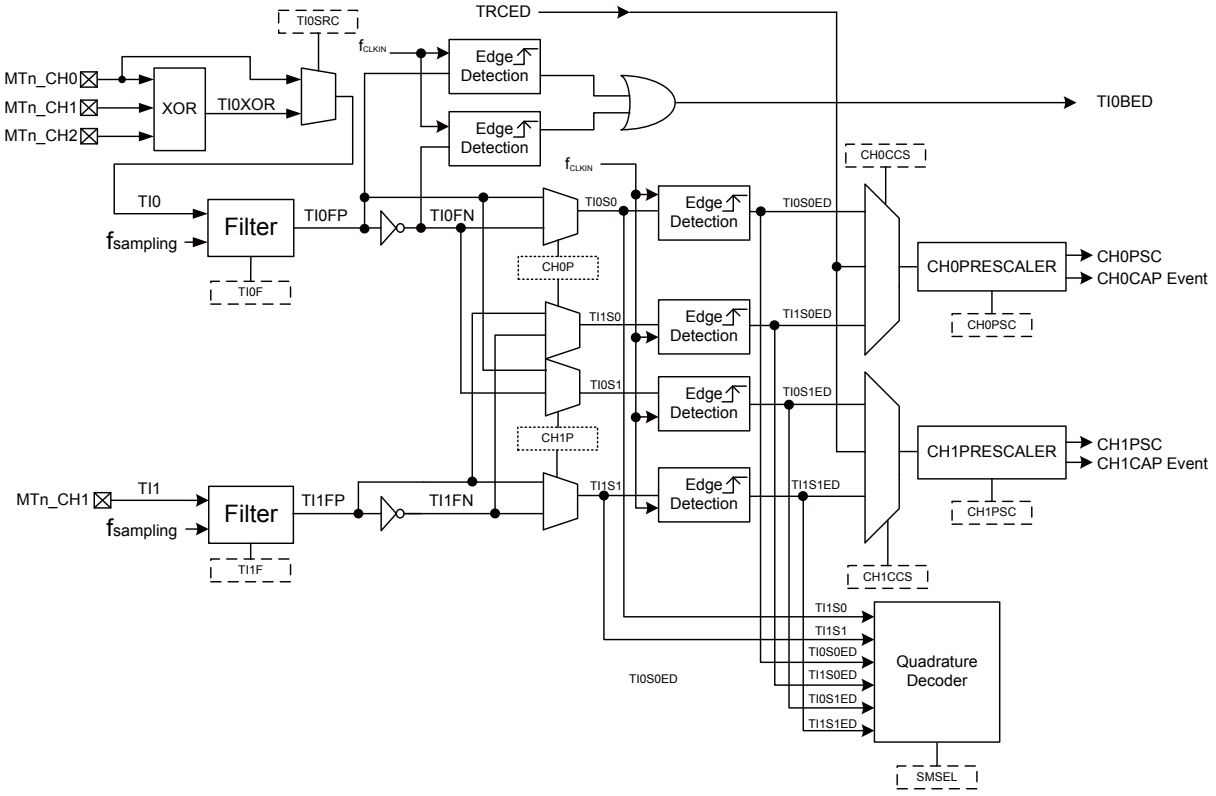


Figure 102. Input Stage and Quadature Decoder Block Diagram

Table 35. Counting Direction and Encoding Signals

Counting mode	Level	TI0S0		TI1S1	
		Rising	Falling	Rising	Falling
Counting on TI0 only (SMSEL=0x01)	TI1S1=High	Down	Up	—	—
	TI1S1=Low	Up	Down	—	—
Counting on TI1 only (SMSEL=0x02)	TI0S0=High	—	—	Up	Down
	TI0S0=Low	—	—	Down	Up
Counting on TI0 and TI1 (SMSEL=0x03)	TI1S1=High	Down	Up	X	X
	TI1S1=Low	Up	Down	X	X
	TI0S0=High	X	X	Up	Down
	TI0S0=Low	X	X	Down	Up

NOTE: "—" → means "no counting"; "X" → impossible

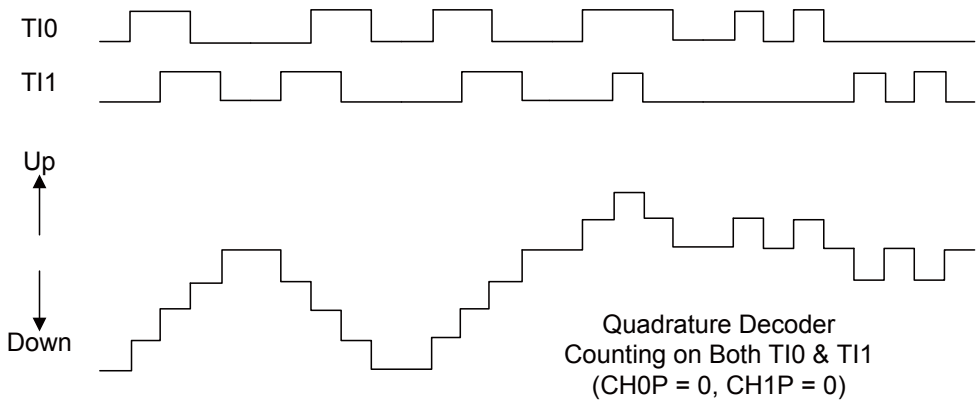


Figure 103. Both TI0 and TI1 Quadrature Decoder Counting

Digital Filter

The digital filters are embedded in the input stage and clock controller block for the MTn_CH0~MTn_CH3 and MTn_ETI pins. The digital filter in the MCTM is an N-event counter where N refers to how many valid transitions are necessary to output a filtered signal. The N value can be 0, 2, 4, 5, 6 or 8 according to the selection for each filter.

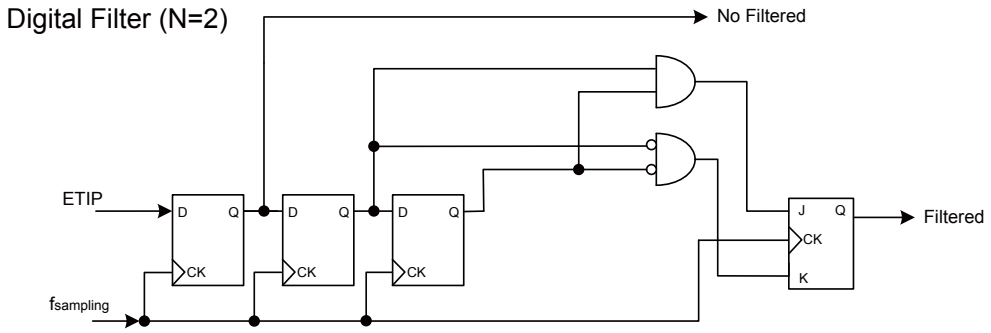


Figure 104. MTn_ETI Pin Digital Filter Diagram with N=2

Clearing CHxOREF when ETIF is high

The CHxOREF signal can be forced to 0 when the ETIF signal is set to a high level by setting the REFxCE bit to 1 in the CHxOCFR register. The CHxOREF signal will not return to its active level until the next update event 1 occurs.

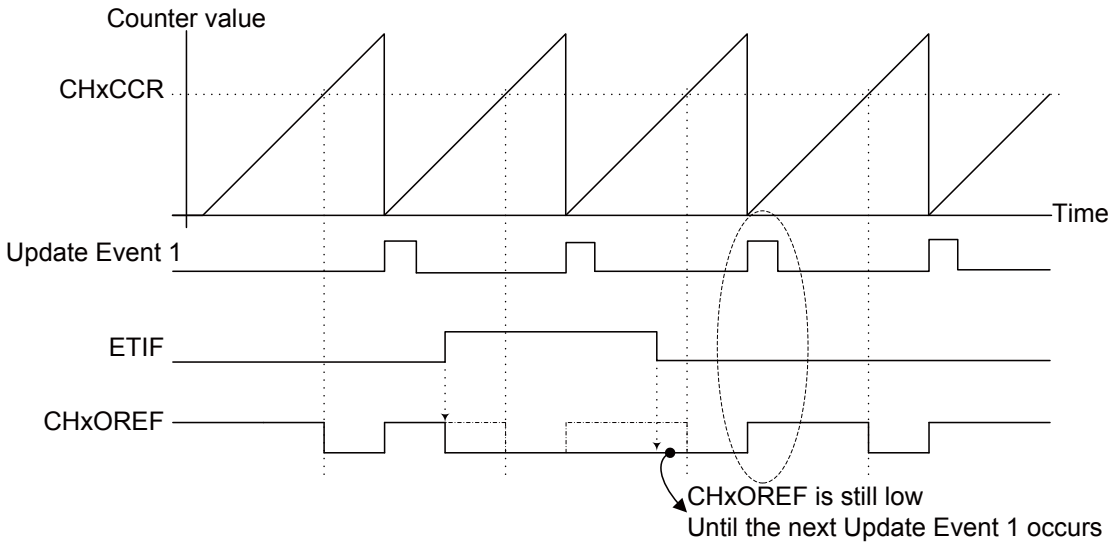


Figure 105. Clearing CHxOREF by ETIF

Single Pulse Mode

Once the timer is set to operate in the single pulse mode, it is not necessary to set the timer enable bit TME in the CTR register to 1 to enable the counter. The trigger to generate a pulse can be sourced from the STI signal rising edge or by setting the TME bit to 1 using software. Setting the TME bit to 1 or a trigger from the STI signal rising edge can generate a pulse and then keep the TME bit at a high state until the update event 1 occurs or the TME bit is cleared to 0 by software. If the TME bit is cleared to 0 using software, the counter will be stopped and its value held. If the TME bit is automatically cleared to 0 by a hardware update event 1, the counter will be reinitialised.

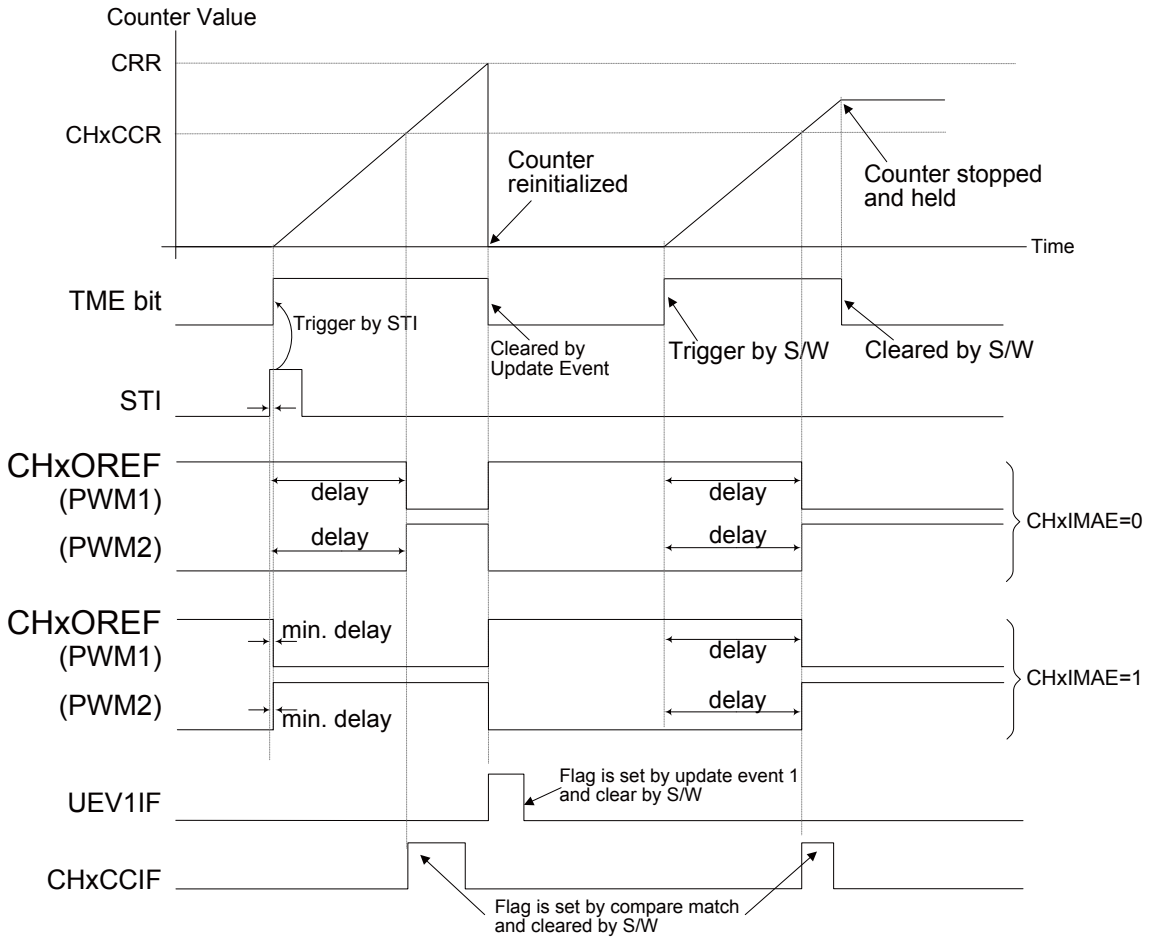


Figure 106. Single Pulse Mode

In the Single Pulse mode, the STI active edge which sets the TME bit to 1 will enable the counter. However, there exist several clock delays to perform the comparison result between the counter value and the CHxCCR value. In order to reduce the delay to a minimum value, users can set the CHxIMAE bit in each CHxOCFR register. After a STI rising edge trigger occurs in the single pulse mode, the CHxOREF signal will immediately be forced to the state to which the CHxOREF signal will change to as the compare match event occurs without taking the comparison result into account. The CHxIMAE bit is available only when the output channel is configured to operate in the PWM1 or PWM2 output mode and the trigger source is derived from the STI signal.

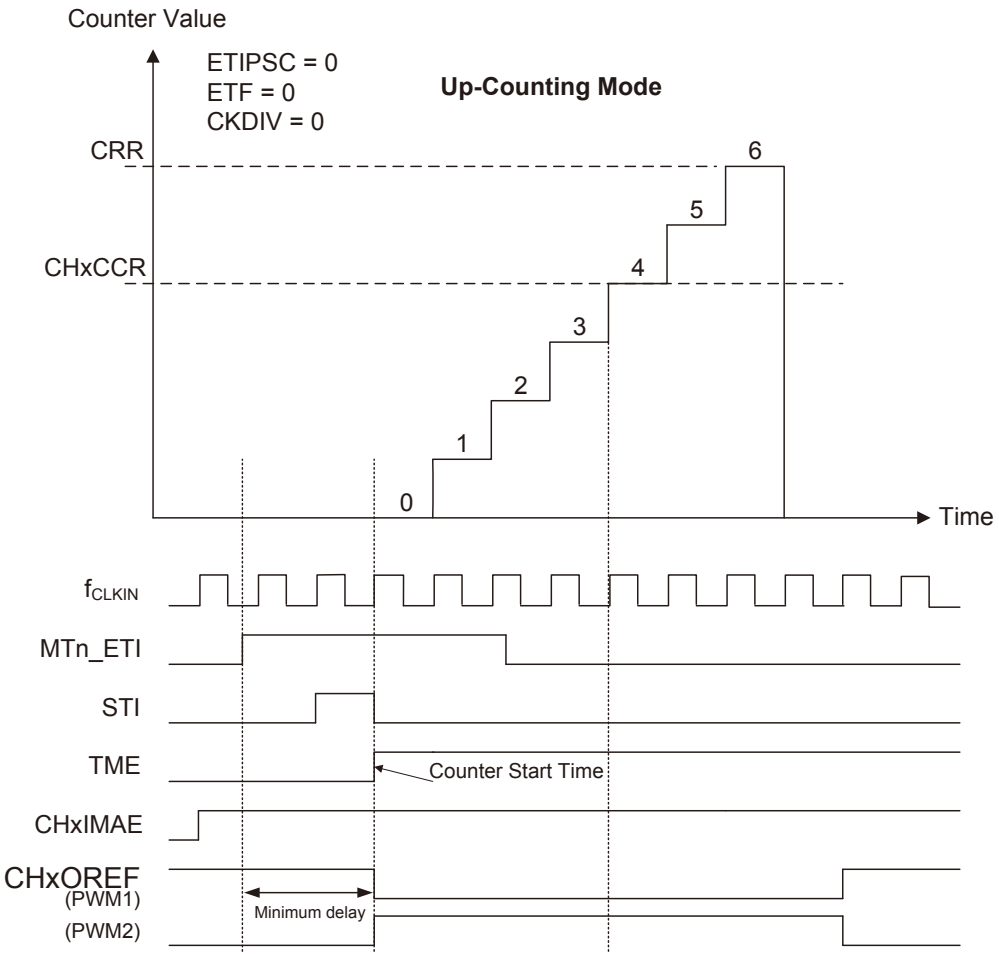


Figure 107. Immediate Active Mode Minimum Delay

Timer Interconnection

The timers can be internally connected together for timer chaining or synchronization. This can be implemented by configuring one timer to operate in the Master mode while configuring another timer to be in the Slave mode. The following figures present several examples of trigger selection for the master and slave modes.

Using one timer to trigger another timer to start or stop counting.

- Configure MCTM0 to be in the master mode and to send its channel 0 Output Reference signal CH0OREF as a trigger output (MMSEL=0x04)
- Configure the MCTM0 CH0OREF waveform
- Configure the GPTM0 to receive its input trigger source from the MCTM0 trigger output (TRSEL=0x0A)
- Configure GPTM0 to operate in the pause mode (SMSEL=0x05)
- Enable GPTM0 by writing 1 to the TME bit
- Enable MCTM0 by writing 1 to the TME bit

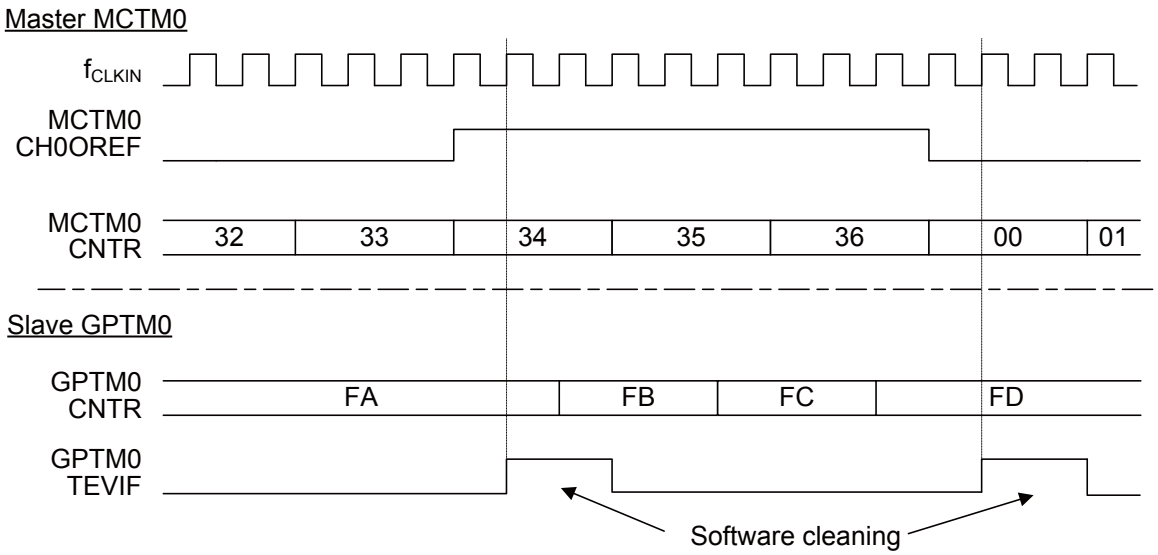


Figure 108. Pausing GPTM0 using the MCTM0 CH0OREF Signal

Using one timer to trigger another timer to start counting.

- Configure MCTM0 to operate in the master mode and to send its Update Event UEV as the trigger output (MMSEL=0x02)
- Configure the MCTM0 period by setting the CHxCRR register
- Configure GPTM0 to get the input trigger source from the MCTM0 trigger output (TRSEL=0x0A)
- Configure GPTM0 to be in the slave trigger mode (SMSEL=0x06)
- Start MCTM0 by writing 1 to the TME bit

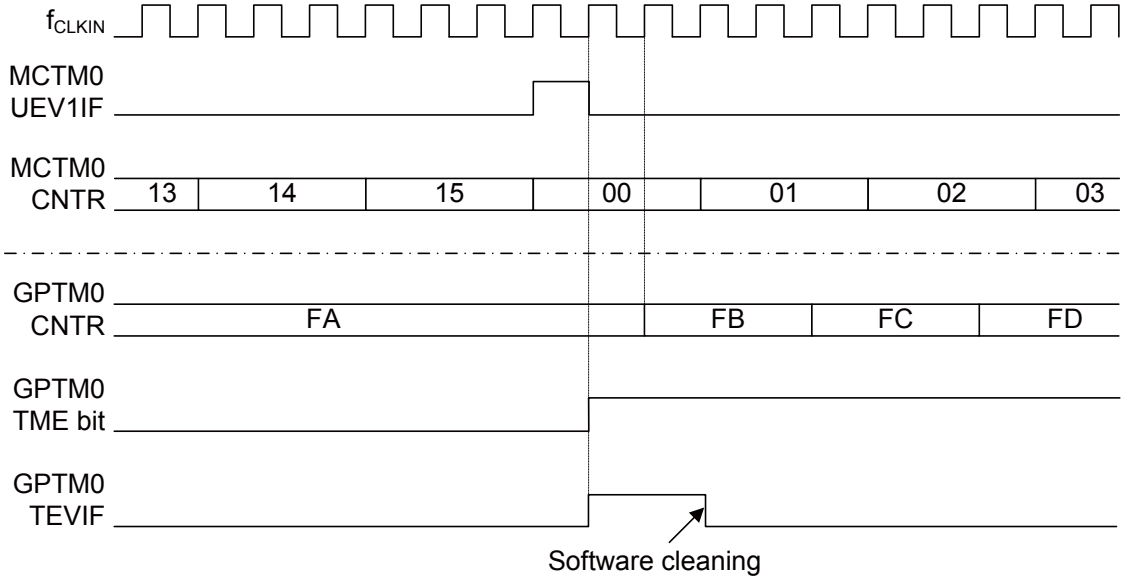


Figure 109. Triggering GPTM0 with MCTM0 Update Event 1

Starting two timers synchronously in response to an external trigger.

- Configure MCTM0 to operate in the master mode to send its enable signal as a trigger output (MMSEL=0x01)
- Configure MCTM0 slave mode to receive its input trigger source from MTn_CH0 pin (TRSEL=0x01)
- Configure MCTM0 to be in the slave trigger mode (SMSEL=0x06)
- Enable the MCTM0 master timer synchronisation function by setting the TSE bit in the MDCFR register to 1 to synchronise the slave timer
- Configure GPTM0 to receive its input trigger source from the MCTM0 trigger output (TRSEL=0x0A)
- Configure GPTM0 to be in the slave trigger mode (SMSEL=0x06)

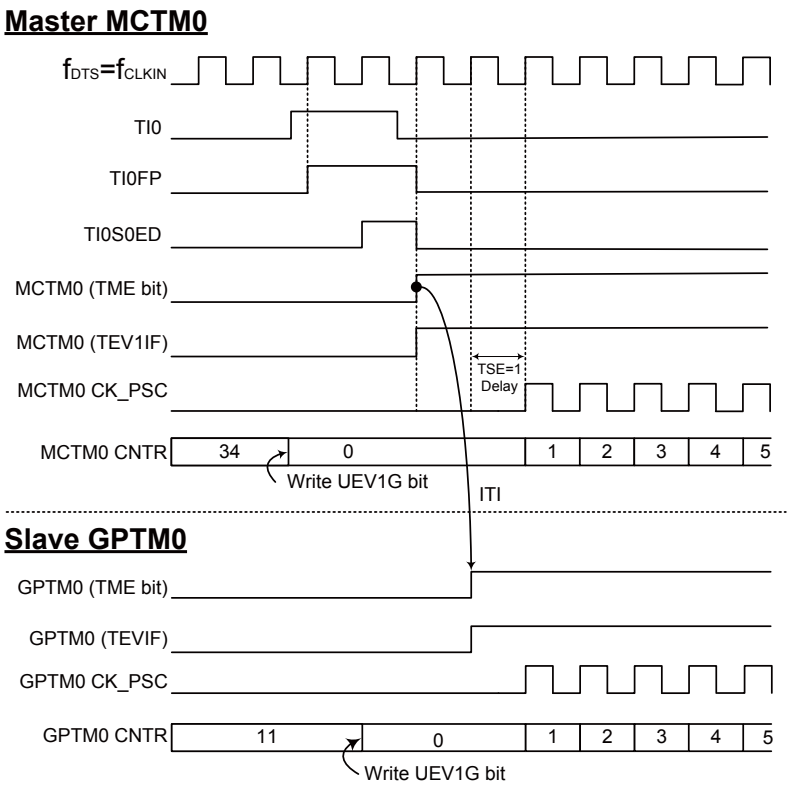


Figure 110. Trigger MCTM0 and GPTM0 with the MCTM0 CH0 Input

Using one timer as a hall sensor interface to trigger another timer with update event 2.

GPTM0:

- Configure channel 0 to choose an input XOR function (TI0SRC=1)
- Configure channel 0 to be in the input capture mode and TRCED as capture source (CH0CCS=0x03) and Enable channel 0 (CH0E=1)
- Configure the UEVG bit as the source of MTO (MMSEL=0x00)
- Configure TI0BED to be connected to STI (TRSEL=0x08)
- Configure the counter to be in the slave restart mode (SMSEL=0x04)
- Enable GPTM0 (TME=1)

MCTM0:

- Select GPTM0 MTO to be the STI source of MCTM (TRSEL=0x0A)
- Enable the CHxE, CHxNE and CHxOM preload function (COMPRE=1)
- Select the rising edge on STI to generate an update event 2 (COMUS=1)
- Enable the update event 2 interrupt (UEV2IE=1)
- In the update event 2 ISR: write CHxE, CHxNE and CHxOM register for the next step

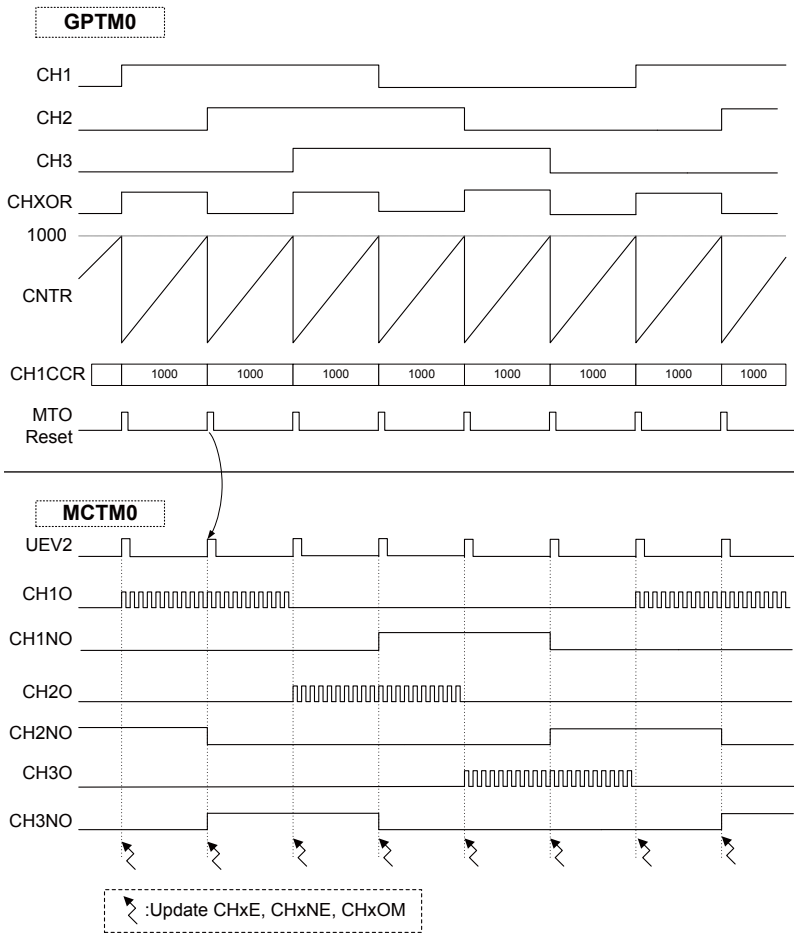


Figure 111. CH1XOR Input as Hall Sensor Interface

Trigger ADC Start

To interconnect to the Analog-to-Digital Converter, the MCTM can output the MTO signal or the channel output MTn_CHx (x=0~3) signal to be used as an Analog-to-Digital Converter input trigger signal.

Lock Level Table

In addition to the break input and output management, a write protection has been internally implemented in the break circuitry to safeguard the application. Users can choose one protection level selected by the LOCKLV bits to protect the relative control bits of the registers. The LOCKLV bits can only be written once after an MCTM reset or system reset. Then the protected bits will be locked and can not be changed anymore except by the MCTM reset or when the system is reset.

Table 36. Lock Level Table

Lock Configuration	Protected Bits					
Lock Level 1 (LOCKLV='01')	CHDTG	CHxOIS	CHxOISN	BKE	BKP	CHAOE
Lock Level 2 (LOCKLV='10')	CHDTG	CHxOIS	CHxOISN	BKE	BKP	CHAOE
	CHxP	CHxNP	CHOSSI	CHOSSR		
Lock Level 3 (LOCKLV='11')	CHDTG	CHxOIS	CHxOISN	BKE	BKP	CHAOE
	CHxP	CHxNP	CHOSSI	CHOSSR		
	CHxPRE	CHxOM				

PDMA Request

The MCTM has a PDMA data transfer interface. There are certain events which can generate PDMA requests if the corresponding enable control bits are set to 1 to enable the PDMA access. These events are the MCTM update events, trigger event and channel capture/compare events. When the PDMA request is generated from the MCTM channel, it can be derived from the channel capture/compare event or the MCTM update event 1 selected by the channel PDMA selection bit, CHCCDS, for all channels. For more detailed PDMA configuring information, refer to the corresponding section in the PDMA chapter.

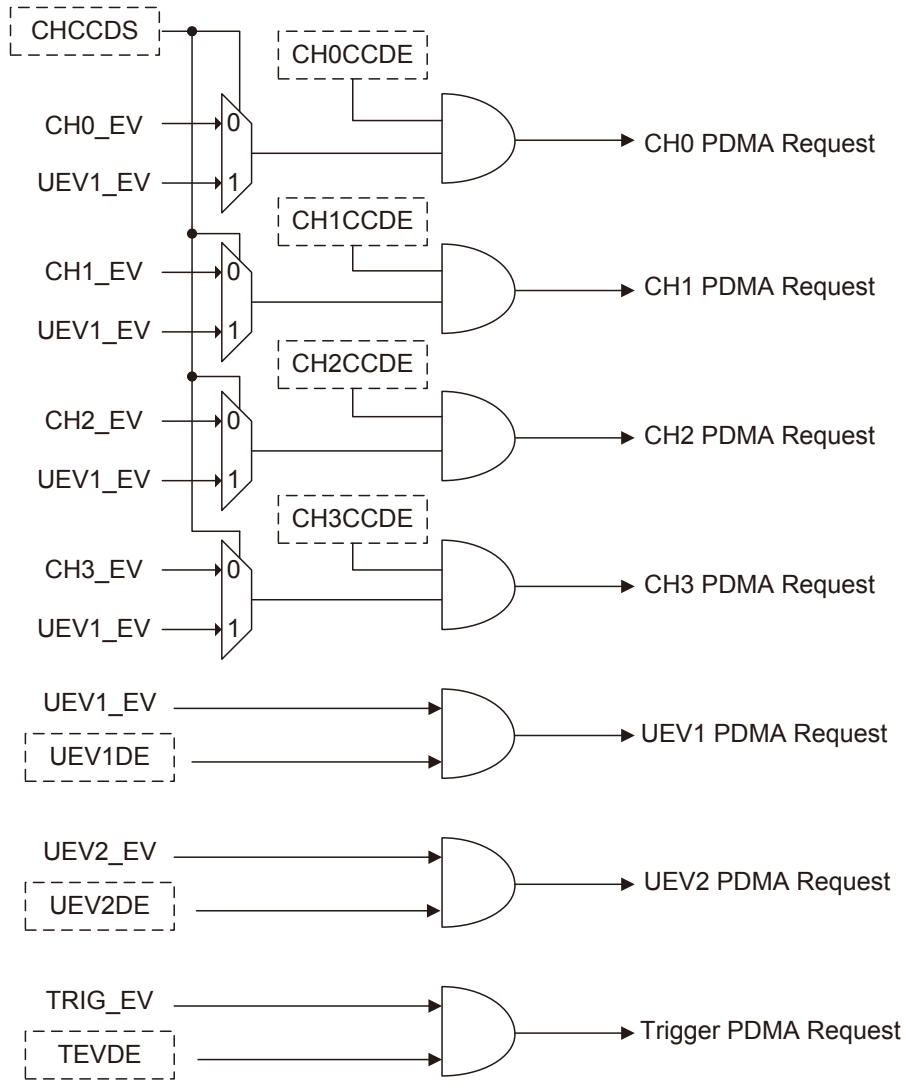


Figure 112. MCTM PDMA Mapping Diagram

Register Map

The following table shows the MCTM registers and reset values.

Table 37. MCTM Register Map

Register	Offset	Description	Reset Value
MCTM0 Base Address=0x4002_C000			
CNTCFR	0x000	Timer Counter Configuration Register	0x0000_0000
MDCFR	0x004	Timer Mode Configuration Register	0x0000_0000
TRCFR	0x008	Timer Trigger Configuration Register	0x0000_0000
CTR	0x010	Timer Control Register	0x0000_0000
CH0ICFR	0x020	Channel 0 Input Configuration Register	0x0000_0000
CH1ICFR	0x024	Channel 1 Input Configuration Register	0x0000_0000
CH2ICFR	0x028	Channel 2 Input Configuration Register	0x0000_0000
CH3ICFR	0x02C	Channel 3 Input Configuration Register	0x0000_0000
CH0OCFR	0x040	Channel 0 Output Configuration Register	0x0000_0000
CH1OCFR	0x044	Channel 1 Output Configuration Register	0x0000_0000
CH2OCFR	0x048	Channel 2 Output Configuration Register	0x0000_0000
CH3OCFR	0x04C	Channel 3 Output Configuration Register	0x0000_0000
CHCTR	0x050	Channel Control Register	0x0000_0000
CHPOLR	0x054	Channel Polarity Configuration Register	0x0000_0000
CHBRKCFR	0x06C	Channel Break Configuration Register	0x0000_0000
CHBRKCTR	0x070	Channel Break Control Register	0x0000_0000
DICTR	0x074	Timer PDMA/Interrupt Control Register	0x0000_0000
EVGR	0x078	Timer Event Generator Register	0x0000_0000
INTSR	0x07C	Timer Interrupt Status Register	0x0000_0000
CNTR	0x080	Timer Counter Register	0x0000_0000
PSCR	0x084	Timer Prescaler Register	0x0000_0000
CRR	0x088	Timer Counter Reload Register	0x0000_FFFF
REPR	0x08C	Timer Repetition Register	0x0000_0000
CH0CCR	0x090	Channel 0 Capture/Compare Register	0x0000_0000
CH1CCR	0x094	Channel 1 Capture/Compare Register	0x0000_0000
CH2CCR	0x098	Channel 2 Capture/Compare Register	0x0000_0000
CH3CCR	0x09C	Channel 3 Capture/Compare Register	0x0000_0000

Register Descriptions

Timer Counter Configuration Register – CNTCFR

This register specifies the MCTM counter configuration.

Offset: 0x000

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							DIR
Type/Reset								RW 0
	23	22	21	20	19	18	17	16
	Reserved							CMSEL
Type/Reset							RW 0	RW 0
	15	14	13	12	11	10	9	8
	Reserved							CKDIV
Type/Reset							RW 0	RW 0
	7	6	5	4	3	2	1	0
	Reserved						UGDIS	UEV1DIS
Type/Reset							RW 0	RW 0

Bits	Field	Descriptions
[24]	DIR	Counting Direction 0: Up-counting 1: Down-counting **Note:** This bit is read only when the Timer is configured to be in the center-aligned counting mode or when used as a Quadrature decoder.
[17:16]	CMSEL	Counter Mode Selection 00: Edge-aligned counting mode. Normal up-counting and down-counting available for this mode. Counting direction is defined by the DIR bit. 01: Center-aligned counting mode 1. The counter counts up and down alternatively. The compare match interrupt flag is set during the down-counting period. 10: Center-aligned counting mode 2. The counter counts up and down alternatively. The compare match interrupt flag is set during the up-counting period. 11: Center-aligned counting mode 3. The counter counts up and down alternatively. The compare match interrupt flag is set during the up-counting or down-counting period.

Bits	Field	Descriptions
[9:8]	CKDIV	Clock Division These two bits define the frequency ratio between the timer clock (f_{CLKIN}) and the dead-time clock (f_{DTS}). The dead-time clock is also used as the digital filter sampling clock. 00: $f_{DTS}=f_{CLKIN}$ 01: $f_{DTS}=f_{CLKIN}/2$ 10: $f_{DTS}=f_{CLKIN}/4$ 11: Reserved
[1]	UGDIS	Update event 1 interrupt generation disable control 0: Any of the following events will generate an update PDMA request or interrupt – Counter overflow/underflow – Setting the UEV1G bit – Update generation through the slave mode 1: Only counter overflow/underflow generates an update PDMA request or interrupt
[0]	UEV1DIS	Update event 1 Disable control 0: Enable the update event 1 request by one of following events – Counter overflow/underflow – Setting the UEV1G bit – Update generation through the slave mode 1: Disable the update event 1 – however the counter and the prescaler are reinitialised if the UEV1G bit is set or if a hardware restart is received from the slave mode

Timer Mode Configuration Register – MDCFR

This register specifies the MCTM master and slave mode selection and single pulse mode.

Offset: 0x004

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							SPMSET
Type/Reset								RW 0
	23	22	21	20	19	18	17	16
	Reserved					MMSEL		
Type/Reset						RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
	Reserved					SMSEL		
Type/Reset						RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	Reserved							TSE
Type/Reset								RW 0

Bits	Field	Descriptions
[24]	SPMSET	Single Pulse Mode Setting 0: Counter counts normally irrespective of whether a update event occurred or not 1: Counter stops counting at the next update event and then the TME bit is cleared by hardware

Bits	Field	Descriptions
[18:16]	MMSEL	Master Mode Selection Master mode selection is used to select the MTO signal source which is used to synchronise the other slave timer.

MMSEL [2:0]	Mode	Descriptions
000	Reset Mode	The MTO in the Reset mode is an output derived from one of the following cases: 1. Software setting UEV1G bit 2. Slave has trigger input when used in slave restart mode
001	Enable Mode	The Counter Enable signal is used as the trigger output.
010	Update Mode	The update event 1 is used as the trigger output according to one of the following cases when the UEV1DIS bit is cleared to 0: 1. Counter overflow/underflow 2. Software setting UEV1G 3. Slave has trigger input when used in slave restart mode
011	Capture/Compare Mode	When a Channel 0 capture or compare match event occurs, it will generate a positive pulse which is used as the master trigger output.
100	Compare output 0	The Channel 0 Output reference signal named CH0OREF is used as the trigger output.
101	Compare output 1	The Channel 1 Output reference signal named CH1OREF is used as the trigger output.
110	Compare output 2	The Channel 2 Output reference signal named CH2OREF is used as the trigger output.
111	Compare output 3	The Channel 3 Output reference signal named CH3OREF is used as the trigger output.

Bits	Field	Descriptions
[10:8]	SMSEL	Slave Mode Selection

SMSEL [2:0]	Mode	Descriptions
000	Disable mode	The prescaler is clocked directly by the internal clock.
001	Quadrature Decoder mode 1	The counter uses the clock pulses generated from the interaction between the TI0 and TI1 signals to drive the counter prescaler. A transition of the TI0 edge is used in this mode depending upon the TI1 level.
010	Quadrature Decoder mode 2	The counter uses the clock pulse generated from the interaction between the TI0 and TI1 signals to drive the counter prescaler. A transition of the TI1 edge is used in this mode depending upon the TI0 level.
011	Quadrature Decoder mode 3	The counter uses the clock pulse generated from the interaction between the TI0 and TI1 signals to drive the counter prescaler. A transition of one channel edge is used in the quadrature decoder mode 3 depending upon the other channel level.
100	Restart Mode	The counter value restarts from 0 or the CRR shadow register value depending upon the counting direction mode on the rising edge of the STI signal. The registers will also be updated.
101	Pause Mode	The counter starts to count when the selected trigger input STI is high. The counter stops counting on the instant, not being reset, when the STI signal changes its state to a low level. Both the counter start and stop control are determined by the STI signal.
110	Trigger Mode	The counter starts to count from the original value in the counter on the rising edge of the selected trigger input STI. Only the start of the counter is controlled.
111	STIED	The rising edge of the selected trigger signal STI will clock the counter.

[0]	TSE	Timer Synchronisation Enable 0: No action 1: Master timer (current timer) will generate a delay to synchronise its slave timer through the MTO signal

Timer Trigger Configuration Register – TRCFR

This register specifies the MCTM external clock setting and the trigger source selection.

Offset: 0x008

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							ECME
Type/Reset								RW 0
	23	22	21	20	19	18	17	16
	Reserved							ETIPOL
Type/Reset								RW 0
	15	14	13	12	11	10	9	8
	Reserved			ETIPSC			ETF	
Type/Reset			RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	Reserved				TRSEL			
Type/Reset					RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[24]	ECME	External Clock Mode Enable 0: External clock mode is disabled 1: External clock mode is enabled The following two settings have the same effect: 1. Setting the ECME bit to 1 2. Setting SMSEL=0x111 with STI connected to ETIF (TRSEL=0x011)
[16]	ETIPOL	External Trigger Polarity 0: MTn_ETI active at high level or rising edge 1: MTn_ETI active at low level or falling edge
[13:12]	ETIPSC	External Trigger Prescaler A prescaler can be enabled to reduce the ETIP frequency. 00: Prescaler OFF 01: ETIP frequency divided by 2 10: ETIP frequency divided by 4 11: ETIP frequency divided by 8

Bits	Field	Descriptions
[11:8]	ETF	External Trigger Filter These bits define the frequency divided ratio that is used to sample the MTn_ETI signal. The digital filter in the MCTM is an N-event counter where N means how many valid transitions are necessary to output a filtered signal. 0000: No filter, the sampling clock is f_{DTS} 0001: $f_{SAMPLING}=f_{CLKIN}$, N=2 0010: $f_{SAMPLING}=f_{CLKIN}$, N=4 0011: $f_{SAMPLING}=f_{CLKIN}$, N=8 0100: $f_{SAMPLING}=f_{DTS}/2$, N=6 0101: $f_{SAMPLING}=f_{DTS}/2$, N=8 0110: $f_{SAMPLING}=f_{DTS}/4$, N=6 0111: $f_{SAMPLING}=f_{DTS}/4$, N=8 1000: $f_{SAMPLING}=f_{DTS}/8$, N=6 1001: $f_{SAMPLING}=f_{DTS}/8$, N=8 1010: $f_{SAMPLING}=f_{DTS}/16$, N=5 1011: $f_{SAMPLING}=f_{DTS}/16$, N=6 1100: $f_{SAMPLING}=f_{DTS}/16$, N=8 1101: $f_{SAMPLING}=f_{DTS}/32$, N=5 1110: $f_{SAMPLING}=f_{DTS}/32$, N=6 1111: $f_{SAMPLING}=f_{DTS}/32$, N=8
[3:0]	TRSEL	Trigger Source Selection These bits are used to select the trigger input (STI) for counter synchronising. 0000: Software Trigger by setting the UEV1G bit 0001: Channel 0 filtered input – TI0S0 0010: Channel 1 filtered input – TI1S1 0011: External Trigger input – ETIF 1000: Channel 0 Edge Detector – TI0BED 1001: Internal Timing Module Trigger 0 – ITI0 1010: Internal Timing Module Trigger 1 – ITI1 1011: Internal Timing Module Trigger 2 – ITI2 Others: Default 0 **Note:** These bits must be updated only when they are not in use, i.e. the slave mode is disabled by setting the SMSEL field to 0x00.

Table 38. MCTM Internal Trigger Connection

Slave Timing Module	ITI0	ITI1	ITI2
MCTM0	Reserved	GPTM0	GPTM1

Timer Counter Register – CTR

This register specifies the timer enable bit (TME), CRR buffer enable bit (CRBE), Capture/compare control bit and Channel PDMA selection bit (CHCCDS).

Offset: 0x010

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							CHCCDS
Type/Reset								RW 0
	15	14	13	12	11	10	9	8
	Reserved						COMUS	COMPRE
Type/Reset							RW 0	RW 0
	7	6	5	4	3	2	1	0
	Reserved						CRBE	TME
Type/Reset							RW 0	RW 0

Bits	Field	Descriptions
[16]	CHCCDS	Channel Capture/Compare PDMA Selection 0: Channel PDMA request derived from the channel capture/compare event 1: Channel PDMA request derived from the update event 1
[9]	COMUS	Capture/Compare Control Update Selection 0: Updated by setting the UEV2G bit only 1: Updated by setting the UEV2G bit or when a STI signal rising edge occurs This bit is only available when the capture/compare preload function is enabled by setting the COMPRE bit to 1.
[8]	COMPRE	Capture/Compare Preloaded Enable Control 0: CHxE, CHxNE and CHxOM bits are not preloaded 1: CHxE, CHxNE and CHxOM bits are preloaded If this bit is set to 1, the corresponding capture/compare control bits including the CHxE, CHxNE and CHxOM bits will be updated when the update event 2 occurs.
[1]	CRBE	Counter-Reload register Buffer Enable 0: Counter reload register can be updated immediately 1: Counter reload register can not be updated until the update event occurs
[0]	TME	Timer Enable bit 0: MCTM off 1: MCTM on – MCTM functions normally When the TME bit is cleared to 0, the counter is stopped and the MCTM consumes no power in any operational mode except for the single pulse mode and the slave trigger mode. In these two modes the TME bit can automatically be set to 1 by hardware which permits all the MCTM registers to function normally.

Channel 0 Input Configuration Register – CH0ICFR

This register specifies the channel 0 input mode configuration.

Offset: 0x020

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	TI0SRC	Reserved						
Type/Reset	RW 0							
	23	22	21	20	19	18	17	16
	Reserved				CH0PSC		CH0CCS	
Type/Reset					RW 0	RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved				TI0F			
Type/Reset					RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[31]	TI0SRC	Channel 0 Input Source TI0 Selection 0: The MTn_CH0 pin is connected to the channel 0 input TI0 1: The XOR operation output of the MTn_CH0, MTn_CH1, and MTn_CH2 pins are connected to the channel 0 input TI0
[19:18]	CH0PSC	Channel 0 Capture Input Source Prescaler Setting These bits define the effective events of the channel 0 capture input. Note that the prescaler is reset once the Channel 0 Capture/Compare Enable bit, CH0E, in the Channel Control register named CHCTR is cleared to 0. 00: No prescaler, channel 0 capture input signal is chosen for each active event 01: Channel 0 Capture input signal is chosen for every 2 events 10: Channel 0 Capture input signal is chosen for every 4 events 11: Channel 0 Capture input signal is chosen for every 8 events
[17:16]	CH0CCS	Channel 0 Capture/Compare Selection 00: Channel 0 is configured as an output 01: Channel 0 is configured as an input derived from the TI0 signal 10: Channel 0 is configured as an input derived from the TI1 signal 11: Channel 0 is configured as an input which comes from the TRCED signal derived from the Trigger Controller **Note:** The CH0CCS field can be accessed only when the CH0E bit is cleared to 0.

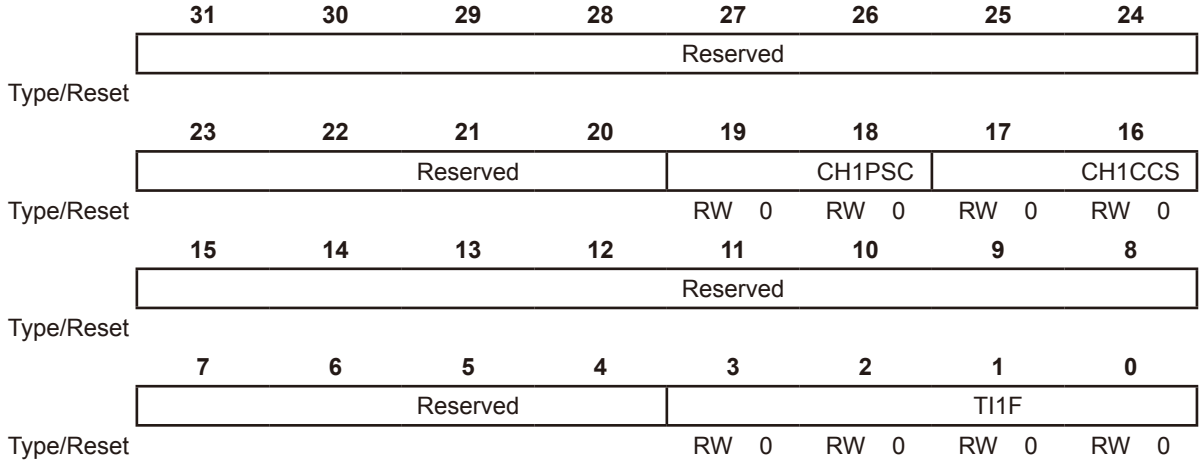
Bits	Field	Descriptions
[3:0]	TI0F	Channel 0 Input Source TI0 Filter Setting These bits define the frequency divided ratio used to sample the TI0 signal. The Digital filter in the MCTM is an N-event counter where N is defined as how many valid transitions are necessary to output a filtered signal. 0000: No filter, the sampling clock is f_{DTS} 0001: $f_{SAMPLING}=f_{CLKIN}$, N=2 0010: $f_{SAMPLING}=f_{CLKIN}$, N=4 0011: $f_{SAMPLING}=f_{CLKIN}$, N=8 0100: $f_{SAMPLING}=f_{DTS}/2$, N=6 0101: $f_{SAMPLING}=f_{DTS}/2$, N=8 0110: $f_{SAMPLING}=f_{DTS}/4$, N=6 0111: $f_{SAMPLING}=f_{DTS}/4$, N=8 1000: $f_{SAMPLING}=f_{DTS}/8$, N=6 1001: $f_{SAMPLING}=f_{DTS}/8$, N=8 1010: $f_{SAMPLING}=f_{DTS}/16$, N=5 1011: $f_{SAMPLING}=f_{DTS}/16$, N=6 1100: $f_{SAMPLING}=f_{DTS}/16$, N=8 1101: $f_{SAMPLING}=f_{DTS}/32$, N=5 1110: $f_{SAMPLING}=f_{DTS}/32$, N=6 1111: $f_{SAMPLING}=f_{DTS}/32$, N=8

Channel 1 Input Configuration Register – CH1ICFR

This register specifies the channel 1 input mode configuration.

Offset: 0x024

Reset value: 0x0000_0000



Bits	Field	Descriptions
[19:18]	CH1PSC	Channel 1 Capture Input Source Prescaler Setting These bits define the effective events of the channel 1 capture input. Note that the prescaler is reset once the Channel 1 Capture/Compare Enable bit, CH1E, in the Channel Control register named CHCTR is cleared to 0. 00: No prescaler, channel 1 capture input signal is chosen for each active event 01: Channel 1 Capture input signal is chosen for every 2 events 10: Channel 1 Capture input signal is chosen for every 4 events 11: Channel 1 Capture input signal is chosen for every 8 events
[17:16]	CH1CCS	Channel 1 Capture/Compare Selection 00: Channel 1 is configured as an output 01: Channel 1 is configured as an input derived from the TI1 signal 10: Channel 1 is configured as an input derived from the TI0 signal 11: Channel 1 is configured as an input which comes from the TRCED signal derived from the Trigger Controller **Note:** The CH1CCS field can be accessed only when the CH1E bit is cleared to 0.

Bits	Field	Descriptions
[3:0]	TI1F	Channel 1 Input Source TI1 Filter Setting These bits define the frequency divide ratio used to sample the TI1 signal. The Digital filter in the MCTM is an N-event counter where N is defined as how many valid transitions are necessary to output a filtered signal. 0000: No filter, the sampling clock is f_{DTS} 0001: $f_{SAMPLING}=f_{CLKIN}$, N=2 0010: $f_{SAMPLING}=f_{CLKIN}$, N=4 0011: $f_{SAMPLING}=f_{CLKIN}$, N=8 0100: $f_{SAMPLING}=f_{DTS}/2$, N=6 0101: $f_{SAMPLING}=f_{DTS}/2$, N=8 0110: $f_{SAMPLING}=f_{DTS}/4$, N=6 0111: $f_{SAMPLING}=f_{DTS}/4$, N=8 1000: $f_{SAMPLING}=f_{DTS}/8$, N=6 1001: $f_{SAMPLING}=f_{DTS}/8$, N=8 1010: $f_{SAMPLING}=f_{DTS}/16$, N=5 1011: $f_{SAMPLING}=f_{DTS}/16$, N=6 1100: $f_{SAMPLING}=f_{DTS}/16$, N=8 1101: $f_{SAMPLING}=f_{DTS}/32$, N=5 1110: $f_{SAMPLING}=f_{DTS}/32$, N=6 1111: $f_{SAMPLING}=f_{DTS}/32$, N=8

Channel 2 Input Configuration Register – CH2ICFR

This register specifies the channel 2 input mode configuration.

Offset: 0x028

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved				CH2PSC		CH2CCS	
Type/Reset					RW 0	RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved				TI2F			
Type/Reset					RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[19:18]	CH2PSC	Channel 2 Capture Input Source Prescaler Setting These bits define the effective events of the channel 2 capture input. Note that the prescaler is reset once the Channel 2 Capture/Compare Enable bit, CH2E, in the Channel Control register named CHCTR is cleared to 0. 00: No prescaler, channel 2 capture input signal is chosen for each active event 01: Channel 2 Capture input signal is chosen for every 2 events 10: Channel 2 Capture input signal is chosen for every 4 events 11: Channel 2 Capture input signal is chosen for every 8 events
[17:16]	CH2CCS	Channel 2 Capture/Compare Selection 00: Channel 2 is configured as an output 01: Channel 2 is configured as an input derived from the TI2 signal 10: Channel 2 is configured as an input derived from the TI3 signal 11: Channel 2 is configured as an input which comes from the TRCED signal derived from the Trigger Controller **Note:** The CH2CCS field can be accessed only when the CH2E bit is cleared to 0.

Bits	Field	Descriptions
[3:0]	TI2F	Channel 2 Input Source TI2 Filter Setting These bits define the frequency divide ratio used to sample the TI2 signal. The Digital filter in the MCTM is an N-event counter where N is defined as how many valid transitions are necessary to output a filtered signal. 0000: No filter, the sampling clock is f_{DTS} 0001: $f_{SAMPLING}=f_{CLKIN}$, N=2 0010: $f_{SAMPLING}=f_{CLKIN}$, N=4 0011: $f_{SAMPLING}=f_{CLKIN}$, N=8 0100: $f_{SAMPLING}=f_{DTS}/2$, N=6 0101: $f_{SAMPLING}=f_{DTS}/2$, N=8 0110: $f_{SAMPLING}=f_{DTS}/4$, N=6 0111: $f_{SAMPLING}=f_{DTS}/4$, N=8 1000: $f_{SAMPLING}=f_{DTS}/8$, N=6 1001: $f_{SAMPLING}=f_{DTS}/8$, N=8 1010: $f_{SAMPLING}=f_{DTS}/16$, N=5 1011: $f_{SAMPLING}=f_{DTS}/16$, N=6 1100: $f_{SAMPLING}=f_{DTS}/16$, N=8 1101: $f_{SAMPLING}=f_{DTS}/32$, N=5 1110: $f_{SAMPLING}=f_{DTS}/32$, N=6 1111: $f_{SAMPLING}=f_{DTS}/32$, N=8

Channel 3 Input Configuration Register – CH3ICFR

This register specifies the channel 3 input mode configuration.

Offset: 0x02C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved				CH3PSC		CH3CCS	
Type/Reset					RW 0	RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved				TI3F			
Type/Reset					RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[19:18]	CH3PSC	Channel 3 Capture Input Source Prescaler Setting These bits define the effective events of the channel 3 capture input. Note that the prescaler is reset once the Channel 3 Capture/Compare Enable bit, CH3E, in the Channel Control register named CHCTR is cleared to 0. 00: No prescaler, channel 3 capture input signal is chosen for each active event 01: Channel 3 Capture input signal is chosen for every 2 events 10: Channel 3 Capture input signal is chosen for every 4 events 11: Channel 3 Capture input signal is chosen for every 8 events
[17:16]	CH3CCS	Channel 3 Capture/Compare Selection 00: Channel 3 is configured as an output 01: Channel 3 is configured as an input derived from the TI3 signal 10: Channel 3 is configured as an input derived from the TI2 signal 11: Channel 3 is configured as an input which comes from the TRCED signal derived from the Trigger Controller **Note:** The CH3CCS field can be accessed only when the CH3E bit is cleared to 0.

Bits	Field	Descriptions
[3:0]	TI3F	Channel 3 Input Source TI3 Filter Setting These bits define the frequency divide ratio used to sample the TI3 signal. The digital filter in the GPTM is an N-event counter where N is defined as how many valid transitions are necessary to output a filtered signal. 0000: No filter, the sampling clock is f_{DTS} 0001: $f_{SAMPLING}=f_{CLKIN}$, N=2 0010: $f_{SAMPLING}=f_{CLKIN}$, N=4 0011: $f_{SAMPLING}=f_{CLKIN}$, N=8 0100: $f_{SAMPLING}=f_{DTS}/2$, N=6 0101: $f_{SAMPLING}=f_{DTS}/2$, N=8 0110: $f_{SAMPLING}=f_{DTS}/4$, N=6 0111: $f_{SAMPLING}=f_{DTS}/4$, N=8 1000: $f_{SAMPLING}=f_{DTS}/8$, N=6 1001: $f_{SAMPLING}=f_{DTS}/8$, N=8 1010: $f_{SAMPLING}=f_{DTS}/16$, N=5 1011: $f_{SAMPLING}=f_{DTS}/16$, N=6 1100: $f_{SAMPLING}=f_{DTS}/16$, N=8 1101: $f_{SAMPLING}=f_{DTS}/32$, N=5 1110: $f_{SAMPLING}=f_{DTS}/32$, N=6 1111: $f_{SAMPLING}=f_{DTS}/32$, N=8

Channel 0 Output Configuration Register – CH0OCFR

This register specifies the channel 0 output mode configuration.

Offset: 0x040

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
		Reserved	CH0IMAE	CH0PRE	REF0CE	CH0OM		
Type/Reset			RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[5]	CH0IMAE	Channel 0 Immediate Active Enable 0: No action 1: Single pulse Immediate Active Mode is enabled CH0OREF will be forced to the compare matched level immediately after an available trigger event occurs irrespective of the result of the comparison between the CNTR and the CH0CCR values. The effective duration ends automatically at the next overflow or underflow event. **Note:** The CH0IMAE bit is available only if channel 0 is configured operate in PWM mode 1 or PWM mode 2.
[4]	CH0PRE	Channel 0 Capture/Compare Register (CH0CCR) Preload Enable 0: CH0CCR preload function is disabled The CH0CCR register can be immediately assigned a new value when the CH0PRE bit is cleared to 0 and the updated CH0CCR value is used immediately. 1: CH0CCR preload function is enabled The new CH0CCR value will not be transferred to its shadow register until an update event 1 occurs.
[3]	REF0CE	Channel 0 Reference Output Clear Enable 0: CH0OREF operates normally and is not affected by the ETIF signal 1: CH0OREF is forced to 0 on the high level of the ETIF signal derived from the MTn_ETI pin

Bits	Field	Descriptions
[2:0]	CH0OM	Channel 0 Output Mode Setting These bits define the functional types of the output reference signal CH0OREF. 000: No Change 001: Output 0 on compare match 010: Output 1 on compare match 011: Output toggles on compare match 100: Force inactive – CH0OREF is forced to 0 101: Force active – CH0OREF is forced to 1 110: PWM mode 1 – During up-counting, channel 0 has an active level when CNTR<CH0CCR or otherwise has an inactive level. – During down-counting, channel 0 has an inactive level when CNTR>CH0CCR or otherwise has an active level. 111: PWM mode 2 – During up-counting, channel 0 is has an inactive level when CNTR<CH0CCR or otherwise has an active level. – During down-counting, channel 0 has an active level when CNTR>CH0CCR or otherwise has an inactive level.

Channel 1 Output Configuration Register – CH1OCFR

This register specifies the channel 1 output mode configuration.

Offset: 0x044

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
		Reserved	CH1IMAE	CH1PRE	REF1CE	CH1OM		
Type/Reset			RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[5]	CH1IMAE	Channel 1 Immediate Active Enable 0: No action 1: Single pulse Immediate Active Mode enabled The CH1OREF will be forced to the compare matched level immediately after an available trigger event occurs irrespective of the result of the comparison between the CNTR and the CH1CCR values. The effective duration ends automatically at the next overflow or underflow event. **Note:** The CH1IMAE bit is available only if channel 1 is configured to be operated in PWM mode 1 or PWM mode 2.
[4]	CH1PRE	Channel 1 Capture/Compare Register (CH1CCR) Preload Enable 0: CH1CCR preload function is disabled The CH1CCR register can be immediately assigned a new value when the CH1PRE bit is cleared to 0 and the updated CH1CCR value is used immediately. 1: CH1CCR preload function is enabled The new CH1CCR value will not be transferred to its shadow register until an update event 1 occurs.
[3]	REF1CE	Channel 1 Reference Output Clear Enable 0: CH1OREF performed normally and is not affected by the ETIF signal 1: CH1OREF is forced to 0 on the high level of the ETIF signal derived from the MTn_ETI pin

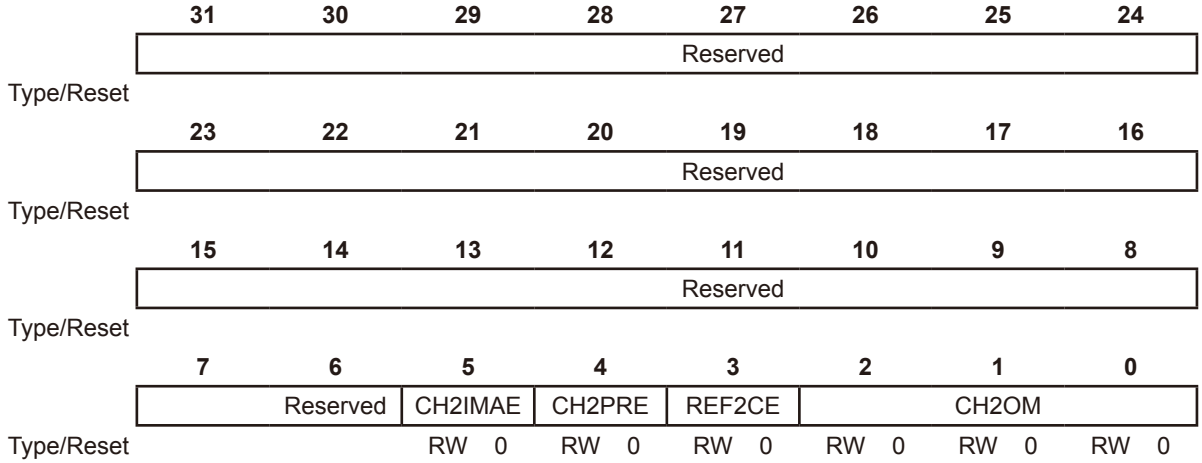
Bits	Field	Descriptions
[2:0]	CH1OM	Channel 1 Output Mode Setting These bits define the functional types of the output reference signal CH1OREF. 000: No Change 001: Output 0 on compare match 010: Output 1 on compare match 011: Output toggles on compare match 100: Force inactive – CH1OREF is forced to 0 101: Force active – CH1OREF is forced to 1 110: PWM mode 1 – During up-counting, channel 1 has an active level when CNTR<CH1CCR or otherwise has an inactive level. – During down-counting, channel 1 has an inactive level when CNTR>CH1CCR or otherwise has an active level. 111: PWM mode 2 – During up-counting, channel 1 has an inactive level when CNTR<CH1CCR or otherwise has an active level. – During down-counting, channel 1 has an active level when CNTR>CH1CCR or otherwise has an inactive level.

Channel 2 Output Configuration Register – CH2OCFR

This register specifies the channel 2 output mode configuration.

Offset: 0x048

Reset value: 0x0000_0000



Bits	Field	Descriptions
[5]	CH2IMAE	Channel 2 Immediate Active Enable 0: No action 1: Single pulse Immediate Active Mode enabled The CH2OREF will be forced to the compare matched level immediately after an available trigger event occurs irrespective of the result of the comparison between the CNTR and the CH2CCR values. The effective duration ends automatically at the next overflow or underflow event. **Note:** The CH2IMAE bit is available only if the channel 2 is configured to be operated in PWM mode 1 or PWM mode 2.
[4]	CH2PRE	Channel 2 Capture/Compare Register (CH2CCR) Preload Enable 0: CH2CCR preload function is disabled The CH2CCR register can be immediately assigned a new value when the CH2PRE bit is cleared to 0 and the updated CH2CCR value is used immediately. 1: CH2CCR preload function is enabled The new CH2CCR value will not be transferred to its shadow register until an update event 1 occurs.
[3]	CH3OCCE	Channel 2 Reference Output Clear Enable 0: CH2OREF operates normally and is not affected by the ETIF signal 1: CH2OREF is forced to 0 during a high level of the ETIF signal derived from the MTn_ETI pin

Bits	Field	Descriptions
[2:0]	CH2OM	Channel 2 Output Mode Setting These bits define the functional types of the output reference signal CH2OREF. 000: No Change 001: Output 0 on compare match 010: Output 1 on compare match 011: Output toggles on compare match 100: Force inactive – CH2OREF is forced to 0 101: Force active – CH2OREF is forced to 1 110: PWM mode 1 – During up-counting, channel 2 has an active level when CNTR<CH2CCR or otherwise has an inactive level. – During down-counting, channel 2 has an inactive level when CNTR>CH2CCR or otherwise has an active level. 111: PWM mode 2 – During up-counting, channel 2 has an inactive level when CNTR<CH2CCR or otherwise has an active level. – During down-counting, channel 2 has an active level when CNTR>CH2CCR or otherwise has an inactive level.

Channel 3 Output Configuration Register – CH3OCFR

This register specifies the channel 3 output mode configuration.

Offset: 0x04C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
		Reserved	CH3IMAE	CH3PRE	REF3CE	CH3OM		
Type/Reset			RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[5]	CH3IMAE	Channel 3 Immediate Active Enable 0: No action 1: Single pulse Immediate Active Mode enabled The CH3OREF will be forced to the compare matched level immediately after an available trigger event occurs irrespective of the result of the comparison between the CNTR and the CH3CCR values. The effective duration ends automatically at the next overflow or underflow event. **Note:** The CH3IMAE bit is available only if channel 3 is configured to be operated in PWM mode 1 or PWM mode 2.
[4]	CH3PRE	Channel 3 Capture/Compare Register (CH3CCR) Preload Enable 0: CH3CCR preload function is disabled The CH3CCR register can be immediately assigned a new value when the CH3PRE bit is cleared to 0 and the updated CH3CCR value is used immediately. 1: CH3CCR preload function is enabled The new CH3CCR value will not be transferred to its shadow register until an update event 1 occurs.
[3]	REF3CE	Channel 3 Reference Output Clear Enable 0: CH3OREF operates normally and is not affected by the ETIF signal 1: CH3OREF is forced to 0 during the high level of the ETIF signal derived from the MTn_ETI pin

Bits	Field	Descriptions
[2:0]	CH3OM	Channel 3 Output Mode Setting These bits define the functional types of the output reference signal CH3OREF. 000: No Change 001: Output 0 on compare match 010: Output 1 on compare match 011: Output toggles on compare match 100: Force inactive – CH3OREF is forced to 0 101: Force active – CH3OREF is forced to 1 110: PWM mode 1 – During up-counting, channel 3 has an active level when CNTR<CH3CCR or otherwise has an inactive level. – During down-counting, channel 3 has an inactive level when CNTR>CH3CCR or otherwise has an active level. 111: PWM mode 2 – During up-counting, channel 3 has an inactive level when CNTR<CH3CCR or otherwise has an active level. – During down-counting, channel 3 has an active level when CNTR>CH3CCR or otherwise has an inactive level.

Channel Control Register – CHCTR

This register contains the channel capture input or compare output function enable control bits.

Offset: 0x050

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved	CH3E	CH2NE	CH2E	CH1NE	CH1E	CH0NE	CH0E
Type/Reset		RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[6]	CH3E	Channel 3 Capture/Compare Enable – Channel 3 is configured as an input (CH3CCS=0x01/0x02/0x03) 0: Input Capture Mode disabled 1: Input Capture Mode enabled – Channel 3 is configured as an output (CH3CCS=0x00) 0: Off – Channel 3 output signal CH3O is not active 1: On – Channel 3 output signal CH3O is generated on the corresponding output pin depending on the condition of the CHMOE, CHOSSI, CHOSSR and CH3OIS bits.
[5]	CH2NE	Channel 2 Capture/Compare Complementary Enable 0: Off – Channel 2 complementary output CH2NO is not active. The CH2NO level is then determined by the CHMOE, CHOSSI, CHOSSR, CH2OIS, CH2OISN and CH2E bits. 1: On – Channel 2 complementary output CH2NO is generated on the corresponding output pin depending on the condition of the CHMOE, CHOSSI, CHOSSR, CH2OIS, CH2OISN and CH2E bits.
[4]	CH2E	Channel 2 Capture/Compare Enable – Channel 2 is configured as an input (CH2CCS=0x01/0x02/0x03) 0: Input Capture Mode disabled 1: Input Capture Mode enabled – Channel 2 is configured as an output (CH2CCS=0x00) 0: Off – Channel 2 output signal CH2O is not active. The CH2O level is then determined by the condition of the CHMOE, CHOSSI, CHOSSR, CH2OIS, CH2OISN and CH2NE bits. 1: On – Channel 2 output signal CH2O is generated on the corresponding output pin determined by the condition of the CHMOE, CHOSSI, CHOSSR, CH2OIS, CH2OISN and CH2NE bits.

Bits	Field	Descriptions
[3]	CH1NE	Channel 1 Capture/Compare Complementary Enable 0: Off – Channel 1 complementary output CH1NO is not active. The CH1NO level is then determined by the condition of the CHMOE, CHOSSI, CHOSSR, CH1OIS, CH1OISN and CH1E bits. 1: On – Channel 1 complementary output CH1NO is generated on the corresponding output pin determined by the condition of the CHMOE, CHOSSI, CHOSSR, CH1OIS, CH1OISN and CH1E bits.
[2]	CH1E	Channel 1 Capture/Compare Enable – Channel 1 is configured as an input (CH1CCS=0x01/0x02/0x03) 0: Input Capture Mode disabled 1: Input Capture Mode enabled – Channel 1 is configured as an output (CH1CCS=0x00) 0: Off – Channel 1 output signal CH1O is not active. The CH1O level is then determined by the condition of the CHMOE, CHOSSI, CHOSSR, CH1OIS, CH1OISN and CH1NE bits. 1: On – Channel 1 output signal CH1O is generated on the corresponding output pin depending on the condition of the CHMOE, CHOSSI, CHOSSR, CH1OIS, CH1OISN and CH1NE bits.
[1]	CH0NE	Channel 0 Capture/Compare Complementary Enable 0: Off – Channel 0 complementary output CH0NO is not active. The CH0NO level is then determined by the condition of the CHMOE, CHOSSI, CHOSSR, CH0OIS, CH0OISN and CH0E bits. 1: On – Channel 0 complementary output CH0NO is generated on the corresponding output pin depending on the condition of the CHMOE, CHOSSI, CHOSSR, CH0OIS, CH0OISN and CH0E bits.
[0]	CH0E	Channel 0 Capture/Compare Enable – Channel 0 is configured as an input (CH0CCS=0x01/0x02/0x03) 0: Input Capture Mode disabled 1: Input Capture Mode enabled – Channel 0 is configured as an output (CH0CCS=0x00) 0: Off – Channel 0 output signal CH0O is not active. The CH0O level is then determined by the condition of the CHMOE, CHOSSI, CHOSSR, CH0OIS, CH0OISN and CH0NE bits. 1: On – Channel 0 output signal CH0O is generated on the corresponding output pin determined by the condition of the CHMOE, CHOSSI, CHOSSR, CH0OIS, CH0OISN and CH0NE bits.

Channel Polarity Configuration Register – CHPOLR

This register contains the channel capture input or compare output polarity control.

Offset: 0x054

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								

	7	6	5	4	3	2	1	0
	Reserved	CH3P	CH2NP	CH2P	CH1NP	CH1P	CH0NP	CH0P
Type/Reset		RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[6]	CH3P	Channel 3 Capture/Compare Polarity – When Channel 3 is configured as an input 0: capture event occurs on a Channel 3 rising edge 1: capture event occurs on a Channel 3 falling edge – When Channel 3 is configured as an output (CH3CCS=0x00) 0: Channel 3 Output active high 1: Channel 3 Output active low
[5]	CH2NP	Channel 2 Capture/Compare Complementary Polarity 0: Channel 2 Output active high 1: Channel 2 Output active low
[4]	CH2P	Channel 2 Capture/Compare Polarity – When Channel 2 is configured as an input 0: capture event occurs on a Channel 2 rising edge 1: capture event occurs on a Channel 2 falling edge – When Channel 2 is configured as an output (CH2CCS=0x00) 0: Channel 2 Output active high 1: Channel 2 Output active low
[3]	CH1NP	Channel 1 Capture/Compare Complementary Polarity 0: Channel 1 Output active high 1: Channel 1 Output active low
[2]	CH1P	Channel 1 Capture/Compare Polarity – When Channel 1 is configured as an input 0: capture event occurs on a Channel 1 rising edge 1: capture event occurs on a Channel 1 falling edge – Channel 1 is configured as an output (CH1CCS=0x00) 0: Channel 1 Output active high 1: Channel 1 Output active low

Bits	Field	Descriptions
[1]	CH0NP	Channel 0 Capture/Compare Complementary Polarity 0: Channel 0 Output active high 1: Channel 0 Output active low
[0]	CH0P	Channel 0 Capture/Compare Polarity – When Channel 0 is configured as an input 0: capture event occurs on a Channel 0 rising edge 1: capture event occurs on a Channel 0 falling edge – When Channel 0 is configured as an output (CH0CCS=0x00) 0: Channel 0 Output active high 1: Channel 0 Output active low

Channel Break Configuration Register – CHBRKCFR

This register specifies the channel output idle state when using the break function.

Offset: 0x06C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								

	7	6	5	4	3	2	1	0
	Reserved	CH3OIS	CH2OISN	CH2OIS	CH1OISN	CH1OIS	CH0OISN	CH0OIS
Type/Reset		RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[6]	CH3OIS	MTx_CH3O Output Idle State 0: Channel 3 output CH3O=0 when CHMOE=0 1: Channel 3 output CH3O=1 when CHMOE=0
[5]	CH2OISN	MTx_CH2NO Output Idle State 0: Channel 2 complementary output CH2NO=0 after a dead time when CHMOE=0 1: Channel 2 complementary output CH2NO=1 after a dead time when CHMOE=0
[4]	CH2OIS	MTx_CH2O Output Idle State 0: Channel 2 output CH2O=0 after a dead time when CHMOE=0 1: Channel 2 output CH2O=1 after a dead time when CHMOE=0
[3]	CH1OISN	MTx_CH1NO Output Idle State 0: Channel 1 complementary output CH1NO=0 after a dead time when CHMOE=0 1: Channel 1 complementary output CH1NO=1 after a dead time when CHMOE=0
[2]	CH1OIS	MTx_CH1O Output Idle State 0: Channel 1 output CH1O=0 after a dead time when CHMOE=0 1: Channel 1 output CH1O=1 after a dead time when CHMOE=0
[1]	CH0OISN	MTx_CH0NO Output Idle State 0: Channel 0 complementary output CH1NO=0 after a dead time when CHMOE=0 1: Channel 0 complementary output CH1NO=1 after a dead time when CHMOE=0
[0]	CH0OIS	MTx_CH0O Output Idle State 0: Channel 0 output CH0O=0 after a dead time when CHMOE=0 1: Channel 0 output CH0O=1 after a dead time when CHMOE=0

Channel Break Control Register – CHBRKCTR

This register specifies the channel break control bits.

Offset: 0x070

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	CHDTG							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	23	22	21	20	19	18	17	16
		Reserved	CHOSSR	CHOSSI		Reserved		LOCKLV
Type/Reset			RW 0	RW 0			RW 0	RW 0
	15	14	13	12	11	10	9	8
	Reserved				BKF			
Type/Reset					RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
		Reserved	CHAOE	CHMOE		Reserved	BKP	BKE
Type/Reset			RW 0	RW 0			RW 0	RW 0

Bits	Field	Descriptions
[31:24]	CHDTG	Channel Dead Time Duration Definition CHDTG[7:5]=0xx: Channel Dead Time=CHDTG [7:0] × t_{dtg}, with $t_{dtg}=t_{DTS}$ CHDTG[7:5]=10x: Channel Dead Time=(64 + CHDTG [5:0]) × t_{dtg}, with $t_{dtg}=2 \times t_{DTS}$ CHDTG[7:5]=110: Channel Dead Time=(32 + CHDTG [4:0]) × t_{dtg}, with $t_{dtg}=8 \times t_{DTS}$ CHDTG[7:5]=111: Channel Dead Time=(32 + CHDTG [4:0]) × t_{dtg}, with $t_{dtg}=16 \times t_{DTS}$
[21]	CHOSSR	Channel Off State (CHxE, CHxNE=0) Selection for Normal Run State (CHMOE=1) 0: When inactive, MTn_CHxO/MTn_CHxNO output disable – not driven by timer 1: When inactive, MTn_CHxO/MTn_CHxNO output enabled with their inactive level
[20]	CHOSSI	Channel Off State Selection for Idle Mode (CHMOE=0) 0: When inactive, MTn_CHxO/MTn_CHxNO output disable – not driven by timer 1: When inactive, MTn_CHxO/MTn_CHxNO output enabled with their idle level depending upon the condition of the CHxOIS and CHxOISN bits
[17:16]	LOCKLV	Lock Level Setting These bits offer write protection against software errors. The bits can be written only once after a reset. 00: LOCK OFF. Register write protected function disabled 01: LOCK Level 1 10: LOCK Level 2 11: LOCK Level 3

Bits	Field	Descriptions
[11:8]	BKF	Break Input Filter Setting These bits define the frequency ratio used to sample the BRKIN signal. The digital filter in the MCTM is an N-event counter where N is defined as how many valid transitions are necessary to output a filtered signal. 0000: No filter – don't need sample clock 0001: $f_{SAMPLING}=f_{CLKIN}$, N=2 0010: $f_{SAMPLING}=f_{CLKIN}$, N=4 0011: $f_{SAMPLING}=f_{CLKIN}$, N=8 0100: $f_{SAMPLING}=f_{DTS}/2$, N=6 0101: $f_{SAMPLING}=f_{DTS}/2$, N=8 0110: $f_{SAMPLING}=f_{DTS}/4$, N=6 0111: $f_{SAMPLING}=f_{DTS}/4$, N=8 1000: $f_{SAMPLING}=f_{DTS}/8$, N=6 1001: $f_{SAMPLING}=f_{DTS}/8$, N=8 1010: $f_{SAMPLING}=f_{DTS}/16$, N=5 1011: $f_{SAMPLING}=f_{DTS}/16$, N=6 1100: $f_{SAMPLING}=f_{DTS}/16$, N=8 1101: $f_{SAMPLING}=f_{DTS}/32$, N=5 1110: $f_{SAMPLING}=f_{DTS}/32$, N=6 1111: $f_{SAMPLING}=f_{DTS}/32$, N=8
[5]	CHAOE	Channel Automatic Output Enable 0: CHMOE can be set only by software 1: CHMOE can be set by software or automatically by an update event
[4]	CHMOE	Channel Main Output Enable Cleared asynchronously by hardware on a break event occurrence. 0: MTn_CHxO and MTn_CHxNO are disabled or forced to an idle status 1: MTn_CHxO and MTn_CHxNO are enabled if the enable bits (CHxE, CHxNE) are set
[1]	BKP	Break Input Polarity 0: Break input active low 1: Break input active high
[0]	BKE	Break Enable 0: Break inputs disabled 1: Break inputs enabled

Timer PDMA/Interrupt Control Register – DICTR

This register contains the timer PDMA and interrupt enable control bits.

Offset: 0x074

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved					TEVDE	UEV2DE	UEV1DE
Type/Reset						RW 0	RW 0	RW 0
	23	22	21	20	19	18	17	16
	Reserved				CH3CCDE	CH2CCDE	CH1CCDE	CH0CCDE
Type/Reset					RW 0	RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
	Reserved				BRKIE	TEVIE	UEV2IE	UEV1IE
Type/Reset					RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	Reserved				CH3CCIE	CH2CCIE	CH1CCIE	CH0CCIE
Type/Reset					RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[26]	TEVDE	Trigger event PDMA Request Enable 0: Trigger PDMA request disabled 1: Trigger PDMA request enabled
[25]	UEV2DE	Update event 2 PDMA Request Enable 0: Update event 2 PDMA request disabled 1: Update event 2 PDMA request enabled
[24]	UEV1DE	Update event 1 PDMA Request Enable 0: Update event 1 PDMA request disabled 1: Update event 1 PDMA request enabled
[19]	CH3CCDE	Channel 3 Capture/Compare PDMA Request Enable 0: Channel 3 PDMA request disabled 1: Channel 3 PDMA request enabled
[18]	CH2CCDE	Channel 2 Capture/Compare PDMA Request Enable 0: Channel 2 PDMA request disabled 1: Channel 2 PDMA request enabled
[17]	CH1CCDE	Channel 1 Capture/Compare PDMA Request Enable 0: Channel 1 PDMA request disabled 1: Channel 1 PDMA request enabled
[16]	CH0CCDE	Channel 0 Capture/Compare PDMA Request Enable 0: Channel 0 PDMA request disabled 1: Channel 0 PDMA request enabled
[11]	BRKIE	Break event Interrupt Enable 0: Break event interrupt disabled 1: Break event interrupt enabled
[10]	TEVIE	Trigger event Interrupt Enable 0: Trigger event interrupt disabled 1: Trigger event interrupt enabled

Bits	Field	Descriptions
[9]	UEV2IE	Update event 2 Interrupt Enable 0: Update event 2 interrupt disabled 1: Update event 2 interrupt enabled
[8]	UEV1IE	Update event 1 Interrupt Enable 0: Update event 1 interrupt disabled 1: Update event 1 interrupt enabled
[3]	CH3CCIE	Channel 3 Capture/Compare Interrupt Enable 0: Channel 3 interrupt disabled 1: Channel 3 interrupt enabled
[2]	CH2CCIE	Channel 2 Capture/Compare Interrupt Enable 0: Channel 2 interrupt disabled 1: Channel 2 interrupt enabled
[1]	CH1CCIE	Channel 1 Capture/Compare Interrupt Enable 0: Channel 1 interrupt disabled 1: Channel 1 interrupt enabled
[0]	CH0CCIE	Channel 0 Capture/Compare Interrupt Enable 0: Channel 0 interrupt disabled 1: Channel 0 interrupt enabled

Timer Event Generator Register – EVGR

This register contains the software event generation bits.

Offset: 0x078

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved				BRKG	TEVG	UEV2G	UEV1G
Type/Reset					WO 0	WO 0	WO 0	WO 0
	7	6	5	4	3	2	1	0
	Reserved				CH3CCG	CH2CCG	CH1CCG	CH0CCG
Type/Reset					WO 0	WO 0	WO 0	WO 0

Bits	Field	Descriptions
[11]	BRKG	Software Break Event Generation The break event BEV can be generated by setting this bit. It is automatically cleared by hardware. 0: No action 1: The BRKIF flag is set and then the CHMOE bit will be cleared
[10]	TEVG	Trigger Event Generation The trigger event TEV can be generated by setting this bit. It is cleared by hardware automatically. 0: No action 1: The TEVIF flag is set
[9]	UEV2G	Update Event 2 Generation The update event 2 UEV2 can be generated by setting this bit. It is cleared by hardware automatically. 0: No action 1: Update the CHxE, CHxNE, and CHxOM bits when COMPRE bit in CTR Register is set to 1
[8]	UEV1G	Update Event 1 Generation The update event 1 UEV1 can be generated by setting this bit. It is cleared by hardware automatically. 0: No action 1: Reinitialise the counter The counter value returns to 0 or the CRR preload value, depending on the counter mode in which the current timer is being used. An update operation on any related registers will also be executed. For a more detailed description, refer to the corresponding section.

Bits	Field	Descriptions
[3]	CH3CCG	Channel 3 Capture/Compare Generation A Channel 3 capture/compare event can be generated by setting this bit. It is cleared by hardware automatically. 0: No action 1: Capture/compare event is generated on channel 3 If Channel 3 is configured as an input, the counter value is captured into the CH3CCR register and then the CH3CCIF bit is set. If Channel 3 is configured as an output, the CH3CCIF bit is set.
[2]	CH2CCG	Channel 2 Capture/Compare Generation A Channel 2 capture/compare event can be generated by setting this bit. It is cleared by hardware automatically. 0: No action 1: Capture/compare event is generated on channel 2 If Channel 2 is configured as an input, the counter value is captured into the CH2CCR register and then the CH2CCIF bit is set. If Channel 2 is configured as an output, the CH2CCIF bit is set.
[1]	CH1CCG	Channel 1 Capture/Compare Generation A Channel 1 capture/compare event can be generated by setting this bit. It is cleared by hardware automatically. 0: No action 1: Capture/compare event is generated on channel 1 If Channel 1 is configured as an input, the counter value is captured into the CH1CCR register and then the CH1CCIF bit is set. If Channel 1 is configured as an output, the CH1CCIF bit is set.
[0]	CH0CCG	Channel 0 Capture/Compare Generation A Channel 0 capture/compare event can be generated by setting this bit. It is cleared by hardware automatically. 0: No action 1: Capture/compare event is generated on channel 0 If Channel 0 is configured as an input, the counter value is captured into the CH0CCR register and then the CH0CCIF bit is set. If Channel 0 is configured as an output, the CH0CCIF bit is set.

Timer Interrupt Status Register – INTSR

This register stores the timer interrupt status.

Offset: 0x07C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved				BRKIF	TEVIF	UEV2IF	UEV1IF
Type/Reset					RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	CH3OCF	CH2OCF	CH1OCF	CH0OCF	CH3CCIF	CH2CCIF	CH1CCIF	CH0CCIF
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[11]	BRKIF	Break Event Interrupt Flag This flag is set by hardware when a break event occurs and is cleared by software. 0: No break event occurred 1: Break event occurred
[10]	TEVIF	Trigger Event Interrupt Flag This flag is set by hardware when a trigger event occurs and is cleared by software. 0: No trigger event occurred 1: Trigger event occurred
[9]	UEV2IF	Update Event 2 Interrupt Flag This bit is set by hardware when an update event 2 occurs and is cleared by software. 0: No update event 2 occurred 1: Update event 2 occurred
[8]	UEV1IF	Update Event 1 Interrupt Flag This bit is set by hardware when an update event 1 occurs and is cleared by software. 0: No update event 1 occurred 1: Update event 1 occurred **Note:** The update event 1 is sourced from the following conditions: – A counter overflow or underflow – The UEV1G bit is set with UEV1DIS=0 – A STI rising edge is received in slave restart mode with UEV1DIS=0
[7]	CH3OCF	Channel 3 Over-capture Flag This flag is set by hardware and cleared by software. 0: No over-capture event is detected 1: Capture event occurs again when the CH3CCIF bit is already set and it is not yet cleared by software

Bits	Field	Descriptions
[6]	CH2OCF	Channel 2 Over-capture Flag This flag is set by hardware and cleared by software. 0: No over-capture event is detected 1: Capture event occurs again when the CH2CCIF bit is already set and it is not cleared yet by software
[5]	CH1OCF	Channel 1 Over-capture Flag This flag is set by hardware and cleared by software. 0: No over-capture event is detected 1: Capture event occurs again when the CH1CCIF bit is already set and it is not cleared yet by software
[4]	CH0OCF	Channel 0 Over-capture Flag This flag is set by hardware and cleared by software. 0: No over-capture event is detected 1: Capture event occurs again when the CH0CCIFbit is already set and it is not yet cleared by software
[3]	CH3CCIF	Channel 3 Capture/Compare Interrupt Flag – Channel 3 is configured as an output 0: No match event occurred 1: The contents of the counter CNTR have matched the contents of the CH3CCR register This flag is set by hardware when the counter value matches the CH3CCR value with exception in some center-aligned counting mode. It is cleared by software. – Channel 3 is configured as an input 0: No input capture occurred 1: Input capture occurred This bit is set by hardware when a capture event occurs. It is cleared by software or by reading the CH3CCR register.
[2]	CH2CCIF	Channel 2 Capture/Compare Interrupt Flag – Channel 2 is configured as an output 0: No match event occurred 1: The contents of the counter CNTR have matched the contents of the CH2CCR register This flag is set by hardware when the counter value matches the CH2CCR value with exception in some center-aligned counting mode. It is cleared by software. – Channel 2 is configured as an input 0: No input capture occurred 1: Input capture occurred. This bit is set by hardware on a capture event. It is cleared by software or by reading the CH2CCR register.

Bits	Field	Descriptions
[1]	CH1CCIF	Channel 1 Capture/Compare Interrupt Flag – Channel 1 is configured as an output 0: No match event occurred 1: The contents of the counter CNTR have matched the contents of the CH1CCR register This flag is set by hardware when the counter value matches the CH1CCR value with exception in some center-aligned counting mode. It is cleared by software. – Channel 1 is configured as an input 0: No input capture occurred 1: Input capture occurred This bit is set by hardware on a capture event. It is cleared by software or by reading the CH1CCR register.
[0]	CH0CCIF	Channel 0 Capture/Compare Interrupt Flag – Channel 0 is configured as an output 0: No match event occurs 1: The contents of the counter CNTR have matched the content of the CH0CCR register This flag is set by hardware when the counter value matches the CH0CCR value with exception in some center-aligned counting mode. It is cleared by software. – Channel 0 is configured as an input 0: No input capture occurred 1: Input capture occurred This bit is set by hardware on a capture event. It is cleared by software or by reading the CH0CCR register.

Timer Counter Register – CNTR

This register stores the timer counter value.

Offset: 0x080

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	Reserved							
Type/Reset								
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	CNTV							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	CNTV							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	CNTV	Counter Value

Timer Prescaler Register – PSCR

This register specifies the timer prescaler value to generate the counter clock.

Offset: 0x084

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	PSCV							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	PSCV							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	PSCV	Prescaler Value These bits are used to specify the prescaler value to generate the counter clock frequency f_{CK_CNT}. $f_{CK\_CNT} = \frac{f_{CK\_PSC}}{PSCV[15:0]+1}$, where the f_{CK_PSC} is the prescaler clock source.

Timer Counter Reload Register – CRR

This register specifies the timer counter reload value.

Offset: 0x088

Reset value: 0x0000_FFFF

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	CRV							
Type/Reset	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1
	7	6	5	4	3	2	1	0
	CRV							
Type/Reset	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1

Bits	Field	Descriptions
[15:0]	CRV	Counter Reload Value The CRV is the reload value which is loaded into the actual counter register.

Timer Repetition Register – REPR

This register specifies the timer repetition counter value.

Offset: 0x08C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	REPV							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[7:0]	REPV	Repetition Counter Value These bits allow the user to specify the update rate of the compare registers.

Channel 0 Capture/Compare Register – CH0CCR

This register specifies the timer channel 0 capture/compare value.

Offset: 0x090

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	Reserved							
Type/Reset								
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	CH0CCV							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	CH0CCV							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	CH0CCV	Channel 0 Capture/Compare Value – When Channel 0 is configured as an output The CH0CCR value is compared with the counter value and the comparison result is used to trigger the CH0OREF output signal. – When Channel 0 is configured as an input The CH0CCR register stores the counter value captured by the last channel 0 capture event.

Channel 1 Capture/Compare Register – CH1CCR

This register specifies the timer channel 1 capture/compare value.

Offset: 0x094

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	Reserved							
Type/Reset								
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	CH1CCV							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	CH1CCV							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	CH1CCV	Channel 1 Capture/Compare Value – When Channel 1 is configured as an output The CH1CCR value is compared with the counter value and the comparison result is used to trigger the CH1OREF output signal. – When Channel 1 is configured as an input The CH1CCR register stores the counter value captured by the last channel 1 capture event.

Channel 2 Capture/Compare Register – CH2CCR

This register specifies the timer channel 2 capture/compare value.

Offset: 0x098

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	CH2CCV							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	CH2CCV							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	CH2CCV	Channel 2 Capture/Compare Value – When Channel 2 is configured as an output The CH2CCR value is compared with the counter value and the comparison result is used to trigger the CH2OREF output signal. – When Channel 2 is configured as an input The CH2CCR register stores the counter value captured by the last channel 2 capture event.

Channel 3 Capture/Compare Register – CH3CCR

This register specifies the timer channel 3 capture/compare value.

Offset: 0x09C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	Reserved							
Type/Reset								
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	CH3CCV							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	CH3CCV							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	CH3CCV	Channel 3 Capture/Compare Value – When Channel 3 is configured as an output The CH3CCR value is compared with the counter value and the comparison result is used to trigger the CH3OREF output signal. – When Channel 3 is configured as an input The CH3CCR register stores the counter value captured by the last channel 3 capture event.

17 Real Time Clock (RTC)

Introduction

The Real Time Clock, RTC, circuitry includes the APB interface, a 32-bit up-counter, a control register, a prescaler, a compare register and a status register. Most of the RTC circuits are located in the Backup Domain, as shown shaded in the accompanying figure, except for the APB interface. The APB interface is located in the V_{DD18} domain. Therefore, it is necessary to be isolated from the ISO signal that comes from the power control unit when the V_{DD18} domain is powered off, i.e., when the device enters the Power-Down mode. The RTC counter is used as a wakeup timer to let the system resume from the Power-Down mode. The detailed RTC function will be described in the following sections.

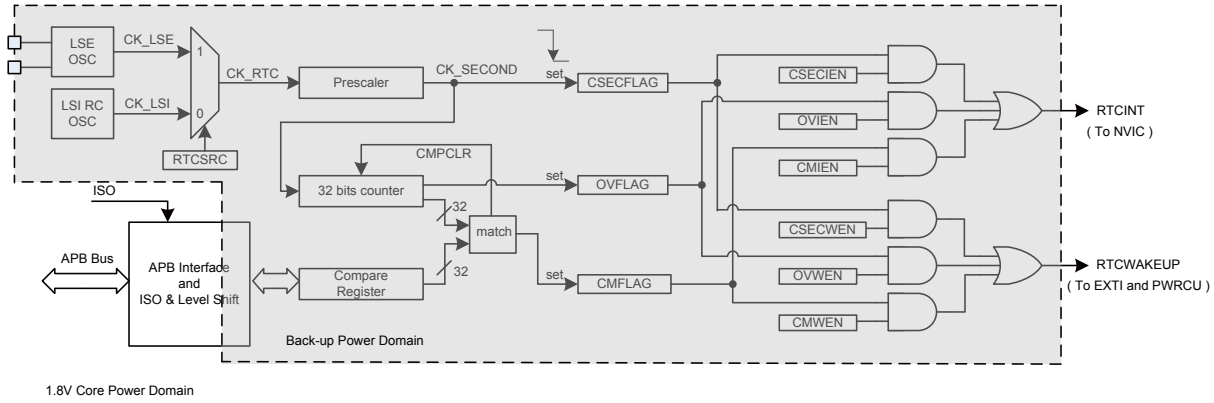


Figure 113. RTC Block Diagram

Features

- 32-bit up counter for counting elapsed time
- Programmable clock prescaler
  - Division factor: 1, 2, 4, 8…, 32768
- 32-bit compare register for alarm usage
- RTC clock source
  - LSE oscillator clock
  - LSI oscillator clock
- Three RTC interrupt/wakeup settings
  - RTC second clock interrupt/wakeup
  - RTC compare match interrupt/wakeup
  - RTC counter overflow interrupt/wakeup
- The RTC interrupt/wakeup event can work together with power management to wake up the chip from power saving modes

Functional Descriptions

RTC Related Register Reset

The RTC registers can only be reset by either a Backup Domain power on reset, PORB, or by a Backup Domain software reset by setting the BAKRST bit in the BAKCR register. Other reset events have no effect to clear the RTC registers.

Reading RTC Register

The RTC control logic and the related registers are powered by the V_{BAK} supply voltage. Therefore, the RTC circuitry remains operational in the Power-Down mode where V_{DD18} is powered off. Only the APB bus, which is located in the V_{DD18} domain, is interconnected to the circuits located in the V_{BAK} domain using level shift circuitry and isolated by the ISO signals when the V_{DD18} supply voltage is powered off. The isolation function must be disabled by setting the BAKISO bit to 1 in the LPCR register as described in the Clock Control Unit before accessing the RTC registers using the APB bus.

Low Speed Clock Configuration

The default RTC clock source, CK_RTC, is derived from the LSI oscillator. The CK_RTC clock can be derived from either the external 32768Hz crystal oscillator, named the LSE oscillator, or the internal 32K RC oscillator named the LSI oscillator, by setting the RTCSRC bit in the RTCCR register. A prescaler is provided to divide the CK_RTC by a ratio ranged from 2^0 to 2^{15} determined by the RPRE [3:0] field. For instance, setting the prescaler value RPRE [3:0] to 0x0F will generate an exact 1Hz CK_SECOND clock if the CK_RTC clock frequency is equal to 32,768Hz. The LSI and LSE oscillators can be enabled by the LSIEN and LSEEN control bits in the RTCCR register respectively. In addition, the LSE oscillator startup mode can be selected by configuring the LSESM bit in the RTCCR register. This enables the LSE oscillator to have either a shorter startup time or a lower power consumption. It is a trade-off between startup time and power consumption depending upon specific application requirements. An example of the startup time and the power consumption for different startup modes are shown in the accompanying table for reference.

Table 39. LSE Startup Mode Operating Current and Startup Time

Startup Mode	LSESM Setting in the RTCCR Register	Operating Current	Startup Time
Normal startup	0	3μA	Above 200ms
Fast startup	1	8μA	Below 200ms

@ V_{DD}=3.3V and LSE clock=32,768Hz; these values are only for reference, actual values are dependent on the specification of the external 32.768kHz crystal.

RTC Counter Operation

The RTC provides a 32-bit up-counter which increments at the falling edge of the CK_SECOND clock and whose value can be read from the RTCCNT register asynchronously via the APB bus. A 32-bit compare register, RTCCMP, is provided to store the specific value to be compared with the RTCCNT content. This is used to define a pre-determined time interval. When the RTCCNT register content is equal to the RTCCMP register value, the match flag CMFLAG in the RTCSR register will be set by hardware and an interrupt or wakeup event can be sent according to the corresponding enable bits in the RTCIWEN register. The RTC counter will be either reset to zero or keep counting when the compare match event occurs, dependent upon the CMPCLR bit in the RTCCR register. For example, if the RPRE [3:0] is set to 0x0F, the RTCCMP register content is set to a decimal value of 60 and the CMPCLR bit is set to 1, then the CMFLAG bit will be set every minute. In addition, the OVFLAG bit in the RTCSR register will be set when the RTC counter overflows. A read operation on the RTCSR register clears the status flags including the CSECFLAG, CMFLAG and OVFLAG bits.

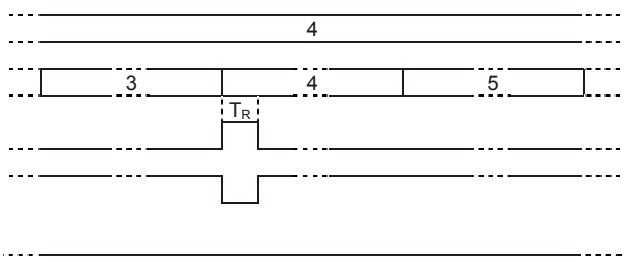
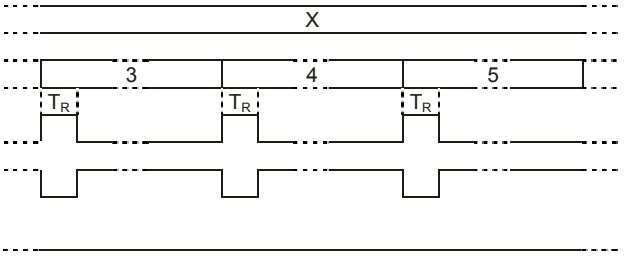
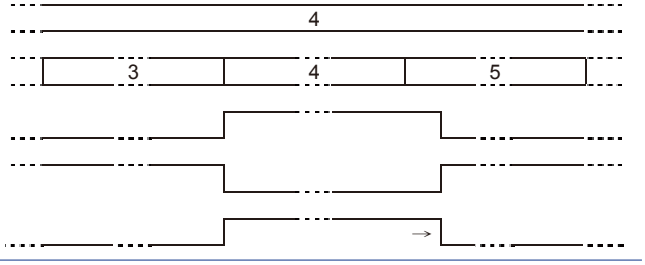
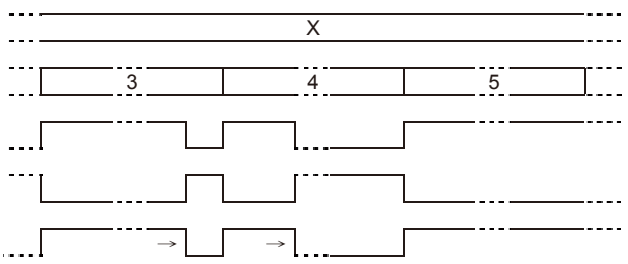
Interrupt and Wakeup Control

The falling edge of the CK_SECOND clock causes the CSECFLAG bit in the RTCSR register to be set and generates an interrupt if the corresponding interrupt enable bit, CSECIEN, in the RTCIWEN register is set. The wakeup event can also be generated to wake up the HSI/HSE oscillators, the PLL circuitry, the LDO and the Cortex™-M3 core if the corresponding wakeup enable bit CSECWEN is set. When the RTC counter overflows or a compare match event occurs, it will generate an interrupt or a wake up event determined by the corresponding interrupt or wakeup enable control bits, OVIEN/OVWEN or CMIEN/CMWEN bits, in the RTCIWEN register. Refer to the related register definitions for more details.

RTCOUT Output Pin Configuration

The following table shows RTCOUT output format according to the mode, polarity, and event selection setting.

Table 40. RTCOUT Output Mode and Active Level Setting

ROWM	ROES	RTCOUT Output Waveform
0 (Pulse mode)	0 Compare match	
	1 Second clock	
1 (Level mode)	0 Compare match	
	1 Second clock	

T_R: RTCOUT output pulse time=1/f_{CK_RTC}
→: Clear by software reading ROLF bit

Register Map

The following table shows the RTC registers and reset values. Note all the registers in this unit are located at the V_{BAK} backup power domain.

Table 41. RTC Register Map

Register	Offset	Description	Reset Value
RTC Base Address=0x4006_A000			
RTCCNT	0x000	RTC Counter Register	0x0000_0000
RTCCMP	0x004	RTC Compare Register	0x0000_0000
RTCCR	0x008	RTC Control Register	0x0000_0F04
RTCSR	0x00C	RTC Status Register	0x0000_0000
RTCIWEN	0x010	RTC Interrupt and Wakeup Enable Register	0x0000_0000

Register Descriptions

RTC Counter Register – RTCCNT

This register defines a 32-bit up counter which is increased by the CK_SECOND clock.

Address: 0x000

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	RTCCNTV							
Type/Reset	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0
	23	22	21	20	19	18	17	16
	RTCCNTV							
Type/Reset	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0
	15	14	13	12	11	10	9	8
	RTCCNTV							
Type/Reset	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0
	7	6	5	4	3	2	1	0
	RTCCNTV							
Type/Reset	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0

Bits	Field	Descriptions
[31:0]	RTCCNTV	RTC Counter Value The current value of the RTC counter is returned when reading the RTCCNT register. The RTCCNT register is updated during the falling edge of the CK_SECOND. This register is reset by one of the following conditions: – Backup Domain software reset – set the BAKRST bit in the BAKCR register – Backup Domain power on reset – PORB – Compare match (RTCCNTV=RTCCMPV) when CMPCLR=1 (in the RTCCR register) – RTCEN bit changed from 0 to 1

RTC Compare Register – RTCCMP

This register defines a specific value to be compared with the RTC counter value.

Address: 0x004

Reset value: 0x0000_0000 (Reset by Backup Domain reset only)

	31	30	29	28	27	26	25	24
	RTCCMPV							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	RTCCMPV							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	RTCCMPV							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	RTCCMPV							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[31:0]	RTCCMPV	RTC Compare Match Value A match condition happens when the value in the RTCCNT register is equal to RTCCMP value. An interrupt can be generated if the CMIEN bit in the RTCIWEN register is set. When the CMPCLR bit in the RTCCR register is set to 0 and a match condition happens, the CMFLAG bit in the RTCSR register is set while the value in the RTCCNT register is not affected and will continue to count until overflow. When the CMPCLR bit is set to 1 and a match condition happens, the CMFLAG bit in the RTCSR register is set and the RTCCNT register will be reset to zero and then the counter continues to count.

RTC Control Register – RTCCR

This register specifies a range of RTC circuitry control bits.

Address: 0x008

Reset value: 0x0000_0F04 (Reset by Backup Domain reset only)

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	Reserved			ROLF	ROAP	ROWM	ROES	ROEN
Type/Reset				RC 0	RW 0	RW 0	RW 0	RW 0
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	Reserved				RPRE			
Type/Reset					RW 1	RW 1	RW 1	RW 1
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
		Reserved	LSESM	CMPCLR	LSEEN	LSIEN	RTCSRC	RTCEN
Type/Reset			RW 0	RW 0	RW 0	RW 1	RW 0	RW 0

Bits	Field	Descriptions
[20]	ROLF	RTCOUT Level Mode Flag 0: RTCOUT Output is inactive 1: RTCOUT Output is holding as active level Set by hardware when level mode (ROWM=1) and a RTCOUT output event occurred. Cleared by software reading this flag. The RTCOUT signal will return to the inactive level after software has read this bit.
[19]	ROAP	RTCOUT Output Active Polarity 0: Active level is high 1: Active level is low
[18]	ROWM	RTCOUT Output Waveform Mode 0: Pulse mode The output pulse duration is one RTC clock (CK_RTC) period. 1: Level mode The RTCOUT signal will remain at an active level until the ROLF bit is cleared by software reading the ROLF bit.
[17]	ROES	RTCOUT Output Event Selection 0: RTC compare match is selected 1: RTC second clock (CK_SECOND) event is selected The ROES bit can be used to select whether the RTCOUT signal is output on the RTCOUT pin when a RTC compare match event or the RTC second clock (CK_SECOND) event occurs.
[16]	ROEN	RTCOUT Output Pin Enable 0: Disable RTCOUT output pin 1: Enable RTCOUT output pin When the ROEN bit is set to 1, the RTCOUT signal will be at an active level once a RTC compare match on the RTC second clock (CK_SECOOD) event occurs. The active polarity and output waveform mode can be configured by the ROAP and ROWM bits respectively. When the ROEN bit is cleared to 0, the RTCOUT pin will be in a floating state.

Bits	Field	Descriptions
[11:8]	RPRE	RTC Clock Prescaler Select CK_SECOND=CK_RTC/2^{RPRE} b0000: CK_SECOND=CK_RTC/2^0 b0001: CK_SECOND=CK_RTC/2^1 b0010: CK_SECOND=CK_RTC/2^2 … b1111: CK_SECOND=CK_RTC/2^{15}
[5]	LSESM	LSE oscillator Startup Mode 0: Normal startup and requires less operating power 1: Fast startup but requires higher operating current
[4]	CMPCLR	Compare Match Counter Clear 0: 32-bit RTC counter is not affected when compare match condition occurs 1: 32-bit RTC counter is cleared when compare match condition occurs
[3]	LSEEN	LSE oscillator Enable Control 0: LSE oscillator disabled 1: LSE oscillator enabled
[2]	LSIEN	LSI oscillator Enable Control 0: LSI oscillator disabled 1: LSI oscillator enabled The LSIEN bit default value is 1 which means the LSI oscillator is enabled automatically after the Backup Domain powered up. **Note:** After the backup domain is powered on, the internal LSI RC oscillator will start to oscillate. The frequency range of the LSI oscillator is shown in the LSI oscillator electrical characteristics in the datasheet. The device also provides a production trim value to obtain a more accurate oscillation frequency. The procedure is to disable the LSI oscillator and then enable it again after the backup domain is powered on. After the trimming procedure has completed, the system will automatically load the production trim value to the frequency trimming circuit of the LSI RC oscillator.
[1]	RTCSRC	RTC Clock Source Selection 0: LSI oscillator selected as the RTC clock source 1: LSE oscillator selected as the RTC clock source
[0]	RTCEN	RTC Enable Control 0: RTC is disabled 1: RTC is enabled

RTC Status Register – RTCSR

This register stores the counter flags.

Address: 0x00C

Reset value: 0x0000_0000 (Reset by Backup Domain reset and RTCEN bit change from 1 to 0)

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved					OVFLAG	CMFLAG	CSECFLAG
Type/Reset						RC 0	RC 0	RC 0

Bits	Field	Descriptions
[2]	OVFLAG	Counter Overflow Flag 0: Counter overflow has not occurred since the last RTCSR register read operation 1: Counter overflow has occurred since the last RTCSR register read operation This bit is set by hardware when the counter value in the RTCCNT register changes from 0xFFFF_FFFF to 0x0000_0000 and cleared by read operation. This bit is suggested to read in the RTC IRQ handler and should be taken care when software polling is used.
[1]	CMFLAG	Compare Match Condition Flag 0: Compare match condition has not occurred since the last RTCSR register read operation 1: Compare match condition has occurred since the last RTCSR register read operation This bit is set by hardware on the CK_SECOND clock falling edge when the RTCCNT register value is equal to the RTCCMP register content. It is cleared by software reading this bit. This bit is suggested for access in the corresponding RTC interrupt routine – do not use software polling during software free running.
[0]	CSECFLAG	CK_SECOND Occurrence Flag 0: CK_SECOND has not occurred since the last RTCSR register read operation 1: CK_SECOND has occurred since the last RTCSR register read operation This bit is set by hardware on the CK_SECOND clock falling edge. It is cleared by software reading this bit. This bit is suggested for access in the corresponding RTC interrupt routine – do not use software polling during software free running.

RTC Interrupt and Wakeup Enable Register – RTCIWEN

This register contains the interrupt and wakeup enable bits.

Address: 0x010

Reset value: 0x0000_0000 (Reset by Backup Domain reset only)

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved					OVWEN	CMWEN	CSECWEN
Type/Reset						RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	Reserved					OVIEN	CMIEN	CSECIEN
Type/Reset						RW 0	RW 0	RW 0

Bits	Field	Descriptions
[10]	OVWEN	Counter Overflow Wakeup Enable 0: Counter overflow wakeup disabled 1: Counter overflow wakeup enabled
[9]	CMWEN	Compare Match Wakeup Enable 0: Compare match wakeup disabled 1: Compare match wakeup enabled
[8]	CSECWEN	Counter Clock CK_SECOND Wakeup Enable 0: Counter Clock CK_SECOND wakeup disabled 1: Counter Clock CK_SECOND wakeup enabled
[2]	OVIEN	Counter Overflow Interrupt Enable 0: Counter Overflow Interrupt disabled 1: Counter Overflow Interrupt enabled
[1]	CMIEN	Compare Match Interrupt Enable 0: Compare Match Interrupt disabled 1: Compare Match Interrupt enabled
[0]	CSECIEN	Counter Clock CK_SECOND Interrupt Enable 0: Counter Clock CK_SECOND Interrupt disabled 1: Counter Clock CK_SECOND Interrupt enabled

18 Watchdog Timer (WDT)

Introduction

The Watchdog Timer is a hardware timing circuitry that can be used to detect system failures due to software malfunctions. It includes a 12-bit down-counting counter, a prescaler, a WDT counter value register, a WDT delta value register, interrupt related circuits, WDT operation control circuitry and the WDT protection mechanism. The Watchdog Timer can be operated in an interrupt mode or a reset mode. The Watchdog Timer will generate an interrupt or a reset when the counter counts down and reaches a zero value. If the software does not reload the counter value before the Watchdog Timer underflow occurs, an interrupt or a reset will be generated when the counter underflows. In addition, an interrupt or reset is also generated if the software reloads the counter when the counter value is greater than or equal to the WDT delta value. That means the counter must be reloaded within a limited timing window using a specific method. The Watchdog Timer counter can be stopped while the processor is in the debug mode. The register write protection function can be enabled to prevent it from changing the configuration of the Watchdog Timer unexpectedly.

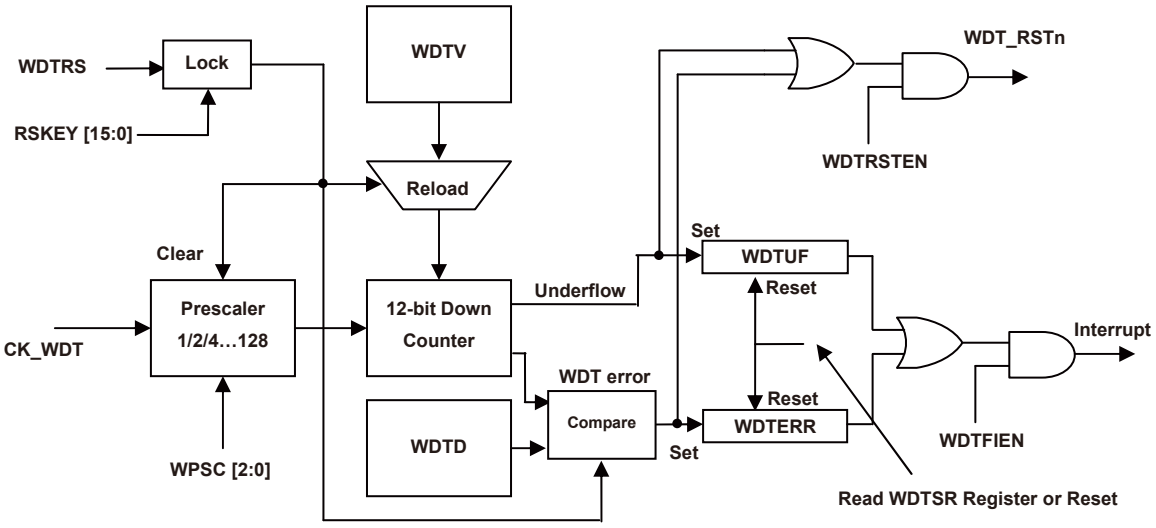


Figure 114. Watchdog Timer Block Diagram

Features

- 12-bit down counter with 3-bit prescaler
- Clock source from either internal 32kHz RC oscillator (LSI) or external 32,768Hz oscillator (LSE)
- Provides reset or interrupt signals to the system
- Limited reload window setting to prevent unsuitable Watchdog Timer reloads
- Watchdog Timer can be selected to be stopped or not while the processor is in the debug state
- Reload lock key to prevent unexpected operation
- Write protection function for register configuration (counter value, interrupt enable, reset enable, delta value, and prescaler)

Functional Descriptions

The Watchdog Timer consists of a 7-stage prescaler and a 12-bit down-counter. The largest time-out period is about 16 seconds using the maximum prescaler value of 1/128.

The configurations of the counter reload value, the interrupt enable, the reset enable, the Delta value and the prescaler selection in the WDTMR0 and WDTMR1 registers must be set properly before the Watchdog Timer starts to count. In order to prevent an unexpected write operation to these configurations, a register write protection function should be enabled by writing any value except the value 0x35CA to the PROTECT [15:0] bits in the WDTPR register. The value 0x35CA can be written into the PROTECT [15:0] bits to disable the register write protection function before accessing the configuration register. The read operation of the PROTECT [0] bit can obtain the enable/disable status of the register write protection function.

During normal operation, the Watchdog Timer counter should be reloaded before the counter underflows to avoid generating an interrupt or a reset. The 12-bit down counter can be reloaded with the Watchdog Timer Counter Value (WDTV) by setting WDTRS to 1 together with correct lock key 0x5FA0 specified in the WDTCR register.

If a software deadlock situation occurs in a task or a subroutine is contained within a WDT reload operation, then the reload operation will continue to function and a Watchdog Timer underflow reset or interrupt will not be generated. This will result in the software deadlock remaining undetected. To prevent this situation, the reload operation is designated to be executed when the WDT counter value is less than the WDT delta value, WDTD. A reload operation is only executed when the WDT counter value is greater than or equal to the WDT delta value which will then cause a Watchdog Timer error which generates an interrupt or reset depending on the related setting. With a proper WDT delta value being specified, if a software deadlock occurs in a task or if a subroutine is contained within a WDT reload operation, the WDT reload operation will not be executed and a WDT error interrupt or a WDT error reset will be generated to obtain CPU attention. However, the delta value feature described can be disabled by programming the WDTD to have a value greater than or equal to the WDTV value.

The WDTERR flag and the WDTUF flag in the WDTSR register will be set respectively when the Watchdog Timer underflows or the Watchdog Timer error occurs. A system reset or the read operation of the WDTSR register clears the WDTERR flag and the WDTUF flag.

When the processor enters the debug mode, the Watchdog Timer counter will either continue to count or stop, depending on the DB_WDT bit configuration in the MCUDBGCR register in the Clock Control Unit.

The following method shows how the Watchdog Timer is setup and used:

- Configure the Watchdog Timer reload value WDTV and the reset or interrupt control in the WDTMR0 register
- Configure the Watchdog Timer delta value WDTD and the prescaler selection in the WDTMR1 register
- Reload the Watchdog Timer by setting the RSKEY field to 0x5FA0 and the WDTRS bit to 1 in the WDTCR register
- Write any value except 0x35CA into the WDTPR register to lock all Watchdog Timer registers except the WDTCR and the WDTPR registers
- The Watchdog Timer counter should be reloaded again within the delta value (WDTD)

Note: The WDT will stop counting if the APB clock is stopped or the WDTEN bit in the APBCCR1 register is disabled.

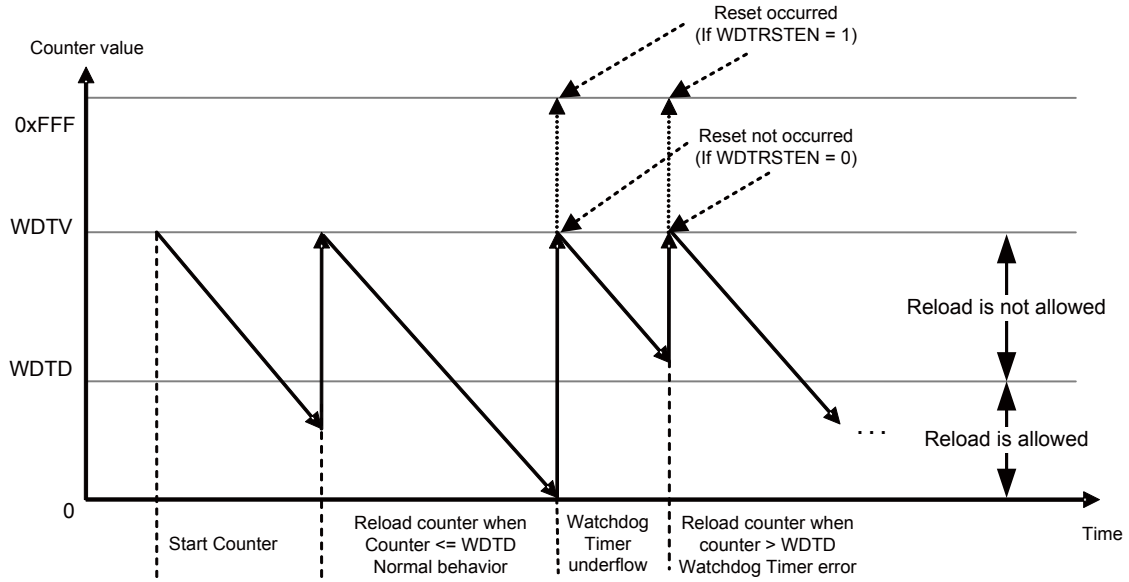


Figure 115. Watchdog Timer Behavior

Register Map

The following table shows the Watchdog Timer registers and reset values.

Table 42. WDT Register Map

Register	Offset	Description	Reset Value
Watchdog Timer Base Address=0x4006_8000			
WDTCR	0x000	Watchdog Timer Control Register	0x0000_0000
WDTMR0	0x004	Watchdog Timer Mode Register 0	0x0000_0FFF
WDTMR1	0x008	Watchdog Timer Mode Register 1	0x0000_7FFF
WDTSR	0x00C	Watchdog Timer Status Register	0x0000_0000
WDTPR	0x010	Watchdog Timer Protection Register	0x0000_0000

Register Descriptions

Watchdog Timer Control Register – WDTCR

This register is used to reload the Watchdog Timer.

Offset: 0x000

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	RSKEY							
Type/Reset	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	RSKEY							
Type/Reset	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	Reserved							
Type/Reset								
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	Reserved							WDTRS
Type/Reset								WO 0

Bits	Field	Descriptions
[31:16]	RSKEY	Watchdog Timer Reload Lock Key The RSKEY [15:0] bits should be written with a value of 0x5FA0 to enable the WDT reload operation function. Writing any other value except 0x5FA0 in this field will abort the write operation.
[0]	WDTRS	Watchdog Timer Reload 0: No operation 1: Reload Watchdog Timer This bit is used to reload the Watchdog Timer Counter with a WDTV value stored in the WDTMR0 register. It is set to 1 by software and cleared to 0 by hardware automatically.

Watchdog Timer Mode Register 0 – WDTMR0

This register specifies the Watchdog Timer counter reload value, interrupt enable and reset enable control.

Offset: 0x004

Reset value: 0x0000_0FFF

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved		WDTRSTEN	WDTFIEN	WDTV			
Type/Reset			RW 0	RW 0	RW 1	RW 1	RW 1	RW 1
	7	6	5	4	3	2	1	0
	WDTV							
Type/Reset	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1

Bits	Field	Descriptions
[13]	WDTRSTEN	Watchdog Timer Reset Enable 0: A Watchdog Timer underflow or error event has no effect on the reset operation 1: A Watchdog Timer underflow or error event triggers a Watchdog Timer reset
[12]	WDTFIEN	Watchdog Timer Fault Interrupt Enable 0: A Watchdog Timer underflow or error has no effect on interrupt 1: A Watchdog Timer underflow or error asserts an interrupt
[11:0]	WDTV	Watchdog Timer Counter Value WDTV defines the value loaded in the 12-bit Watchdog down Counter.

Watchdog Timer Mode Register 1 – WDTMR1

This register specifies the Watchdog delta value and the prescaler selection.

Offset: 0x008

Reset value: 0x0000_7FFF

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved	WPSC			WDTD			
Type/Reset		RW 1	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1
	7	6	5	4	3	2	1	0
	WDTD							
Type/Reset	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1

Bits	Field	Descriptions
[14:12]	WPSC	Watchdog Timer Prescaler Selection 000: 1/1 001: 1/2 010: 1/4 011: 1/8 100: 1/16 101: 1/32 110: 1/64 111: 1/128
[11:0]	WDTD	Watchdog Timer Delta Value WDTD is used to define the permitted range to reload the Watchdog Timer. If the Watchdog Timer counter value is less than the WDTD value, writing the WDTCR register with the setting including WDTRS=1 and RSKEY=0x5FA0 to execute a WDT reload operation will successfully reload the timer. If the Watchdog Timer value is greater than or equal to the WDTD value, writing the WDTCR register with the setting including WDTRS=1 and RSKEY=0x5FA0 to execute a WDT reload operation will cause a Watchdog Timer error. This feature can be disabled by programming the WDTD value to be greater than or equal to the WDTV value.

Watchdog Timer Status Register – WDTSR

This register specifies the Watchdog Timer status.

Offset: 0x00C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved						WDTERR	WDTUF
Type/Reset							RC 0	RC 0

Bits	Field	Descriptions
[1]	WDTERR	Watchdog Timer Error 0: No Watchdog Timer error occurred since the last read operation on this register 1: Watchdog Timer error occured since the last read operation on this register **Note:** A reload operation will cause a Watchdog Timer error when the Watchdog Timer counter value is greater than or equal to the WDTD value.
[0]	WDTUF	Watchdog Timer Underflow 0: No Watchdog Timer underflow occurred since the last read operation on this register 1: Watchdog Timer underflow occurred since the last read operation on this register

Watchdog Timer Protection Register – WDTPR

This register specifies the Watchdog Timer write protection key configuration.

Offset: 0x010

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	PROTECT							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	PROTECT							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	PROTECT	Watchdog Timer Register Protection For write operation: 0x35CA: Disable the Watchdog Timer register write protection Other values: Enable the Watchdog Timer register write protection For read operation: 0x0000: Watchdog Timer register write protection disabled 0x0001: Watchdog Timer register write protection enabled This register is used to enable or disable the write protection of WDTMR0 and WDTMR1 registers. Enable write protection will make WDTMR0 and WDTMR1 registers become read only to prevent any unexpected write operation. Read the WDTPR register to indicate if the write protection is enabled or not.

19 Inter-Integrated Circuit (I²C0 & I²C1)

Introduction

The I²C Module is an internal circuit allowing communication with an external I²C interface which is an industry standard two line serial interface used for connection to external hardware. These two serial lines are known as a serial data line, SDA, and a serial clock line, SCL. The I²C module provides three data transfer rates: (1) 100kHz in the Standard mode, (2) 400kHz in the Fast mode and (3) 1MHz in the Fast-mode plus. The SCL period generation register is used to setup different kinds of duty cycle implementation for the SCL pulse.

The SDA line which is connected to the whole I²C bus is a bi-directional data line between the master and slave devices used for the transmission and reception of data. The I²C module also has an arbitration detection function to prevent the situation where more than one master attempts to transmit data on the I²C bus at the same time.

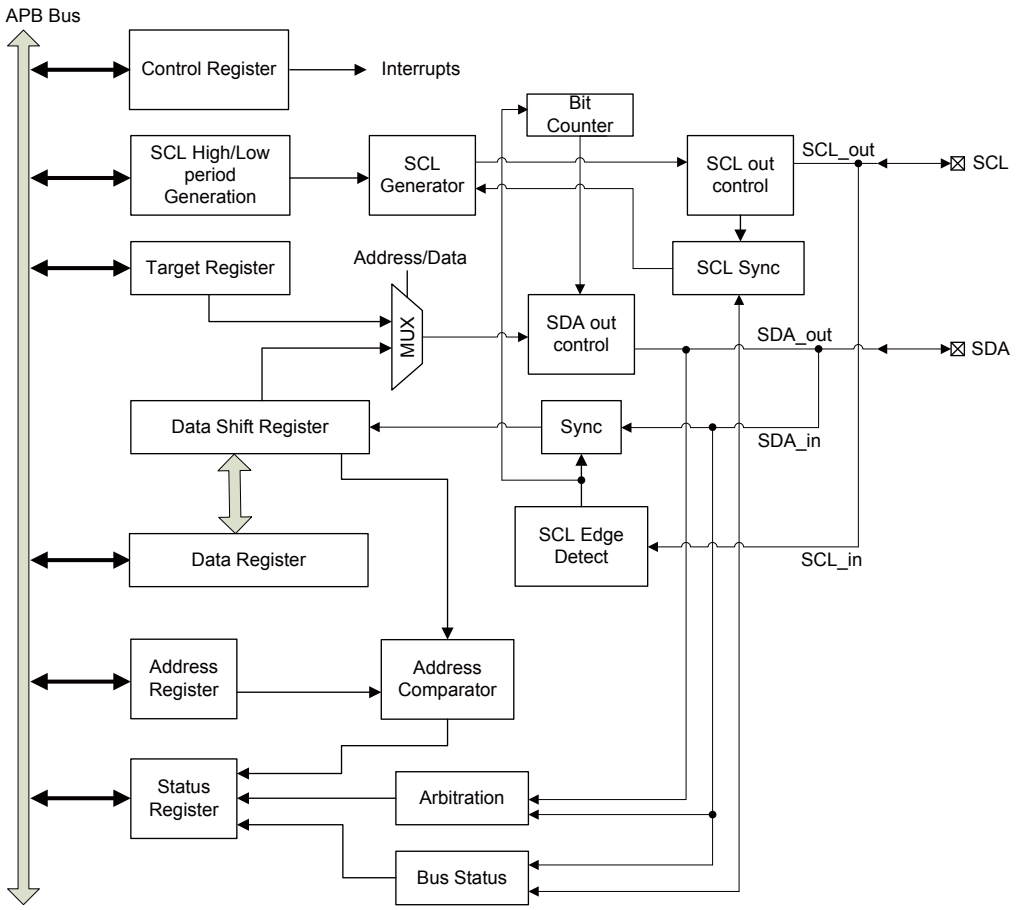


Figure 116. I²C Module Block Diagram

Features

- Two-wire I²C serial interface
  - Serial data line (SDA) and serial clock (SCL)
- Multiple speed modes
  - Standard mode – 100kHz
  - Fast mode – 400kHz
  - Fast mode plus – 1MHz
- Bi-directional data transfer between master and slave
- Multi-master bus – no central master
  - The same interface can act as Master or Slave
- Arbitration among simultaneously transmitting masters without corrupting of serial data on the bus
- Clock synchronization
  - Allow devices with different bit rates to communicate via one serial bus
- 7-bit and 10-bit addressing mode and general call addressing
- Multiple slave addresses using address mask function
- Time-out function
- Supports PDMA Interface

Functional Descriptions

Two Wire Serial Interface

The I²C module has two external lines, the serial data SDA and serial clock SCL lines, to carry information between the interconnected devices connected to the bus. The SCL and SDA lines are both bidirectional and must be connected to a pull-high resistor. When the I²C bus is in the free or idle state, both pins are at a high level to perform the required wired-AND function for multiple connected devices.

START and STOP Conditions

A master device can initialize a transfer by sending a START signal and terminate the transfer with a STOP signal. A START signal is usually referred to as the “S” bit, which is defined as a High to Low transition on the SDA line while the SCL line is high. A STOP signal is usually referred to as the “P” bit, which is defined as a Low to High transition on the SDA line while the SCL line is high.

A repeated START, which is denoted as the “Sr” bit, is functionally identical to the normal START condition. A repeated START signal allows the I²C interface to communicate with another slave device or with the same device but in a different transfer direction without releasing the I²C bus control.

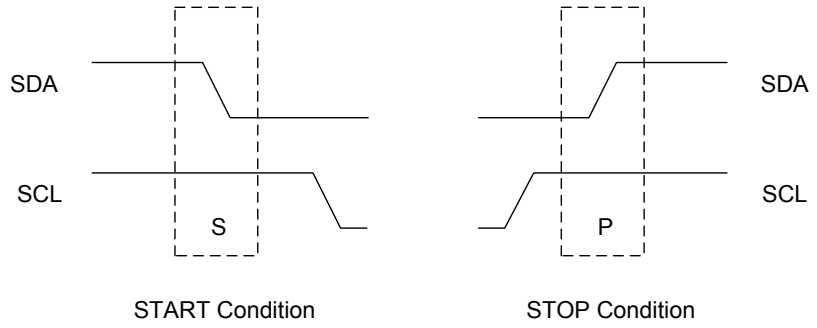


Figure 117. START and STOP Condition

Data Validity

The data on the SDA line must be stable during the high period of the SCL clock. The SDA data state can only be changed when the clock signal on the SCL line is in a low state.

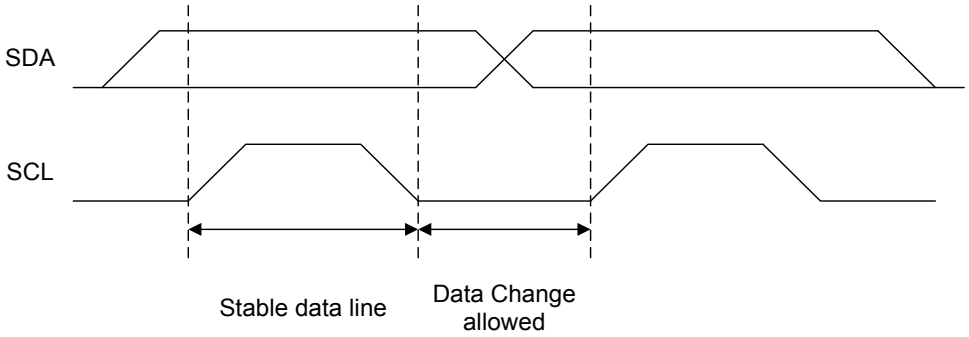


Figure 118. Data Validity

Addressing Format

The I²C interface starts to transfer data after the master device has sent the address to confirm the targeted slave device. The address frame is sent just after the START signal by master device. The addressing mode selection bit named ADRM in the I2CCR register should be defined to choose either the 7-bit or 10-bit addressing mode.

7-bit Address Format

The 7-bit address format is composed of the seven-bit length slave address, which the master device wants to communicate with a R/$\overline{W}$ bit and an ACK bit. The R/$\overline{W}$ bit defines the direction of the data transfer.

R/$\overline{W}$=0 (Write): The master transmits data to the addressed slave.

R/$\overline{W}$=1 (Read): The master receives data from the addressed slave.

The slave address can be assigned through the ADDR field in the I2CADDR register. The slave device sends back the acknowledge bit (ACK) if its slave address matches the transmitted address sent by master.

Note that it is forbidden to own the same address for two slave devices.

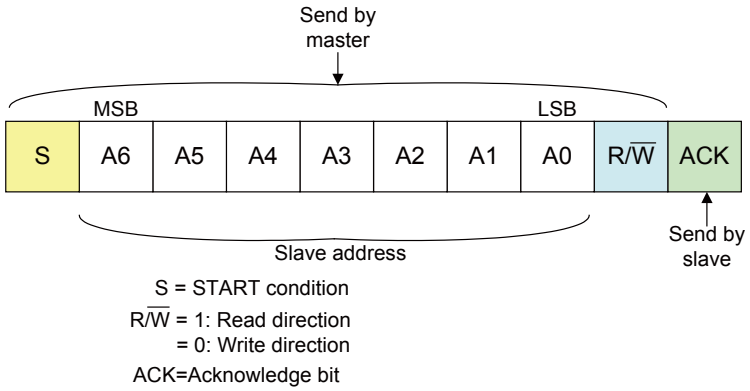
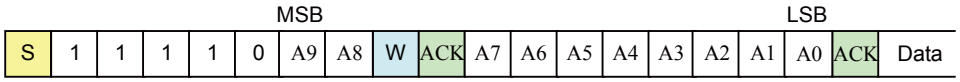


Figure 119. 7-bit Addressing Mode

10-bit Address Format

In order to prevent address clashes, due to the limited range of the 7-bit addresses, a new 10-bit address scheme has been introduced. This enhancement can be mixed with the 7-bit addressing mode which increases the available address range about ten times. For the 10-bit addressing mode, the first two bytes after a START signal include a header byte and an address byte that usually determines which slave will be selected by the master. The header byte is composed of a leading "11110", 10th and 9th bits of the slave address. The second byte is the remaining 8 bit address of the slave device.



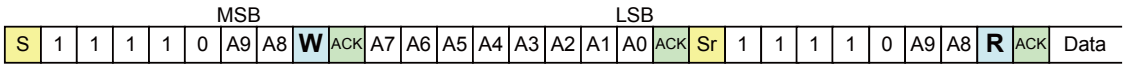
S = START condition

W = Write command

ACK = Acknowledge

A9 ~ A0 = 10-bits Address

Figure 120. 10-bit Addressing Write Transmit Mode



S = START condition

Sr = Repeated-START condition

W = Write command

R = Read command

ACK = Acknowledge

A9 ~ A0 = 10-bits Address

Figure 121. 10-bit Addressing Read Receive Mode

Data Transfer and Acknowledge

Once the slave device address has been matched, the data can be transmitted to or received from the slave device according to the transfer direction specified by the R/$\overline{W}$ bit. Each byte is followed by an acknowledge bit on the 9th SCL clock

If the slave device returns a Not Acknowledge (NACK) signal to the master device, the master device can generate a STOP signal to terminate the data transfer or generate a repeated START signal to restart the transfer.

If the master device sends a Not Acknowledge (NACK) signal to the slave device, the slave device should release the SDA line for the master device to generate a STOP signal to terminate the transfer.

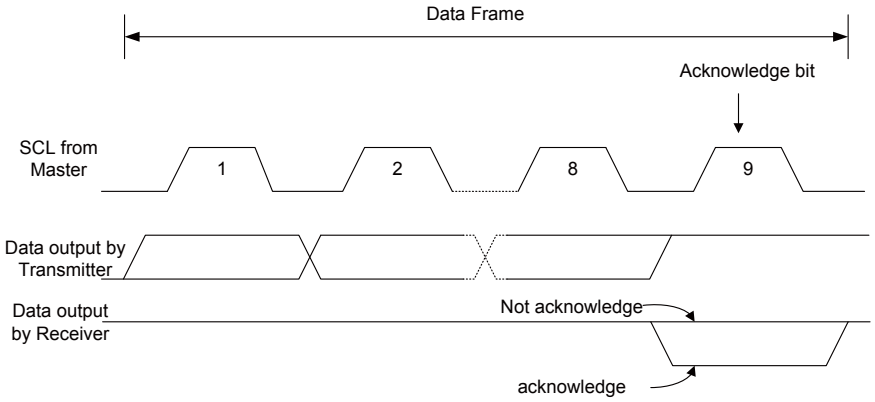


Figure 122. I²C Bus Acknowledge

Clock Synchronization

Only one master device can generate the SCL clock under normal operation. However when there is more than one master trying to generate the SCL clock, the clock should be synchronized so that the data output can be compared. Clock synchronization is performed using the wired-AND connection of the I²C interface to the SCL line.

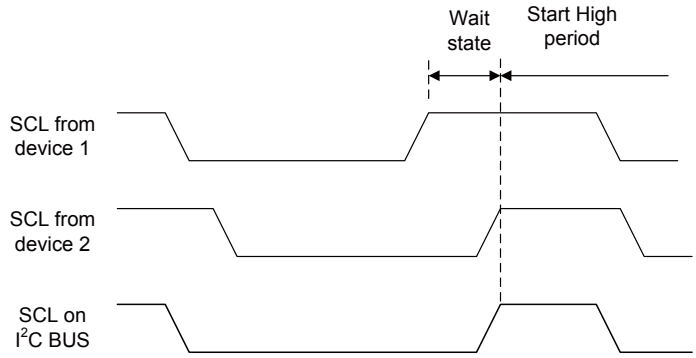


Figure 123. Clock Synchronization during Arbitration

Arbitration

A master may start a transfer only if the I²C bus line is in the free or idle mode. If two or more masters generate a START signal at approximately the same time, an arbitration procedure will occur.

Arbitration takes place on the SDA line and can continue for many bits. The arbitration procedure gives a higher priority to the device that transmits serial data with a binary low bit (logic low). Other master devices which want to transmit binary high bits (logic high) will lose the arbitration. As soon as a master loses the arbitration, the I²C module will set the ARBLOS bit in the I2CSR register and generate an interrupt if the interrupt enable bit, ARBLSIEN, in the I2CIER register is set to 1. Meanwhile, it stops sending data and listens to the bus in order to detect an I²C stop signal. When the stop signal is detected, the master which has lost the arbitration may try to access the bus again.

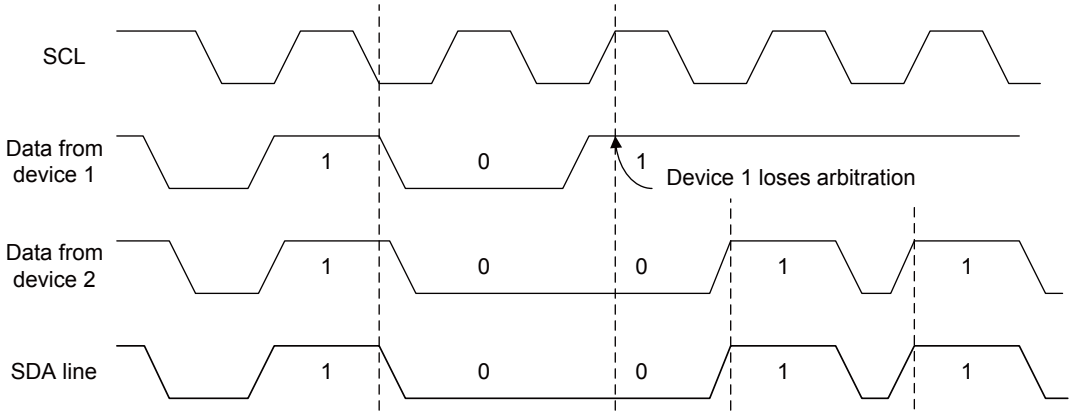


Figure 124. Two Master Arbitration Procedure

General Call Addressing

The general call addressing function can be used to address all the devices connected to the I²C bus. The master device can activate the general call function by writing 00 into the TAR and setting the RWD bit to 0 in the I2CTAR register on the addressing frame.

The device can support the general call addressing function by setting the corresponding enable control bit GCEN to 1. If the GCEN bit is set to 1 to support the general call addressing, the AA bit in the I2CCR register should also be set to 1 to send an acknowledge signal back when the device receives an address frame with a value of 00H. When this condition occurs, the general call flag, GCS, will be set to 1, but the ADRS flag will not be set.

Bus Error

If an unpredictable START or STOP condition occurs when the data is being transferred on the I²C bus, it will be considered as a bus error and the transferring data will be aborted. When a bus error event occurs, the relevant bus error flag BUSERR in the I2CSR register will set to 1 and both the SDA and SCL lines are released. The BUSERR flag should be cleared by writing 1 to it to initiate the I²C module to an idle state.

Address Mask

The I²C module in the HT32F1755/1765/2755 series of devices provides address mask function for user to decide which address bit can be ignored during the comparison with the address frame sent from the master. The ADRS flag will be asserted when the unmasked address bits and the address frame sent from the master are matched. Note that this function is only available in the slave mode.

For instance, the user sets a data transfer with 7-bit addressing mode together with the I2CADDMR register value as 0x05h and the I2CADDR register value as 0x55h, this means if an address which is sent by an I²C master on the bus is equal to 0x50h, 0x51h, 0x54h or 0x55h, the I²C slave address will all be considered to be matched and the ADRS flag in the I2CSR register will be asserted after the address frame.

Address Snoop

The Address Snoop register, I2CADDSR, is used to monitor the calling address on the I²C bus during the whole data transfer operation no matter if the I²C module operates as a master or a slave device. Note that the I2CADDSR register is a read only register and each calling address on the I²C bus will be stored in the I2CADDSR register automatically even if the I²C device is not addressed.

Operation Mode

The I²C module can operate in one of the following modes:

- Master Transmitter
- Master Receiver
- Slave Transmitter
- Slave Receiver

The I²C module operates in the slave mode by default. The interface will switch to the master mode automatically after generating a START signal.

Master Transmitter Mode

Start Condition

Users write the target slave device address and communication direction into the I2CTAR register after setting the I2CEN bit in the I2CCR register. The STA flag in the I2CSR register is set by hardware after a start condition occurs. In order to send the following address frame, the STA flag must be cleared to 0 if it has been set to 1. The STA flag is cleared by reading the I2CSR register.

Address Frame

The ADRS flag in the I2CSR register will be set after the address frame is sent by the master device and the acknowledge signal from the address matched slave device is received. In order to send the following data frame, the ADRS flag must be cleared to 0 if it has been set to 1. The ADRS bit is cleared by reading the I2CSR register.

Data Frame

The data to be transmitted to the slave device must be transferred to the I2CDR register.

The TXDE bit in the I2CSR register is set to indicate that the I2CDR register is empty, which results in the SCL line being held at a logic low state. New data must then be transferred to the I2CDR register to continue the data transfer process. Writing data into the I2CDR register will clear the TXDE flag.

Close/Continue Transmission

After transmitting the last data byte, the STOP bit in the I2CCR register can be set to terminate the transmission or re-assign another slave device by configuring the I2CTAR register to restart a new transfer.

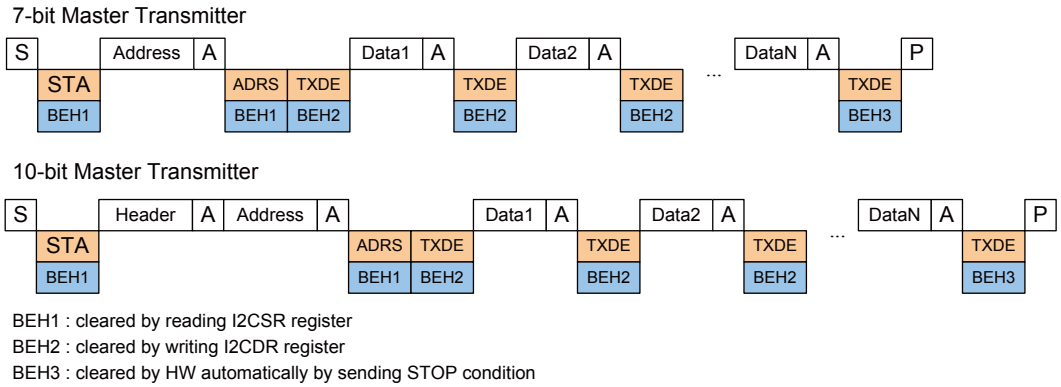


Figure 125. Master Transmitter Timing Diagram

Master Receiver Mode

Start Condition

The target slave device address and communication direction must be written into the I2CTAR register. The STA flag in the I2CSR register is set by hardware after a start condition occurs. In order to send the following address frame, the STA flag must be cleared to 0 if it has been set to 1. The STA flag is cleared by reading the I2CSR register.

Address Frame

In the 7-bit addressing mode: The ADRS flag is set after the address frame is sent by the master device and the acknowledge signal from the address matched slave device is received. In order to receive the following data frame, the ADRS bit must be cleared to 0 if it has been set to 1. The ADRS bit is cleared after reading the I2CSR register.

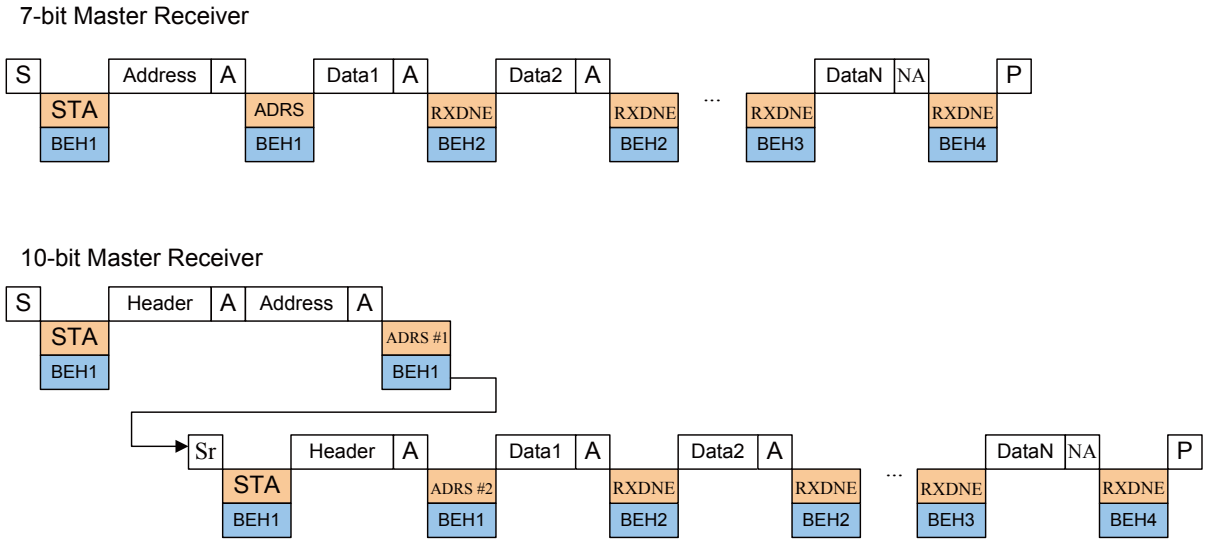
In the 10-bit addressing mode: The ADRS bit in the I2CSR register will be set twice in the 10-bit addressing mode. The first time the ADRS bit is set is when the 10-bit address is sent and the acknowledge signal from the slave device is received. The second time the ADRS bit is set is when the header byte is sent and the slave acknowledge signal is received. In order to receive the following data frame, the ADRS bit must be cleared to 0 if it has been set to 1. The ADRS bit is cleared after reading the I2CSR register. The detailed master receiver mode timing diagram is shown in the following figure.

Data Frame

In the master receiver mode, data is transmitted from the slave device. Once a data is received by the master device, the RXDNE flag in the I2CSR register is set but it will not hold the SCL line. However, if the device receives a complete new data byte and the RXDNE flag has already been set to 1, the RXBF bit in the I2CSR register will be set to 1 and the SCL line will be held at a logic low state. When this situation occurs, data from the I2CDR register should be read to continue the data transfer process. The RXDNE flag can be cleared after reading the I2CDR register.

Close/Continue Transmission

The master device needs to reset the AA bit in the I2CCR register to send a NACK signal to the slave device before the last data byte transfer has been completed. After the last data byte has been received from the slave device, the master device will hold the SCL line at a logic low state following after a NACK signal sent by the master device to the slave device. The STOP bit can be set to terminate the data transfer process or re-assign the I2CTAR register to restart a new transfer.



BEH1 : cleared by reading I2CSR register
BEH2 : cleared by reading I2CDR register
BEH3 : cleared by reading I2CDR register, set AA=0 to send NACK signal
BEH4 : cleared by reading I2CDR register, set STOP=1 to send STOP signal

Figure 126. Master Receiver Timing Diagram

Slave Transmitter Mode

Address Frame

In the 7-bit addressing mode, the ADRS bit in the I2CSR register is set after the slave device receives the calling address which matches with the slave device address. In the 10-bit addressing mode, the ADRS bit is set when the first header byte is matched and the second address byte is matched respectively. After the ADRS bit has been set to 1, it must be cleared to 0 to continue the data transfer process. The ADRS bit is cleared after reading the I2CSR register.

Data Frame

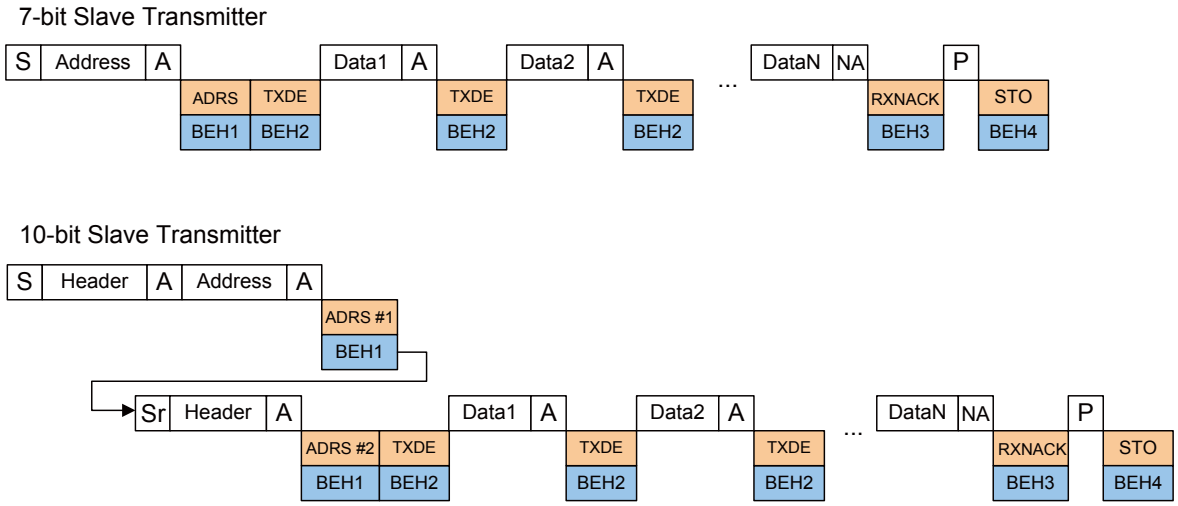
In the Slave transmitter mode, the TXDE bit is set to indicate that the I2CDR is empty, which results in the SCL line being held at a logic low state. New transmission data must then be written into the I2CDR register to continue the data transfer process. Writing data into the I2CDR register will clear the TXDE bit.

Receive Not-Acknowledge

When the slave device receives a Not-Acknowledge signal, the RXNACK bit in the I2CSR Register is set but it will not hold the SCL line. Writing 1 to RXNACK will clear the RXNACK flag.

STOP Condition

When the slave device detects a STOP condition, the STO bit in the I2CSR register is set to indicate that the I²C interface transmission is terminated. Reading the I2CSR register can clear the STO flag.



BEH1 : cleared by reading I2CSR register
BEH2 : cleared by writing I2CDR register
BEH3 : cleared by writing 1 to RXNACK flag, TXDE is not set when NACK is received.
BEH4 : cleared by reading I2CSR register

Figure 127. Slave Transmitter Timing Diagram

Slave Receiver Mode

Address Frame

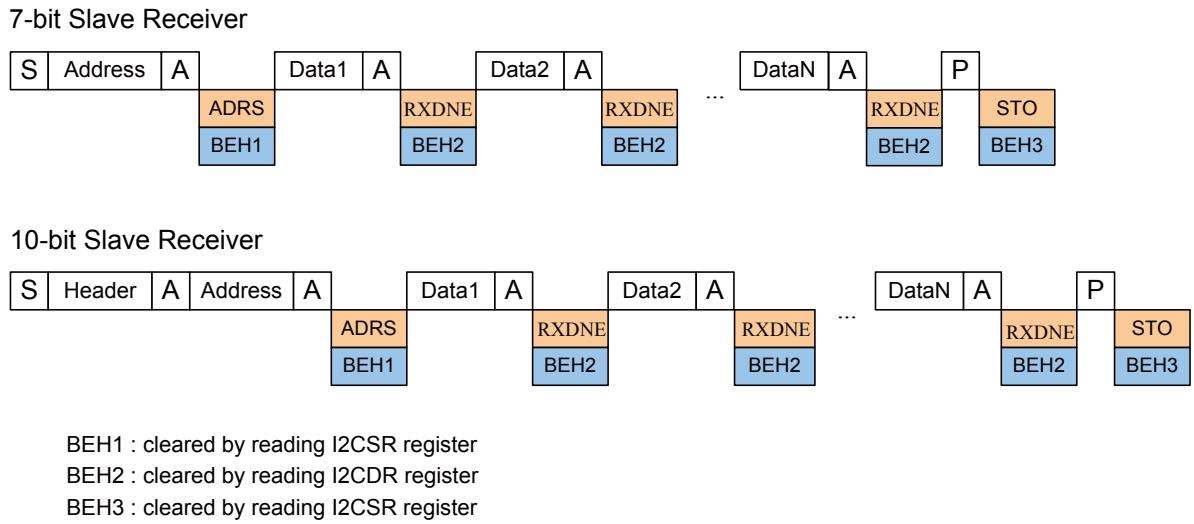
The ADRS bit in the I2CSR register is set after the slave device receives the calling address which matches with the slave device address. After the ADRS bit has been set to 1, it must be cleared to 0 to continue the data transfer process. The ADRS flag is cleared after reading the I2CSR register.

Data Frame

In the slave receiver mode, the data is transmitted from the master device. Once a data byte is received by the slave device, the RXDNE flag in the I2CSR register is set but it will not hold the SCL line. However, if the device receives a complete new data byte and the RXDNE bit has been set to 1, the RXBF bit in the I2CSR register will be set to 1 and the SCL line will be held at a logic low state. When this situation occurs, data from the I2CDR register should be read to continue the data transfer process. The RXDNE flag bit can be cleared after reading the I2CDR register.

STOP Condition

When the slave device detects a STOP condition, the STO flag bit in the I2CSR register is set to indicate that the I²C interface transmission is terminated. Reading the I2CSR register can clear the STO flag bit.



BEH1 : cleared by reading I2CSR register
BEH2 : cleared by reading I2CDR register
BEH3 : cleared by reading I2CSR register

Figure 128. Slave Receiver Timing Diagram

Holding SCL Line Conditions

The following conditions will cause the SCL line to be held at a logic low state by hardware resulting in all the I²C transfers being stopped. Data transfer will be continued after the creating conditions are eliminated.

Table 43. Conditions of Holding SCL line

Type	Condition	Description	Elimination
Flag	STA	Master device sends a START signal	Reading the I2CSR register
	ADRS	Master: The I²C module sends the address frame and receives an ACK signal from the slave device. **Note:** Refer to Figure 125. Master Transmitter Timing Diagram on page 442 and Figure 126. Master Receiver Timing Diagram on page 443. Slave: The I²C module is addressed as a slave device. **Note:** Refer to Figure 127. Slave Transmitter Timing Diagram on page 444 and Figure 128. Slave Receiver Timing Diagram on page 445.	Reading the I2CSR register
	TXDE	The I²C module is used in the transmitter mode and a new data byte to be transmitted is necessary to be loaded into the I2CDR register. **Note:** The TXDE bit will not be asserted after receiving a NACK signal.	Master case: Writing data to I2CDR register Set TAR Set STOP Slave case: Writing data to I2CDR register
	RXBF	The device received complete new data and the RXDNE flag has been set already.	Reading the I2CDR register
	GCS	The I²C module is addressed as a slave device through a general call.	Reading the I2CSR register
Event	Master receives NACK	No matter whether address or data frame, when the I²C module operating in the master mode receives a NACK signal, the SCL line will be held at a logic low state.	Set TAR Set STOP
	Master sends a NACK used in received mode	When the I²C module operating in the master receiver mode receives the last data byte, the SCL line will be held at a logic low state. **Note:** Refer to Figure 126. Master Receiver Timing Diagram on page 443 and the RXNACK flag will not be asserted in this case.	Set TAR Set STOP

I²C Timeout Function

In order to reduce the occurrence of I²C lockup problem due to the reception of erroneous clock source, a timeout function is provided. If the I²C bus clock source is not received for a certain timeout period, then a corresponding I²C timeout flag will be asserted. This timeout period is determined by a 16-bit down-counting counter with a programmable preload value. The timeout counter is driven by the I²C timeout clock, f_{I2CTO}, which is specified by the timeout prescaler field in the I2CTOUT register. The TOUT field in the I2CTOUT register is used to define the timeout counter preload value. The timeout function is enabled by setting the ENTOUT bit in the I2CCR register. The timeout counter will start to count down from the preloaded value if the ENTOUT bit is set to 1 and one of the following conditions occurs:

- The I²C master module sends a START signal.
- The I²C slave module detects a START signal.
- The RXBF, TXDE, RXDNE, RXNACK, GCS or ADRS flags are asserted.

The timeout counter will stop counting when the ENTOUT bit is cleared. However, the counter will also stop counting when the conditions, listed as follows occur:

- The I²C slave module is not addressed.
- The I²C slave module detects a STOP signal.
- The I²C master module sends a STOP signal.
- The ARBLOS or BUSERR flags in the I2CSR register are asserted.

If the timeout counter underflows, the corresponding timeout flag, TOUTF, in the I2CSR register will be set to 1 and a timeout interrupt will be generated if the relevant interrupt is enabled.

PDMA Interface

The PDMA interface is integrated in the I²C module. The PDMA function can be enabled by setting the TXDMAE or RXDMAE bit to 1 in the transmitter or receiver mode respectively. When the data register is empty in the transmitter mode and the TXDMAE bit is set to 1, the PDMA function will be activated to move data from the memory location that users designated into the I²C data register. Similarly, when the data register is not empty in the receiver mode and the RXDMAE bit is set to 1, the PDMA function will also be activated to move data from the I²C data register to the memory location that users designated.

The control bit, DMANACK, is used to send a NACK signal automatically to the slave in order to properly terminate the data transfer after receiving the last data byte when the I2C module uses the PDMA interface in the master receiver mode.

For a mode detailed description on the PDMA configurations, refer to the PDMA chapter.

Register Map

The following table shows the I²C registers and reset values.

Table 44. I²C Register Map

Register	Offset	Description	Reset Value
I²C0 Base Address=0x4004_8000 I²C1 Base Address=0x4004_9000			
I2CnCR	0x000	I²Cn Control Register	0x0000_0000
I2CnIER	0x004	I²Cn Interrupt Enable Register	0x0000_0000
I2CnADDR	0x008	I²Cn Address Register	0x0000_0000
I2CnSR	0x00C	I²Cn Status Register	0x0000_0000
I2CnSHPGR	0x010	I²Cn SCL High Period Generation Register	0x0000_0000
I2CnSLPGR	0x014	I²Cn SCL Low Period Generation Register	0x0000_0000
I2CnDR	0x018	I²Cn Data Register	0x0000_0000
I2CnTAR	0x01C	I²Cn Target Register	0x0000_0000
I2CnADDMR	0x020	I²Cn Address Mask Register	0x0000_0000
I2CnADDSR	0x024	I²Cn Address Snoop Register	0x0000_0000
I2CnTOUT	0x028	I²Cn Timeout Register	0x0000_0000

Register Descriptions

I²Cn Control Register – I2CnCR, n=0 or 1

This register specifies the corresponding I²Cn function enable control.

Offset: 0x000

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved			ENTOUT	Reserved	DMANACK	RXDMAE	TXDMAE
Type/Reset				RW 0		RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	ADRM	Reserved			I2CEN	GCEN	STOP	AA
Type/Reset	RW 0				RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[12]	ENTOUT	I²C Timeout Function Enable Control 0: Timeout Function disabled 1: Timeout Function enabled This bit is used to enable or disable the I²C timeout function. When the I2CEN bit is cleared to 0, the ENTOUT bit will be automatically cleared to 0 by hardware. It is recommended that users should properly configure the PSC and TOUT fields in the I2CnTOUT register before starting the timeout counter to count by setting the ENOUT bit to 1.
[10]	DMANACK	PDMA Mode NACK Control 0: No operation 1: The I²C master receiver module sends a NACK signal automatically after receiving the last byte from the slave transmitter in the PDMA mode When the I2CEN bit is cleared to 0, the DMANACK bit is automatically cleared to 0 by hardware.
[9]	RXDMAE	PDMA Mode RX Request Enable Control 0: RX PDMA request disabled 1: RX PDMA request enabled If the data register is not empty in the receiver mode and the RXDMAE bit is set to 1, the relevant PDMA channel will be activated to move the data from the data register to a specific location which is defined in the corresponding PDMA register. When the I2CEN bit is cleared to 0, the RXDMAE bit is automatically cleared to 0 by hardware.

Bits	Field	Descriptions
[8]	TXDMAE	PDMA Mode TX Request Enable Control 0: TX PDMA request disabled 1: TX PDMA request enabled If the data register is empty in the transmitter mode and the TXDMAE bit is set to 1, the relevant PDMA channel will be activated to move the data from a specific location defined in the corresponding PDMA register to the data register. When the I2CEN bit is cleared to 0, the TXDMAE bit is automatically cleared to 0 by hardware.
[7]	ADRM	Addressing Mode 0: 7-bit addressing mode 1: 10-bit addressing mode When the I^2C master/slave module operates in the 7-bit addressing mode, it can only send out and respond to a 7-bit address and vice versa. When the I2CEN bit is disabled, the ADRM bit is automatically cleared to 0 by hardware.
[3]	I2CEN	I^2C Interface Enable 0: I^2C interface disabled 1: I^2C interface enabled
[2]	GCEN	General Call Enable 0: General call disabled 1: General call enabled When the device receives the calling address with a value of 0x00 and if both the GCEN and the AA bits are set to 1, then the I^2C interface is addressed as a slave and the GCS bit in the I2CSR register is set to 1. When the I2CEN bit is cleared to 0, the GCEN bit is automatically cleared to 0 by hardware.
[1]	STOP	STOP Condition Control 0: No action 1: Send a STOP condition in master mode This bit is set to 1 by software to generate a STOP condition and automatically cleared to 0 by hardware. The STOP bit is only available for the master device.
[0]	AA	Acknowledge Bit 0: Send a Not Acknowledge (NACK) signal after a byte is received 1: Send an Acknowledge (ACK) signal after a byte is received When the I2CEN bit is cleared to 0, the AA bit is automatically cleared to 0 by hardware.

I²Cn Interrupt Enable Register – I2CnIER, n=0 or 1

This register specifies the corresponding I²Cn interrupt enable bits.

Offset: 0x004

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved					RXBFIE	TXDEIE	RXDNEIE
Type/Reset						RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
	Reserved				TOUTIE	BUSERRIE	RXNACKIE	ARBLOSIE
Type/Reset					RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	Reserved				GCSIE	ADRSIE	STOIE	STAIE
Type/Reset					RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[18]	RXBFIE	RX Buffer Full Interrupt Enable Bit 0: Interrupt disabled 1: Interrupt enabled When the I2CEN bit in the I2CCR register is cleared to 0, this bit is cleared to 0 by hardware.
[17]	TXDEIE	Data Register Empty Interrupt Enable Bit in Transmitter Mode 0: Interrupt disabled 1: Interrupt enabled When the I2CEN bit in the I2CCR register is cleared to 0, this bit is cleared to 0 by hardware.
[16]	RXDNEIE	Data Register Not Empty Interrupt Enable Bit in Receiver Mode 0: Interrupt disabled 1: Interrupt enabled When the I2CEN bit in the I2CCR register is cleared to 0, this bit is cleared to 0 by hardware.
[11]	TOUTIE	Timeout Interrupt Enable Bit 0: Interrupt disabled 1: Interrupt enabled When the I2CEN bit in the I2CCR register is cleared to 0, this bit is cleared to 0 by hardware.
[10]	BUSERRIE	Bus Error Interrupt Enable Bit 0: Interrupt disabled 1: Interrupt enabled When the I2CEN bit in the I2CCR register is cleared to 0, this bit is cleared to 0 by hardware.

Bits	Field	Descriptions
[9]	RXNACKIE	Received Not Acknowledge Interrupt Enable Bit 0: Interrupt disabled 1: Interrupt enabled When the I2CEN bit in the I2CCR register is cleared to 0, this bit is cleared to 0 by hardware.
[8]	ARBLOSIE	Arbitration Loss Interrupt Enable Bit in I^2C multi-master mode 0: Interrupt disabled 1: Interrupt enabled When the I2CEN bit in the I2CCR register is cleared to 0, this bit is cleared to 0 by hardware.
[3]	GCSIE	General Call Slave Interrupt Enable Bit 0: Interrupt disabled 1: Interrupt enabled When the I2CEN bit in the I2CCR register is cleared to 0, this bit is cleared to 0 by hardware.
[2]	ADRSIE	Slave Address Match Interrupt Enable Bit 1: Interrupt enabled 0: Interrupt disabled When the I2CEN bit in the I2CCR register is cleared to 0, this bit is cleared to 0 by hardware.
[1]	STOIE	STOP Condition Detected Interrupt Enable Bit 0: Interrupt disabled 1: Interrupt enabled When the I2CEN bit in the I2CCR register is cleared to 0, this bit is cleared to 0 by hardware. The bit is used for the I^2C slave mode only.
[0]	STAIE	START Condition Transmit Interrupt Enable Bit 0: Interrupt disabled 1: Interrupt enabled When the I2CEN bit in the I2CCR register is cleared to 0, this bit is cleared to 0 by hardware. The bit is used for the I^2C master mode only.

I²Cn Address Register – I2CnADDR, n=0 or 1

This register specifies the I²Cn device address.

Offset: 0x008

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved						ADDR	
Type/Reset							RW 0	RW 0
	7	6	5	4	3	2	1	0
	ADDR							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[9:0]	ADDR	Device Address The register indicates the I²C device address. When the I²C device is used in the 7-bit addressing mode, only the ADDR [6:0] bits will be compared with the received address sent from the I²C master device.

I²Cn Status Register – I2CnSR, n=0 or 1

This register contains the I²Cn operation status.

Offset: 0x00C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
		Reserved	TXNRX	MASTER	BUSBUSY	RXBF	TXDE	RXDNE
Type/Reset			RO 0	RO 0	RO 0	RO 0	RO 0	RO 0
	15	14	13	12	11	10	9	8
	Reserved				TOUTF	BUSERR	RXNACK	ARBLOS
Type/Reset					WC 0	WC 0	WC 0	WC 0
	7	6	5	4	3	2	1	0
	Reserved				GCS	ADRS	STO	STA
Type/Reset					RC 0	RC 0	RC 0	RC 0

Bits	Field	Descriptions
[21]	TXNRX	Transmitter/Receiver Mode 0: Receiver mode 1: Transmitter mode Read only bit.
[20]	MASTER	Master Mode 0: I²C is in the slave mode or idle 1: I²C is in the master mode The I²C interface is switched as a master device on the I²C bus when the I2CTAR register is assigned and the I²C bus is idle. The MASTER bit is cleared by hardware when software disables the I²C bus by clearing the I2CEN bit to 0 or sends a STOP condition to the I²C bus or the bus error is detected. This bit is set and cleared by hardware and is a read only bit.
[19]	BUSBUSY	Bus Busy 0: I²C bus idle 1: I²C bus busy The I²C interface hardware starts to detect the I²C bus status if the interface is enabled by setting the I2CEN bit to 1. It is set to 1 when the SDA or SCL signal is detected to have a logic low state and cleared when a STOP condition is detected.
[18]	RXBF	Buffer Full Flag in Receiver Mode 0: Data buffer not full 1: Data buffer full This bit is set when the data register I2CDR has already stored a data byte and meanwhile the data shift register also has been received a complete new data byte. The RXBF bit is cleared by software reading the I2CDR register.

Bits	Field	Descriptions
[17]	TXDE	Data Register Empty in Transmitter Mode 0: Data register I2CDR not empty 1: Data register I2CDR empty This bit is set when the I2CDR register is empty in the Transmitter mode. Note that the TXDE bit will be set after the address frame is being transmitted to inform that the data to be transmitted should be loaded into the I2CDR register. The TXDE bit is cleared by software writing data to the I2CDR register in both the master and slave mode or cleared automatically by hardware after setting the STOP signal to terminate the data transfer or setting the I2CTAR register to restart a new data transfer in the master mode.
[16]	RXDNE	Data Register Not Empty in Receiver Mode 0: Data register I2CDR empty 1: Data register I2CDR not empty This bit is set when the I2CDR register is not empty in the receiver mode. The RXDNE bit is cleared by software reading the data byte from the I2CDR register.
[11]	TOUTF	Timeout Counter Underflow Flag 0: No timeout counter underflow occurred 1: Timeout counter underflow occurred Writing 1 to this bit will clear the TOUTF flag.
[10]	BUSERR	Bus Error Flag 0: No bus error occurs 1: Bus error has occurred This bit is set by hardware when the I^2C interface detects a misplaced START or STOP condition in a transfer process. Writing 1 to this bit will clear the BUSERR flag. In Master Mode: Once the Bus Error event occurs, both the SDA and SCL lines are released by hardware and the BUSERR flag is asserted. The application software has to clear the BUSERR flag before the next address byte is transmitted. In Slave Mode: Once a misplaced START or STOP condition has been detected by the slave device, the software must clear the BUSERR flag before the next address byte is received.
[9]	RXNACK	Received Not Acknowledge Flag 0: Acknowledge is returned from receiver 1: Not Acknowledge is returned from receiver The RXNACK bit indicates that the not Acknowledge signal is received in master or slave transmitter mode. Writing 1 to this bit will clear the RXNACK flag.
[8]	ARBLOS	Arbitration Loss Flag 0: No arbitration loss is detected 1: Bit arbitration loss is detected This bit is set by hardware on the current clock which the I^2C interface loses the bus arbitration to another master during the address or data frame transmission. Writing 1 to this bit will clear the ARBLOS flag. Once the ARBLOS flag is asserted by hardware, the ARBLOS flag must be cleared before the next transmission.
[3]	GCS	General Call Slave Flag 0: No general call slave occurs 1: I^2C interface is addressed by a general call command When the I^2C interface receives an address with a value of 0x00 or 0x000 in the 7-bit or 10-bit addressing mode, if both the GCEN and the AA bit are set to 1, then it is switched as a general call slave. This flag is cleared automatically after being read.

Bits	Field	Descriptions
[2]	ADRS	Address Transmit (master mode)/Address Receive (slave mode) Flag – Address Sent in Master Mode 0: Address frame has not been transmitted 1: Address frame has been transmitted For the 7-bit addressing mode, this bit is set after the master device receives the address frame acknowledge bit sent from the slave device. For the 10-bit addressing mode, this bit is set after receiving the acknowledge bit of the first header byte and the second address. – Address Matched in Slave Mode 0: I^2C interface is not addressed 1: I^2C interface is addressed as slave When the I^2C interface has received the calling address that matches the address defined in the I2CADDR register together with the AA bit being set to 1 in the I2CCR register, it will be switched to a slave mode. This flag is cleared automatically after the I2CSR register has been read.
[1]	STO	STOP Condition Detected Flag 0: No STOP condition detected 1: STOP condition detected in slave mode This bit is only available for the slave mode and is cleared automatically after the I2CSR register is read.
[0]	STA	START Condition Transmit 0: No START condition detected 1: START condition is transmitted in master mode This bit is only available for the master mode and is cleared automatically after the I2CSR register is read.

I²Cn SCL High Period Generation Register – I2CnSHPGR, n=0 or 1

This register specifies the I²Cn SCL clock high period interval.

Offset: 0x010

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	SHPG							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	SHPG							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	SHPG	SCL Clock High Period Generation High period duration setting $SCL_{HIGH}=T_{PCLK} \times (SHPG + d)$ where d=7 and T_{PCLK} is the APB bus peripheral clock (PCLK) period.

I²Cn SCL Low Period Generation Register – I2CnSLPGR, n=0 or 1

This register specifies the I²Cn SCL clock low period interval.

Offset: 0x014

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	SLPG							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	SLPG							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	SLPG	SCL Clock Low Period Generation High period duration setting $SCL_{LOW}=T_{PCLK} \times (SLPG + d)$ where d=9 and T_{PCLK} is the APB bus peripheral clock (PCLK) period.

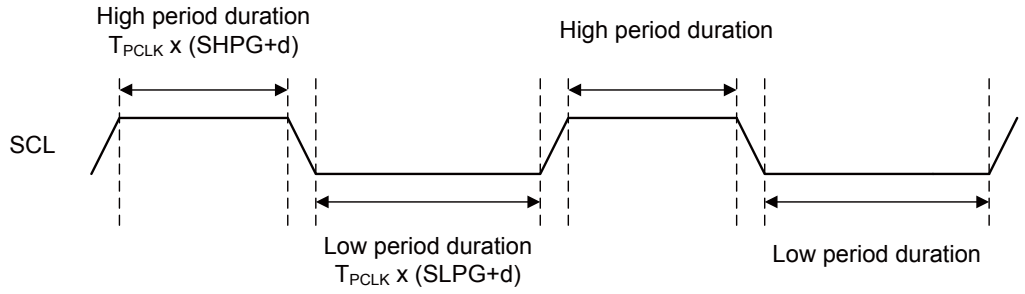


Figure 129. SCL Timing Diagram

Table 45. I²C Clock Setting Example

I²C Clock	$T_{SCL}=T_{PCLK} \times [(SHPG + d) + (SLPG + d)]$ (where d=9) SHPG + SLPG value at PCLK			
	8MHz	24MHz	48MHz	72MHz
100kHz (Standard Mode)	62	222	462	702
400kHz (Fast Mode)	2	42	102	162
1MHz (Fast Mode Plus)	x	6	30	54

I²Cn Data Register – I2CnDR, n=0 or 1

This register specifies the data to be transmitted or received by the I²Cn module.

Offset: 0x018

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	DATA							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[7:0]	DATA	I²Cn Data Register For the transmitter mode, a data byte which is transmitted to a slave device can be assigned to these bits. The TXDE flag is cleared if the application software assigns new data to the I2CDR register. For the receiver mode, a data byte is received bit by bit from MSB to LSB through the I²C interface and stored in the data shift register. Once the acknowledge bit is given, the data shift register value is delivered into the I2CDR register if the RXDNE flag is equal to 0.

I²Cn Target Address Register – I2CnTAR, n=0 or 1

This register specifies the target device address to be communicated.

Offset: 0x01C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved					RWD	TAR	
Type/Reset						RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	TAR							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[10]	RWD	Read or Write Direction 0: Write direction to target slave address 1: Read direction from target slave address If this bit is set to 1 in the 10-bit master receiver mode, the I²C interface will initiate a byte with a value of 11110XX0b in the first header frame and then continue to deliver a byte with a value of 11110XX1b in the second header frame by hardware automatically.
[9:0]	TAR	Target Slave Address The I²C interface will assign a START signal and send a target slave address automatically once the data is written to this register. When the system wants to send a repeated START signal to the I²C bus, the timing is suggested to set the I2CTAR register after a byte transfer is completed. It is not allowed to set TAR in the address frame. I2CTAR [9:7] is not available under the 7-bit addressing mode.

I²Cn Address Mask Register – I2CnADDMR, n=0 or 1

This register specifies which bit of the I²Cn address is masked and not compared with corresponding bit of the received address frame.

Offset: 0x020

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved						ADDMR	
Type/Reset							RW 0	RW 0
	7	6	5	4	3	2	1	0
	ADDMR							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[9:0]	ADDMR	Address Mask Control Bit The ADDMR [i] is used to specify whether the ith bit of the ADDR in the I2CnADDR register is masked and is compared with the received address frame or not on the I²Cn bus. The register is only used for the I²Cn slave mode only. 0: ith bit of the ADDR is compared with the address frame on the I²Cn bus 1: ith bit of the ADDR is masked and not compared with the address frame on the I²Cn bus

I²Cn Address Snoop Register – I2CnADDSR, n=0 or 1

This register is used to indicate the address frame value appeared on the I²Cn bus.

Offset: 0x024

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved						ADDSR	
Type/Reset							RO 0	RO 0
	7	6	5	4	3	2	1	0
	ADDSR							
Type/Reset	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0

Bits	Field	Descriptions
[9:0]	ADDSR	Address Snoop Once the I2CEN bit is enabled, the calling address value on the I²Cn bus will automatically be loaded into this ADDSR field.

I²Cn Timeout Register – I2CnTOUT, n=0 or 1

This register specifies the I²Cn Timeout counter preload value and clock prescaler ratio.

Offset: 0x028

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved					PSC		
Type/Reset						RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
	TOUT							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	TOUT							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[18:16]	PSC	I²C Time-out Counter Prescaler Selection This PSC field is used to specify the I²C time-out counter clock frequency, f_{I2CTO}. The time-out clock frequency is obtained using the formula. $f_{I2CTO} = \frac{f_{PCLK}}{2^{PSC}}$ PSC=0 → $f_{I2CTO}=f_{PCLK}/2^0=f_{PCLK}$ PSC=1 → $f_{I2CTO}=f_{PCLK}/2^1=f_{PCLK}/2$ PSC=2 → $f_{I2CTO}=f_{PCLK}/2^2=f_{PCLK}/4$ … PSC=7 → $f_{I2CTO}=f_{PCLK}/2^7=f_{PCLK}/128$
[15:0]	TOUT	I²C Timeout Counter Preload Value The TOUT field is used to define the counter preloaded value. The counter value is reloaded as the following conditions occur: 1. The RXBF, TXDE, RXDNE, RXNACK, GCS or ADRS flag in the I2CSR register is asserted. 2. The I²C master module sends a START signal. 3. The I²C slave module detects a START signal. The counter stops counting as the following conditions occur: 1. The I²C slave device is not addressed. 2. The I²C master module sends a STOP signal. 3. The I²C slave module detects a STOP signal. 4. The ARBLOS or BUSERR flag in the I2CSR register is asserted.

20 Serial Peripheral Interface (SPI0 & SPI1)

Introduction

The Serial Peripheral Interface, SPI, provides an SPI protocol data transmit and receive functions in both master and slave modes. The SPI interface uses 4 pins, among which are the serial data input and output lines MISO and MOSI, the clock line SCK, and the slave select line, SEL. One SPI device acts as a master which controls the data flow using the SEL and SCK signals to indicate the start of the data communication and the data sampling rate. To receive the data bits, the streamed data bits which ranges from 1 bit to 16 bits specified by the DFL field in the SPInCR1 register are latched on a specific clock edge and stored in the data register or in the RX FIFO. Data transmission is carried in a similar way but with the reverse sequence. The mode fault detection provides a capability for multi-master applications.

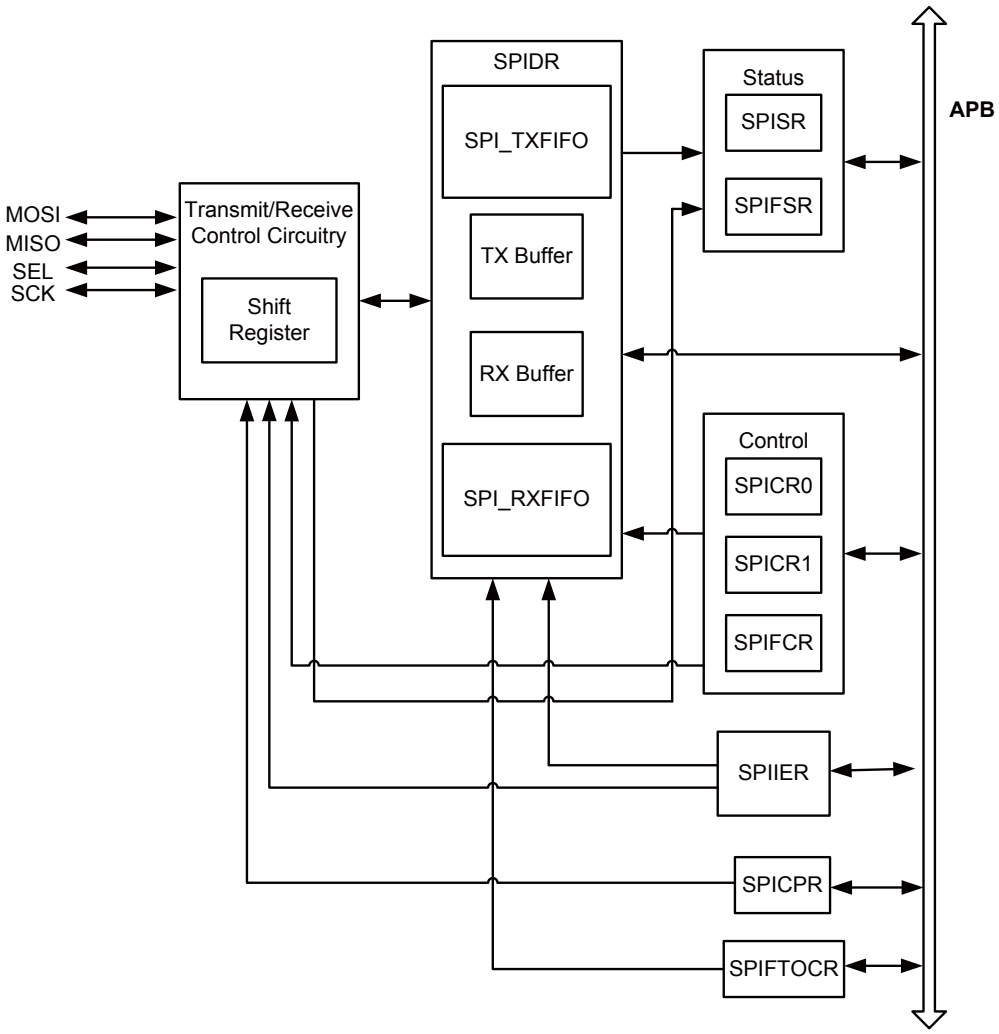


Figure 130. SPI Block Diagram

Features

- Master or slave mode
- Master mode speed up to 36MHz
- Slave mode speed up to 24MHz
- Programmable data frame length up to 16 bits
- FIFO Depth: 8 levels
- MSB or LSB first shift selection
- Programmable slave select high or low active polarity
- Multi-master and multi-slave operation
- Four error flags with individual interrupts
  - Read overrun
  - Write collision
  - Mode fault
  - Slave abort
- Supports PDMA Interface

Functional Descriptions

Master Mode

Each data frame can range from 1 to 16 bits in data length. The first bit of the transmitted data can be either an MSB or LSB determined by the FIRSTBIT bit in the SPICR1 register. The SPI module is configured as a master or a slave by setting the MODE bit in the SPICR1 register. When the MODE bit is set, the SPI module is configured as a master and will generate the serial clock on the SCK pin. The data stream will transmit data in the shift register to the MOSI pin on the serial clock edge. The SEL pin is active during the full data transmission. When the SELAP bit in the SPICR1 register is set, the SEL pin is active high during the complete data transactions. When the SELM bit in the SPICR1 register is set, the SEL pin will be driven by the hardware automatically and the time interval between the active SEL edge and the first edge of SCK is equal to one half an SCK period.

Slave Mode

In the slave mode, the SCK pin acts as an input pin and the serial clock will be derived from the external master device. The SEL pin also acts as an input. When the SELAP bit is cleared to 0, the SEL signal is active low during the full data stream reception. When the SELAP bit is set to 1, the SEL signal will be active high during the full data stream byte reception.

Note: For the slave mode, the APB clock, known as f_{PCLK}, must be at least 3 times faster than the external SCK clock input frequency.

SPI Serial Frame Format

The SPI interface format is base on the Clock Polarity, CPOL, and the Clock Phase, CPHA, configurations.

- Clock Polarity Bit – CPOL
  When the Clock Polarity bit is cleared to 0, the SCK line idle state is LOW. When the Clock Polarity bit is set to 1, the SCK line idle state is HIGH.

- Clock Phase – CPHA
  When the Clock Phase bit is cleared to 0, the data is sampled on the first SCK clock transition. When the Clock Phase bit is set to1, the data is sampled on the second SCK clock transition.

There are four formats contained in the SPI interface. Table 46 shows how to configure these formats by setting the FORMAT field in the SPICR1 register.

Table 46. SPI Interface Format Setup

FORMAT [2:0]	CPOL	CPHA
001	0	0
010	0	1
110	1	0
101	1	1
Others	Reserved	

CPOL=0, CPHA=0

In this format, the received data is sampled on the SCK line rising edge while the transmitted data is changed on the SCK line falling edge. In the master mode, the first bit is driven when data is written into the SPIDR Register. In the slave mode, the first bit is driven when the SEL signal goes to an active level. Figure 131 shows the single byte data transfer timing of this format

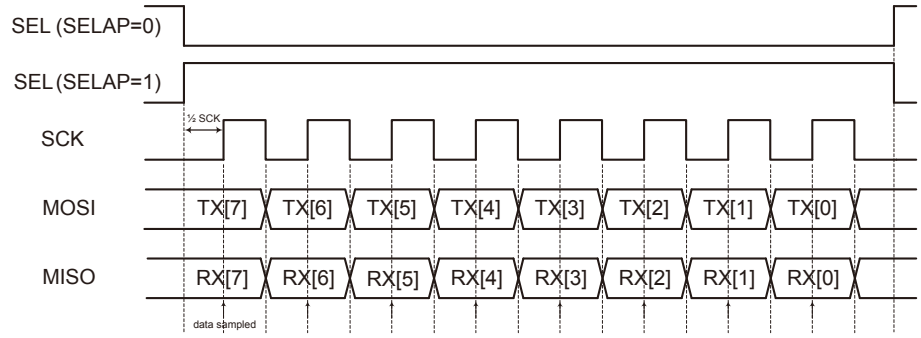


Figure 131. SPI Single Byte Transfer Timing Diagram – CPOL=0, CPHA=0

Figure 132 shows the continuous data transfer timing diagram of this format. Note that the SEL signal must change to an inactive level between each data frame.

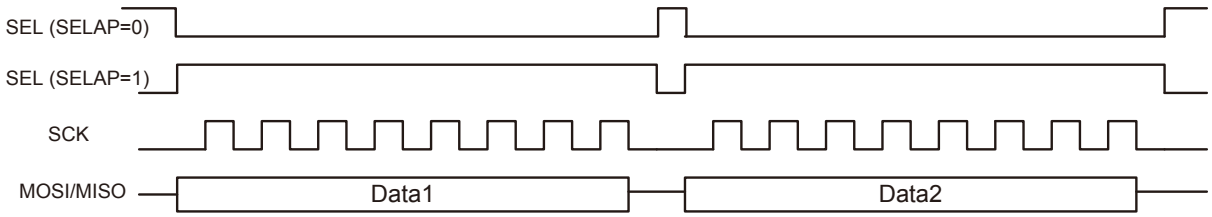


Figure 132. SPI Continuous Data Transfer Timing Diagram – CPOL=0, CPHA=0

CPOL=0, CPHA=1

In this format, the received data is sampled on the SCK line falling edge while the transmitted data is changed on the SCK line rising edge. In the master mode, the first bit is driven when data is written into the SPIDR register. In the slave mode, the first bit is driven at the first SCK clock rising edge. Figure 133 shows the single data byte transfer timing.

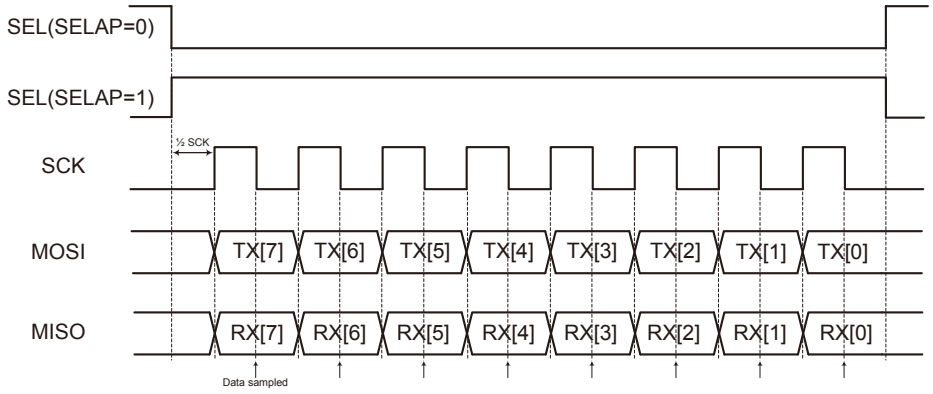


Figure 133. SPI Single Byte Transfer Timing Diagram – CPOL=0, CPHA=1

Figure 134 shows the continuous data transfer diagram timing. Note that the SEL signal must remain active until the last data transfer has completed.

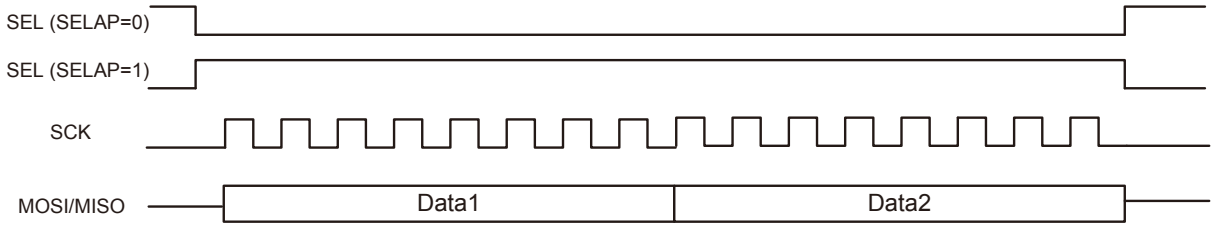


Figure 134. SPI Continuous Transfer Timing Diagram – CPOL=0, CPHA=1

CPOL=1, CPHA=0

In this format, the received data is sampled on the SCK line falling edge while the transmitted data is changed on the SCK line rising edge. In the master mode, the first bit is driven when data is written into the SPIDR register. In the slave mode, the first bit is driven when the SEL signal changes to an active level. Figure 135 shows the single byte transfer timing of this format.

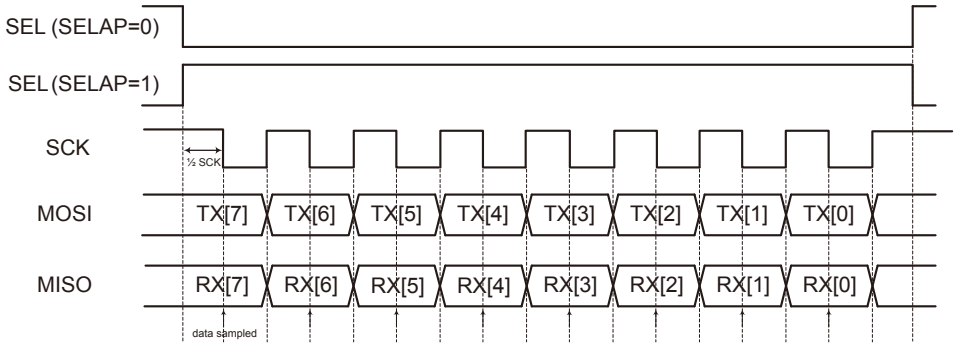


Figure 135. SPI Single Byte Transfer Timing Diagram – CPOL=1, CPHA=0

Figure 136 shows the continuous data transfer timing of this format. Note that the SEL signal must change to an inactive level between each data frame.

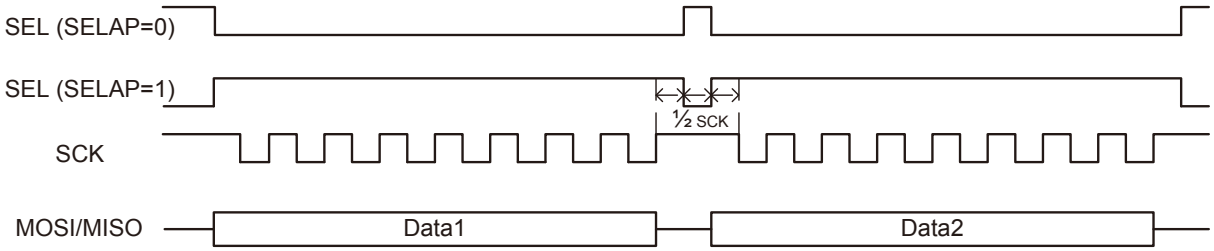


Figure 136. SPI Continuous Data Transfer Timing Diagram – CPOL=1, CPHA=0

CPOL=1, CPHA=1

In this format, the received data is sampled on the SCK line rising edge while the transmitted data is changed on the SCK line falling edge. In the master mode, the first bit is driven when data is written into the SPIDR register. In the slave mode, the first bit is driven at the first SCK falling edge. Figure 137 shows the single byte transfer timing of this format.

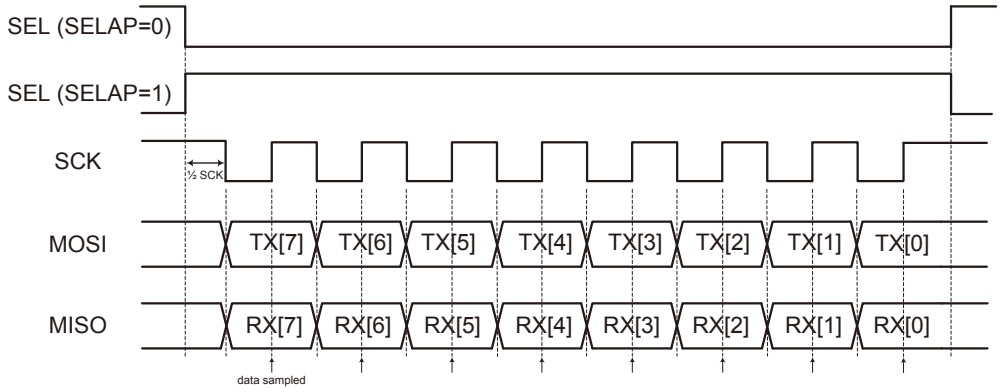


Figure 137. SPI Single Transfer Timing Diagram – CPOL=1, CPHA=1

Figure 138 shows the continuous data transfer timing of this format. Note that the SEL signal must remain active until the last data transfer has completed.

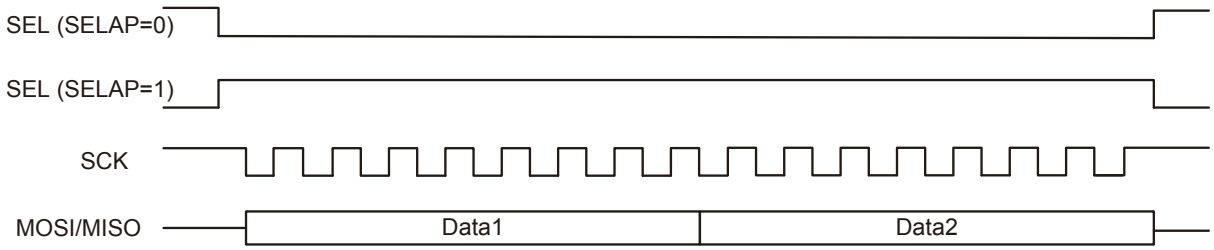


Figure 138. SPI Continuous Transfer Timing Diagram – CPOL=1, CPHA=1

Status Flags

TX Buffer Empty – TXBE

This TXBE flag is set when the Tx buffer is empty in the non-FIFO mode or when the TX FIFO data length is equal to or less than the TX FIFO threshold level as defined by the TXFTLS field in the SPIFCR register in the FIFO mode. The following data to be transmitted can then be loaded into the buffer again. After this, the TXBE flag will be reset when the Tx buffer already contains new data in the non-FIFO mode or the TX FIFO data length is greater than the TX FIFO threshold level determined by the TXFTLS bits in FIFO mode.

Transmission Register Empty – TXE

This TXE flag is set when both the TX buffer and the TX shift registers are empty. It will be reset when the TX buffer or the TX shift register contains new transmitted data.

RX Buffer Not Empty – RXBNE

This RXBNE flag is set when there is valid received data in the RX Buffer in the non-FIFO mode or the RX FIFO data length is equal to or greater than the RX FIFO threshold level as defined by the RXFTLS field in the SPIFCR register in the SPI FIFO mode. This flag will be automatically cleared by hardware when the received data have been read out from the RX buffer totally in the non-FIFO mode or when the RX FIFO data length is less than the RX FIFO threshold level set in the RXFTLS field

Time Out Flag – TO

The time out function is only available in the SPI FIFO mode and is disabled by loading a zero value into the TOC field in the Time Out Counter register. The time out counter will start counting if the SPI RX FIFO is not empty, once data is read from the SPIDR register or new data is received, the time out counter will be reset to 0 and count again. When the time out counter value is equal to the value specified by the TOC field in the SPIFTOCR register, the TO flag will be set. The flag is cleared by writing 1 to this bit.

Mode Fault – MF

The mode fault flag can be used to detect SPI bus usage in the SPI multi-master mode. For the multi-master mode, the SPI module is configured as a master device and the SEL signal is setup as an input signal. The mode fault flag is set when the SPI SEL pin is suddenly changed to an active level by another SPI master. This means that another SPI master is requesting to use the SPI bus. Therefore, when an SPI mode fault occurs, it will force the SPI module to operate in the slave mode and also disable all of the SPI interface signals to avoid SPI bus signal collisions. For the same reason, if the SPI master wants to transfer data, it also needs to inform other SPI masters by driving its SEL signal to an active state. The detailed configuration diagram for the SPI multi-master mode is shown in the following figure.

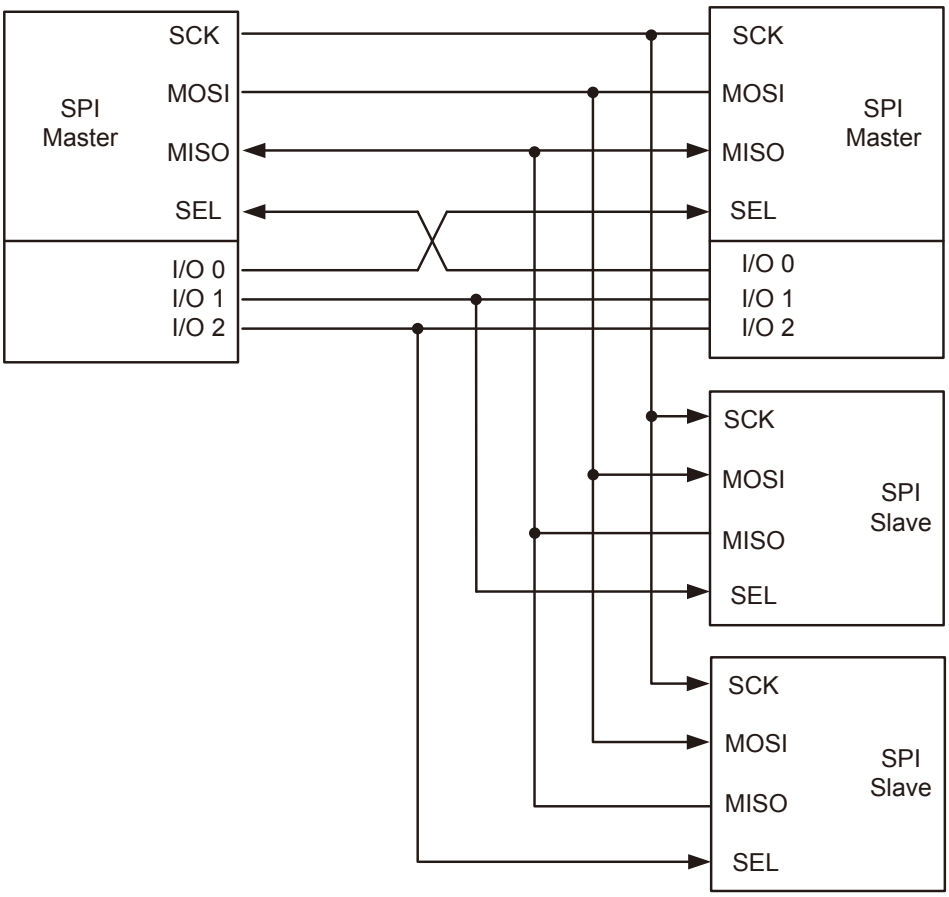


Figure 139. SPI Multi-Master Slave Environment

Table 47. SPI Mode Fault Trigger conditions

Mode fault	Descriptions
Trigger condition	1. SPI Master mode. 2. SELOEN=0 in the SPICR0 register - SEL pin is configured to be the input mode 3. SEL signal changes to an active level when driven by the external SPI master.
SPI behavior	1. Mode fault flag is set. 2. The SPIEN bit in the SPICR0 register is reset. This disables the SPI interface and blocks all output signals from the device. 3. The MODE bit in the SPICR1 register is reset. This forces the device into the slave mode.

Table 48. SPI Master Mode SEL Pin Status

	SEL as Input – SELOEN=0		SEL as Output – SELOEN=1	
Multi-master	Support		Not support	
SPI SEL control signal	Use another GPIO to replace the SEL pin function		SEL pin in hardware or software mode – using SELM setting	
Continuous transfer	**Case 1**	**Case 2**	**Case 1**	**Case 2**
	Not supported	Supported	Using hardware control	Hardware or software control

Case 1: SEL signal must be inactive between each data transfer.

Case 2: SEL signal will not be inactive until the last data frame has finished.

Note: When the SPI module is in the slave mode, the SEL signal is always an input and not affected by the SELOEN bit in the SPICR0 register.

Write Collision Flag – WC

The following conditions will assert the Write Collision Flag:

- The FIFOEN bit in the SPIFCR register is cleared.
  The write collision flag is asserted when new data is written into the SPIDR register while both the TX buffer and the shift register are already full. Any new data written into the TX buffer will be lost.
- The FIFOEN bit in the SPIFCR register is set.
  The write collision flag is asserted to indicate that new data is written into the SPIDR register while both the TX FIFO and the TX shift register are already full. Any new data written into the TX FIFO will be lost.

Read Overrun Flag – RO

- The FIFOEN bit in the SPIFCR register is cleared.
  The read overrun flag is asserted to indicate that both the RX shift register and the RX buffer are already full, if one more data is received. This will result in the newly received data not being shifted into the SPI shift register. As a result the latest received data will be lost.
- The FIFOEN bit in the SPIFCR register is set.
  The read overrun flag is set to indicate that the RX shift register and the RX FIFO are both full, if one more data is received. This means that the latest received data can not be shifted into the SPI shift register. As a result the latest received data will be lost.

Slave Abort Flag – SA

In the SPI slave mode, the slave abort flag is set to indicate that the SEL pin has suddenly changed to an inactive state during the reception of a data frame transfer. The data frame length is set by the DFL field in the SPICR1 register.

PDMA Interface

The PDMA interface is integrated in the SPI module. The PDMA function can be enabled by setting the TXDMAE or RXDMAE bit to 1 in the transmitter or receiver mode respectively. When the transmit buffer empty flag, TXBE, is asserted and the TXDMAE bit is set to 1, the PMDA function will be activated to move data from the memory location that users designated into the SPI data register or the TX FIFO until the TXBE flag is cleared to 0. The TXBE flag will be asserted when the transmit buffer is empty in the non-FIFO mode or the data contained in the TX FIFO is equal to or less than the level defined by the TXFTLS field in the FIFO mode.

Similarly, when the receive buffer not empty flag, RXBNE, is asserted and the RXDMAE bit is set to 1, the PDMA function will be activated to move data from the SPI data register or the RX FIFO to the memory location that users designated until the RXBNE flag is cleared to 0. The RXBNE flag will be asserted when the receive buffer is not empty in the non-FIFO mode or the data contained in the RX FIFO is equal to or greater than the level defined by the RXFTLS field in the FIFO mode.

For a mode detailed description on the PDMA configurations, refer to the PDMA chapter.

Register Map

The following table shows the SPI registers and their reset values.

Table 49. SPI Register Map

Register	Offset	Description	Reset Value
SPI0 Base Address=0x4000_4000 SPI1 Base Address=0x4004_4000			
SPInCR0	0x000	SPIn Control Register 0	0x0000_0000
SPInCR1	0x004	SPIn Control Register 1	0x0000_0000
SPInIER	0x008	SPIn Interrupt Enable Register	0x0000_0000
SPInCPR	0x00C	SPIn Clock Prescaler Register	0x0000_0000
SPInDR	0x010	SPIn Data Register	0x0000_0000
SPInSR	0x014	SPIn Status Register	0x0000_0003
SPInFCR	0x018	SPIn FIFO Control Register	0x0000_0000
SPInFSR	0x01C	SPIn FIFO Status Register	0x0000_0000
SPInFTOCR	0x020	SPIn FIFO Time Out Counter Register	0x0000_0000

Register Descriptions

SPIn Control Register 0 – SPInCR0, n=0 or 1

This register specifies the SEL control and the SPIn enable bits.

Offset: 0x000

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved			SSELC	SELOEN	RXDMAE	TXDMAE	SPIEN
Type/Reset				RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[4]	SSELC	Software Slave Select Control 0: Set the SEL output to an inactive state 1: Set the SEL output to an active state The application Software can setup the SEL output to an active or inactive state by configuring the SSELC bit. The active level is configured by the SELAP bit in the SPICR1 register. Note that the SSELC bit is only available when the SELOEN bit is set to 1 for enabling the SEL output meanwhile the SELM bit is cleared to 0 for controlling the SEL signal by software. Otherwise, the SSELC bit has no effect.
[3]	SELOEN	Slave Select Output Enable 0: Set the SEL signal to the input mode for Multi-master mode 1: Set the SEL signal to the output mode for slave select The SELOEN is only available in the master mode to setup the SEL signal as an input or output signal. When the SEL signal is configured to operate in the output mode, it is used as a slave select signal in either the hardware or software mode according to the SELM bit setting in the SPICR1 register. The SEL signal is used for mode fault detection in the multi-master environment when it is configured to operate in the input mode.
[2]	RXDMAE	RX PDMA request enable 0: SPI RX path PDMA request disabled 1: SPI RX path PDMA request enabled
[1]	TXDMAE	TX PDMA request enable 0: SPI TX path PDMA request disabled 1: SPI TX path PDMA request enabled
[0]	SPIEN	SPI Enable 0: SPI interface disabled 1: SPI interface enabled

SPIn Control Register 1 – SPInCR1, n=0 or 1

This register specifies the SPIn parameters including the data length, the transfer format, the SEL active polarity/mode, the LSB/MSB control and the master/slave mode.

Offset: 0x004

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved	MODE	SELM	FIRSTBIT	SELAP	FORMAT		
Type/Reset		RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	Reserved				DFL			
Type/Reset					RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[14]	MODE	Master or Slave Mode 0: Slave mode 1: Master mode
[13]	SELM	Slave Select Mode 0: SEL signal is controlled by software - asserted or de-asserted by the SSELC bit 1: SEL signal is controlled by hardware - generated automatically by the SPI hardware Note that the SELM bit is available for the master mode only – MODE=1
[12]	FIRSTBIT	LSB or MSB Transmitted First 0: MSB transmitted first 1: LSB transmitted first
[11]	SELAP	Slave Select Active Polarity 0: SEL signal is active low 1: SEL signal is active high

Bits	Field	Descriptions
[10:8]	FORMAT	SPI Data Transfer Format These three bits are used to determine the data transfer format of the SPI interface.

FORMAT [2:0]	CPOL	CPHA
001	0	0
010	0	1
110	1	0
101	1	1
Others	Reserved	

CPOL: Clock Polarity
0: SCK Idle state is low
1: SCK Idle state is high
CPHA: Clock Phase
0: Data is captured on the first SCK clock edge
1: Data is captured on the second SCK clock edge

Bits	Field	Descriptions
[3:0]	DFL	Data Frame Length Selects the data transfer frame length from 1 bit to 16 bits. 0x1: 1 bit 0x2: 2 bits : : 0xF: 15 bits 0x0: 16 bits

SPIn Interrupt Enable Register – SPInIER, n=0 or 1

This register contains the corresponding SPIn interrupt enable control bits.

Offset: 0x008

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	TOIEN	SAIEN	MFIEN	ROIEN	WCIEN	RXBNEIEN	TXEIEN	TXBEIEN
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[7]	TOIEN	Time Out Interrupt Enable 0: Disable 1: Enable
[6]	SAIEN	Slave Abort Interrupt Enable 0: Disable 1: Enable
[5]	MFIEN	Mode Fault Interrupt Enable 0: Disable 1: Enable
[4]	ROIEN	Read Overrun Interrupt Enable 0: Disable 1: Enable
[3]	WCIEN	Write Collision Interrupt Enable 0: Disable 1: Enable
[2]	RXBNEIEN	RX Buffer Not Empty Interrupt Enable 0: Disable 1: Enable Generates an interrupt request when the RXBNE flag is set and when RXBNEIEN is set. In the FIFO mode, the interrupt request being generated depends upon the RX FIFO trigger level setting.
[1]	TXEIEN	TX Register Empty Interrupt Enable 0: Disable 1: Enable The TX register empty interrupt request will be generated when the TXE flag and the TXEIEN bit are set.
[0]	TXBEIEN	TX Buffer Empty Interrupt Enable 0: Disable 1: Enable The TX buffer empty interrupt request will be generated when the TXBE flag and the TXBEIEN bit are set. In the FIFO mode, the interrupt request being generated depends upon the TX FIFO trigger level setting.

SPIn Clock Prescaler Register – SPInCPR, n=0 or 1

This register specifies the SPIn clock prescaler ratio.

Offset: 0x00C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	Reserved							
Type/Reset								
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	CP							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	CP							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	CP	SPI Clock Prescaler The SPI clock (SCK) is determined by the following equation: $f_{SCK}=f_{PCLK}/(2 \times (CP + 1))$, where the CP range is from 0 to 65535 **Note:** For the SPI slave mode, the system clock (f_{PCLK}) must be at least 3 times faster than the external SPI SCK input.

SPIn Data Register – SPInDR, n=0 or 1

This register stores the SPIn received or transmitted Data.

Offset: 0x010

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	Reserved							
Type/Reset								
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	DR							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	DR							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	DR	Data Register The SPI data register is used to store the serial bus transmitted or received data. In the non-FIFO mode, writing data into the SPI data register will also load the data into the data transmission buffer, known as the TX buffer. Reading data from the SPI data register will return the data held in the data received buffer, named RX buffer.

SPIn Status Register – SPInSR, n=0 or 1

This register contains the relevant SPIn status.

Offset: 0x014

Reset value: 0x0000_0003

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							BUSY
Type/Reset								RO 0
	7	6	5	4	3	2	1	0
	TO	SA	MF	RO	WC	RXBNE	TXE	TXBE
Type/Reset	WC 0	WC 0	WC 0	WC 0	WC 0	RO 0	RO 1	RO 1

Bits	Field	Descriptions
[8]	BUSY	SPI Busy flag 0: SPI not busy 1: SPI busy In the master mode, this flag is reset when the TX buffer and TX shift register are both empty and is set when the TX buffer or the TX shift register are not empty. In the slave mode, this flag is set when SEL changes to an active level and is reset when SEL changes to an inactive level.
[7]	TO	Time Out flag 0: No RX FIFO time out 1: Rx FIFO time out has occurred Once the time out counter value is equal to the TOC field setting in the SPIFTOCR register, the time out flag will be set and an interrupt will be generated if the TOIEN bit in the SPIIER register is enabled. This bit is cleared by writing 1. **NOTE:** The Time Out flag function is only available in the SPI FIFO mode.
[6]	SA	Slave Abort flag 0: No slave abort 1: Slave abort has occurred This bit is set by hardware and cleared by writing 1.
[5]	MF	Mode Fault flag 0: No mode fault 1: Mode fault has occurred This bit is set by hardware and cleared by writing 1.
[4]	RO	Read Overrun flag 0: No read overrun 1: Read overrun has occurred This bit is set by hardware and cleared by writing 1.

Bits	Field	Descriptions
[3]	WC	Write Collision flag 0: No write collision 1: Write collision has occurred This bit is set by hardware and cleared by writing 1.
[2]	RXBNE	Receive Buffer Not Empty flag 0: RX buffer empty 1: RX buffer not empty This bit indicates the RX buffer status in the non-FIFO mode. It is also used to indicate if the RX FIFO trigger level has been reached in the FIFO mode. This bit will be cleared when the SPI RX buffer is empty in the non-FIFO mode or if the number of data contained in RX FIFO is less than the trigger level which is specified by the RXFTLS field in the SPIFCR register in the SPI FIFO mode.
[1]	TXE	Transmission Register Empty flag 0: TX buffer or TX shift register is not empty 1: TX buffer and TX shift register both are empty
[0]	TXBE	Transmit Buffer Empty flag 0: TX buffer not empty 1: TX buffer empty In the FIFO mode, this bit indicates that the number of data contained in TX FIFO is equal to or less than the trigger level specified by the TXFTLS field in the SPIFCR register.

SPIn FIFO Control Register – SPInFCR, n=0 or 1

This register contains the related SPIn FIFO control including the FIFO enable control and the FIFO trigger level selections.

Offset: 0x018

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved					FIFOEN	Reserved	Reserved
Type/Reset						RW 0		
	7	6	5	4	3	2	1	0
	RXFTLS				TXFTLS			
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[10]	FIFOEN	FIFO Enable 0: FIFO disable 1: FIFO enable This bit cannot be set or reset when the SPI interface is transmitting.
[7:4]	RXFTLS	RX FIFO Trigger Level Select 0000: Trigger level is 0 0001: Trigger level is 1 ... 1000: Trigger level is 8 Others: Reserved The RXFTLS field is used to specify the RX FIFO trigger level. When the number of data contained in the RX FIFO is equal to or greater than the trigger level defined by the RXFTLS field, the RXBNE flag will be set.
[3:0]	TXFTLS	TX FIFO Trigger Level Select 0000: Trigger level is 0 0001: Trigger level is 1 ... 1000: Trigger level is 8 Others: Reserved The TXFTLS field is used to specify the TX FIFO trigger level. When the number of data contained in the TX FIFO is equal to or less than the trigger level defined by the TXFTLS field, the TXBE flag will be set.

SPIn FIFO Status Register – SPInFSR, n=0 or 1

This register contains the relevant SPIn FIFO status.

Offset: 0x01C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	RXFS				TXFS			
Type/Reset	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0

Bits	Field	Descriptions
[7:4]	RXFS	RX FIFO Status 0000: RX FIFO empty 0001: RX FIFO contains 1 data ... 1000: RX FIFO contains 8 data Others: Reserved
[3:0]	TXFS	TX FIFO Status 0000: TX FIFO empty 0001: TX FIFO contains 1 data … 1000: TX FIFO contains 8 data Others: Reserved

SPIn FIFO Time Out Counter Register – SPInFTOCR, n=0 or 1

The register stores the SPIn RX FIFO time out counter value.

Offset: 0x020

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	TOC							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	TOC							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	TOC							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	TOC							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[31:0]	TOC	Time Out Counter The time out counter starts to count from 0 after the SPI RX FIFO receives a data, and reset the counter value once the data is read from the SPIDR register by software or another new data is received. If the FIFO does not receive new data or the software does not read data from the SPIDR register, the time out counter value will continuously increase. When the time out counter value is equal to the TOC setting value, the TO flag in the SPISR register will be set and an interrupt will be generated if the TOIEN bit in the SPIIEN register is set. The time out counter will be stopped when the RX FIFO is empty. The SPI FIFO time out function can be disabled by setting the TOC field to zero. The time out counter is driven by the system APB clock, named f_{PCLK}.

21 Universal Synchronous Asynchronous Receiver Transmitter (USART0 & USART1)

Introduction

The Universal Synchronous Asynchronous Receiver Transmitter, USART, provides a flexible full duplex data exchange using synchronous or asynchronous transfer. The USART is used to translate data between parallel and serial interfaces, and is also commonly used for RS232 standard communication. The USART peripheral function supports a variety of interrupts.

The USART module includes a 16-byte transmitter FIFO, TX_FIFO, and a 16-byte receiver FIFO, RX_FIFO.

Software can detect a USART error status by reading Line Status Register, LSR. The status includes the type and the condition of the transfer operations as well as several error conditions resulting from Parity, Overrun, Framing and Break events.

The USART includes a programmable baud rate generator which is capable of dividing the CK_AHB to produce a clock for the USART transmitter and receiver.

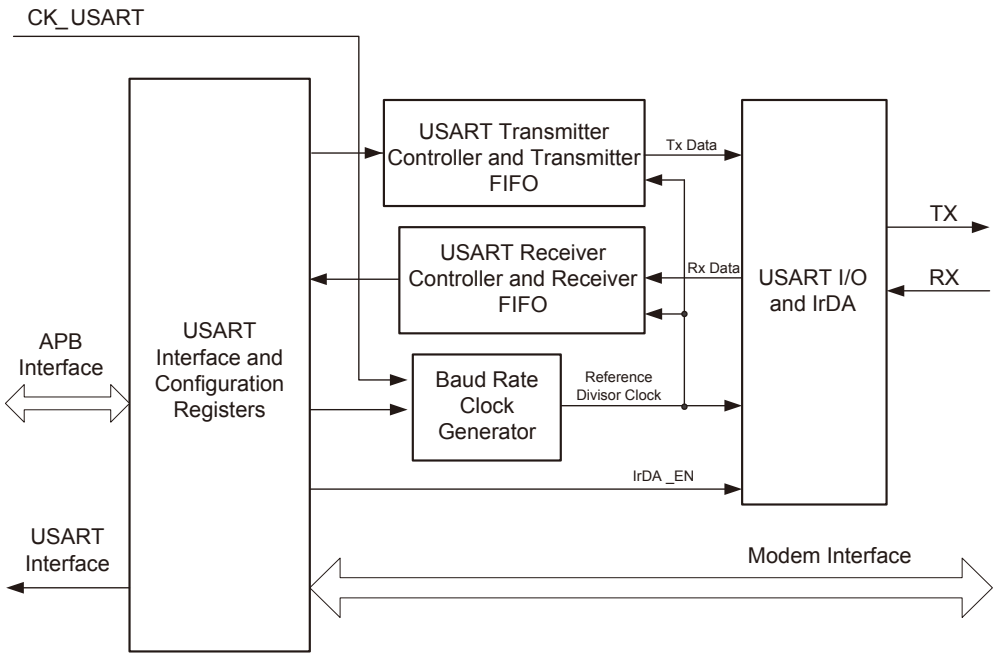


Figure 140. USART Block Diagram

Features

- Supports both asynchronous and clocked synchronous serial communication modes
- Full Duplex Communication Capability
- IrDA SIR encoder and decoder
  - Support normal 3/16 bit duration and low-power (1.41~2.23μs) duration
- Supports RS485 mode with output enable
- Auto hardware flow control mode – RTS, CTS
- Full modem function
- Fully programmable serial communication functions including:
  - Word length: 7, 8, or 9-bit character
  - Parity: Even, odd, or no-parity bit generation and detection
  - Stop bit: 1 or 2 stop bit generation
  - Bit order: LSB-first or MSB-first transfer
- Error detection: Parity, overrun, and frame error
- FIFO:
  - Receiver FIFO: 16×9 bits (max. 9 data bits)
  - Transmitter FIFO: 16×9 bits (max. 9 data bits)
- Supports PDMA Interface

Functional Descriptions

Serial Data Format

The USART module performs a parallel-to-serial conversion on data that is read from the Transmitter FIFO and then sends the data with the following format: start bit, 7~9 LSB first data bits, optional parity bit and finally 1~2 stop bits. The start bit has the opposite polarity of the data line idle state. The stop bit is the same as the data line idle state and provides a delay before the next start situation. The start and stop bits are both used for data synchronization during the asynchronous data transmission.

The USART module also performs a serial-to-parallel conversion on the data that is read from the Receiver FIFO. It will first check the Parity bit and will then look for a Stop bit. If the Stop bit is not found, the USART module will consider the entire word transmission to have failed and respond with a Framing Error.

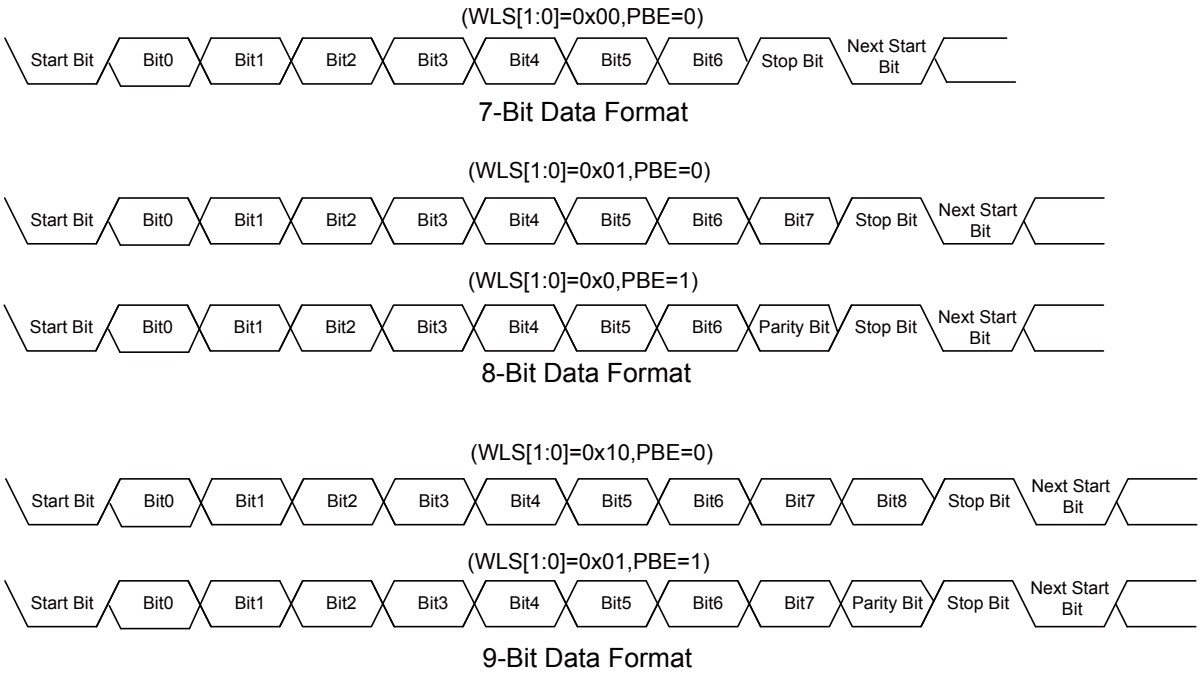


Figure 141. USART Serial Data Format

Baud Rate Generation

The baud rate for the USART receiver and transmitter are both set with the same values. The baud-rate divisor, BRD, has the following relationship with the USART clock which is known as CK_USART.

```
Baud Rate Clock=CK_USART/BRD
```

Where CK_USART clock is the system clock connected to the USART module while the BRD range is from 16 to 65535.

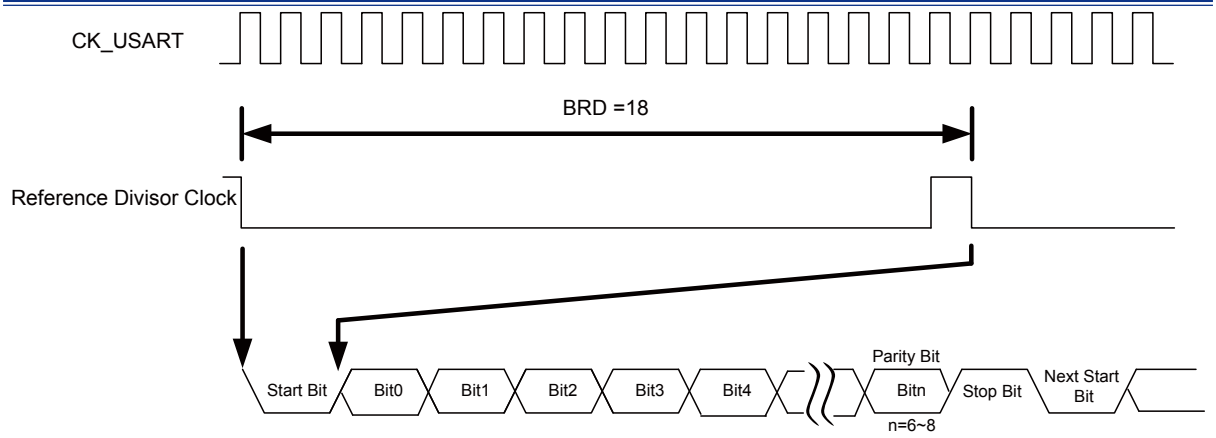


Figure 142. USART Clock CK_USART and Data Frame Timing

Table 50. Baud Rate Error calculation – CK_USART=72MHz

Baud rate		CK_USART=72MHz			
No	Kbps	Actual	BRD/16	BRD	Error rate
1	2.4	2.4	1875	30000	0%
2	9.6	9.6	468.75	7500	0%
3	19.2	19.2	234.375	3750	0%
4	57.6	57.6	78.125	1250	0%
5	115.2	115.2	39.0625	625	0%
6	230.4	230.769	19.5	312	0.16%
7	460.8	461.538	9.75	156	0.16%
8	921.6	923.076	4.875	78	0.16%
9	2250	2250	2	32	0%
10	4500	4500	1	16	0%

IrDA Mode

The USART IrDA mode is provided half-duplex point-to-point wireless communication.

The USART module include an integrated modulator and demodulator which allow a wireless communication using infrared transceivers. The transmitter specifies a data "0" as a "low" pulse and a data "1" as a "low" level while the Receiver specifies a data "0" as a "low" pulse and a data "1" as "high" level in the IrDA mode. The IrDA mode provides two operation modes, one is the normal mode, and the other is the low-power mode.

For the IrDA normal mode, the width of each transmitted pulse generated by the transmitter modulator is specified as 3/16 of the baud rate clock period. The receiver pulse width for the IrDA receiver demodulator is based on the IrDA receive debounce filter which is implement using an 8-bit down-counting counter. The debounce filter counter value is specified by the IrDAPSC field in the IrDACR register. When a falling edge is detected on the UR_RX pin, the debounce filter counter starts to count down, driven by the CK_USART clock. If a rising edge is detected on the UR_RX pin, the counter stops counting and is reloaded with the IrDAPSC value. When a low pulse falling edge on the UR_RX pin is detected and then before the debounce filter has counted down to zero, a rising edge is also detected, then this low pulse will be considered as glitch noise and will be discarded. If a low pulse falling edge appears on the UR_RX pin but no rising edge is detected before the debounce counter reaches 0, then the input on the USART receiver pin is regarded as a valid data "0" for this bit duration. The IrDAPSC value must be set to be greater than or equal to 0x01, then the IrDA receiver demodulation operation can function properly. The IrDAPSC value can be adjusted to meet the USART baud rate setting to filter the IrDA received glitch noise of which the width is smaller than the prescaler setting duration.

In the IrDA low-power mode, the transmitted IrDA pulse width generated by the transmitter modulator is not kept at 3/16 of the baud rate clock period. Instead, the pulse width is fixed and is calculated by the following formula. The transmitted pulse width can be adjusted by the IrDAPSC field to meet the minimum pulse width specification of the external IrDA Receiver device.

$$T_{IrDA\_L}=3\times IrDAPSC/CK\_USART$$

Note: T_{IrDA_L} is transmitted pulse width in the low power mode.
The IrDAPSC filed in the IrDACR prescaler value in the IrDA Control Register IrDACR.

The debounce behavior in the IrDA low-power receiving mode is similar to the IrDA normal mode. For glitch detection, the low pulse of which the pulse width is shorter than 1×(IrDAPSC/CK_USART) should be discarded in the IrDA receiver demodulation. A valid low data is accepted if its low pulse width is greater than 2×(IrDAPSC/CK_USART) duration.

The IrDA physical layer specification specifies a minimum delay with a value of 10ms between the transmission and reception and this IrDA receiver set-up time should be managed by the software.

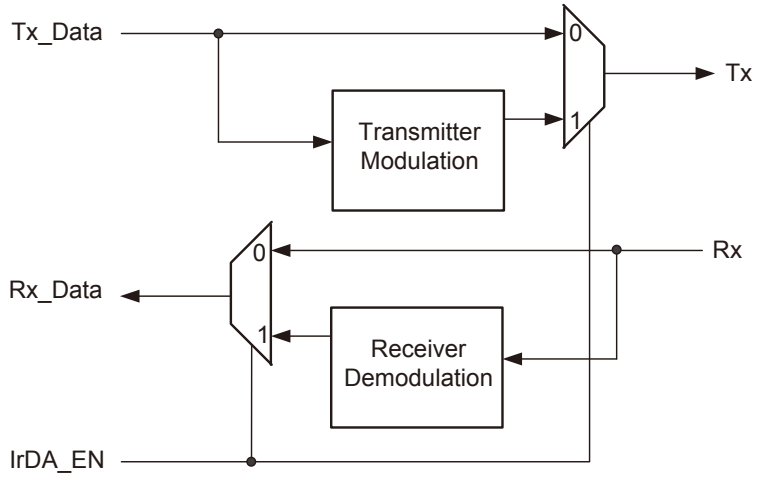


Figure 143. USART I/O and IrDA Block Diagram

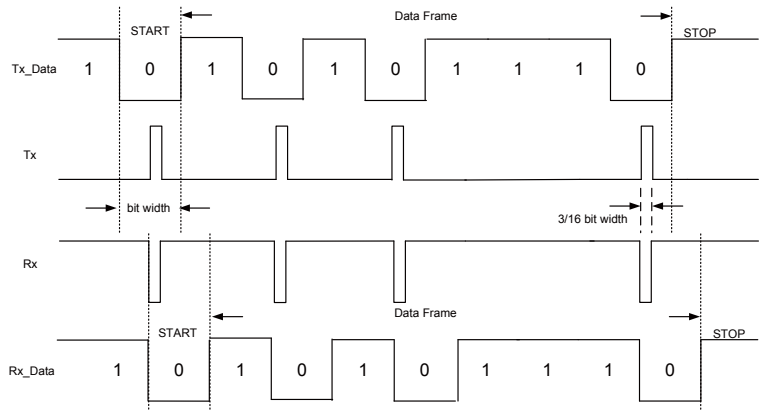


Figure 144. IrDA Modulation and Demodulation

RS485 Mode

The data on RS485 interface is transmitted over a 2-wire twisted pair bus. The RS485 transceiver interprets the voltage levels of the differential signals with respect to a third common voltage. Without this common reference, the transceiver may interpret the differential signals incorrectly. This enhances the noise rejection capabilities of the RS485 interface. The UR_RTS pin is used to control the external RS485 transceiver whose polarity can be selected by configuring the TXENP bit in the RS485 Control Register, named RS485CR, when the USART module operates in the RS485 mode.

RS485 Auto Direction Mode – AUD

When the RS485 interface is configured as a master transmitter, it will operate in the Auto Direction Mode, AUD. In the AUD mode the polarity of the UR_RTS pin is configurable according to the TXENP bit in the RS485 Control Register in the RS485 mode. This pin can be used to control the external RS485 transceiver to enable the transmitter.

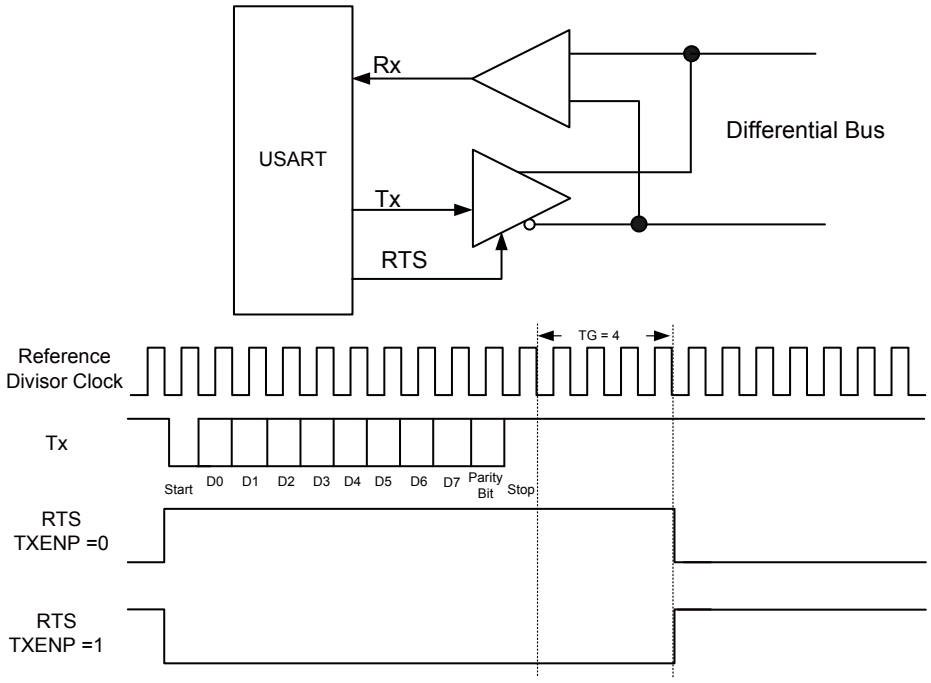


Figure 145. RS485 Interface and Waveform

RS485 Normal Multi-drop Operation Mode – NMM

When the RS485 interface is configured as an addressable slave, it will operate in the Normal Multi-drop Operation Mode, NMM. This mode is enabled when the RSNMM field is set in the RS485CR register. Regardless of the URRXEN value in the FCR register, all the received data with a parity bit "0" will be ignored until the first address byte is detected with a parity bit "1" and then the received address byte will be stored in the RXFIFO. Once the first address data is detected and stored in the RXFIFO, the RSADDEF flag in the LSR register will be set and generate an interrupt if the RLSIE bit in the IER register is set to 1. Application software can determine whether the receiver is enabled or disabled to accept the following data by configuring the URRXEN bit. When the receiver is enabled by setting the URRXEN bit to 1, all received data will be stored in the RXFIFO. Otherwise, all received data will be ignored if the receiver is disabled by clearing the URRXEN bit to 0.

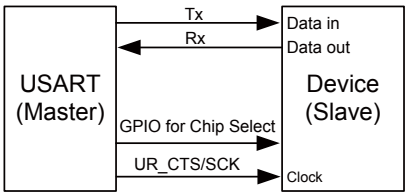
RS485 Auto Address Detection Operation Mode – AAD

Except in the Normal Multi-drop Operation Mode, the RS485 interface can operate in the Auto Address Detection Operation Mode, AAD, when it is configured as an addressable slave. This mode is enabled by setting the RSAAD filed to 1 in the RS485CR register. The receiver will detect the address frame with a parity bit "1" and then compare the received address data with the ADDMATCH field value which is a programmable 8-bit address value specified in the RS485CR register. If the address data matches the ADDMATCH value, it will be stored in the RXFIFO and the URRXEN bit will be automatically set. When the receiver is enabled, all received data will be stored in the RXFIFO until the next address frame does not match the ADDMATCH value and then the receiver will be automatically disabled. After the receiver is enabled, software can disable the receiver by setting the URRXEN bit to "0".

Synchronous Mode

The data is transmitted in a full-duplex style in the USART Synchronous Master Mode, i.e., data transmission and reception both occur at the same time and only support master mode. The USART UR_CTS/SCK pin is the synchronous USART transmitter clock output. In this mode, no clock pulses will be sent to the UR_CTS pin during the start bit, parity bit and stop bit duration. The CPS bit in the Synchronous Control Register, SYNCR, can be used to determine whether data is captured on the first or the second clock edge. The CPO bit in the SYNCR can be use to configure the clock polarity in the USART Synchronous Mode idle state. Detailed timing information is shown in the accompanying diagram.

In the USART synchronous Mode, the UR_CTS/SCK clock output pin is only used to transmit the data to slave device. If the transmission data register TBR, is written with valid data, the USART synchronous mode will automatically transmit this data with the corresponding clock output and the USART receiver will also receive data on the UR_RX pin. Otherwise the receiver will not obtain synchronous data if no data is transmitted.



Note: The USART supports the synchronous master mode only: it cannot receive or send data related to an input clock. The USART clock is always an output.

Figure 146. USART Synchronous Transmission Example

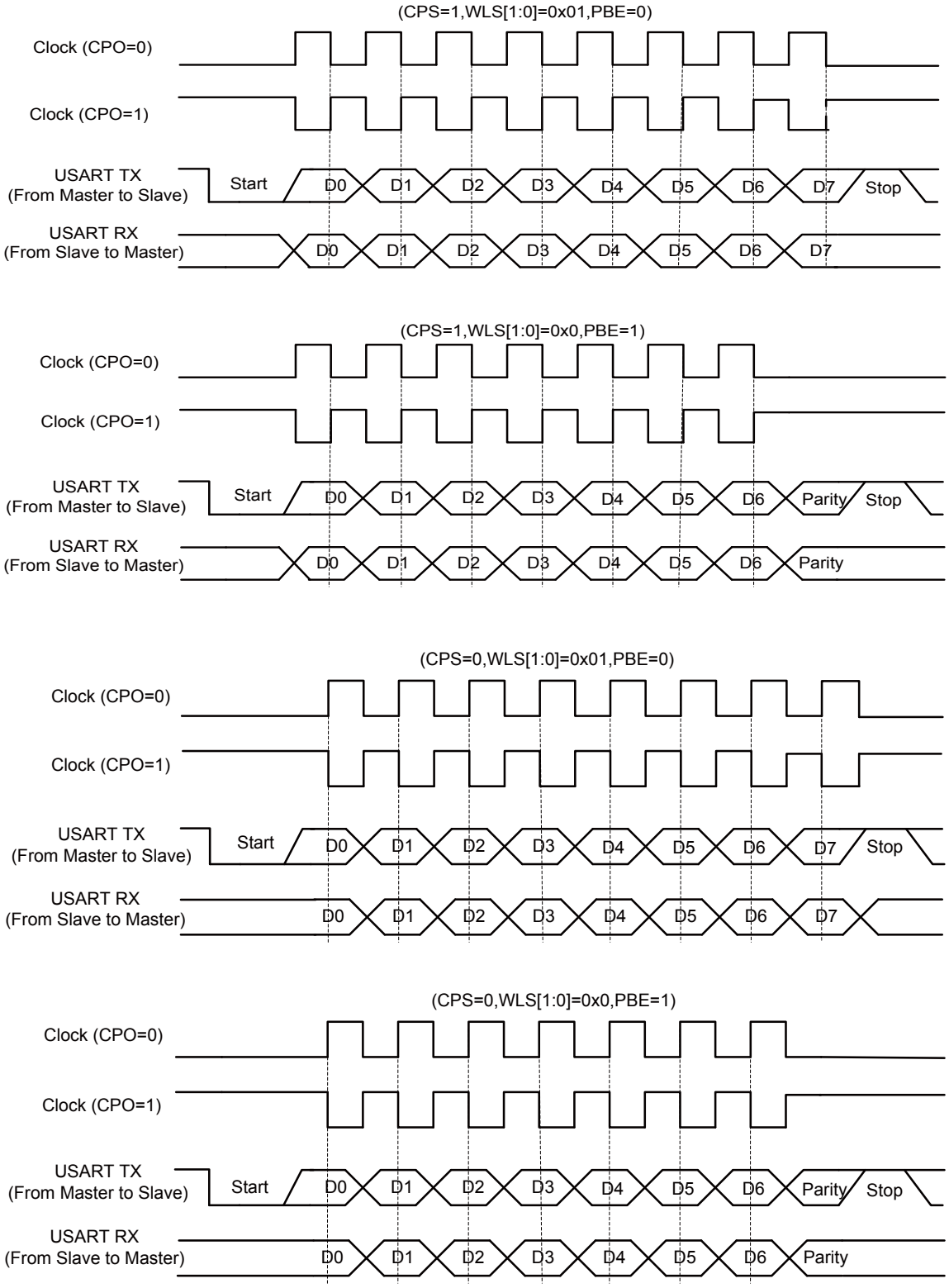


Figure 147. 8-bit Format USART Synchronous Waveform

Hardware Flow Control

The RS485 interface supports the hardware flow control function which is enabled by setting the HFCEN bit in the MODCR register to 1. The hardware flow control function is categorized into to types. One is the RTS flow control function and the other is the CTS flow control function.

RTS Flow Control

In the RTS flow control, the UR_RTS pin is active with a logic low state when the RX FIFO is empty. It means that the receiver is ready to receive a new data. When the RX FIFO reaches the trigger level which is specified by configuring the RFTL field in the FCR register, the UR_RTS pin is inactive with a logic high state. Figure 148 shows the example of RTS flow control.

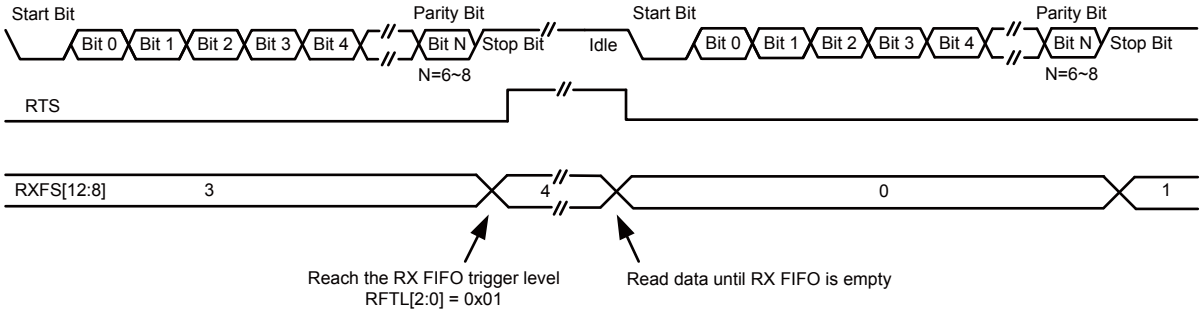


Figure 148. USART RTS Flow Control

CTS Flow Control

If the hard flow control function is enabled, the URTXEN bit in the FCR register is controlled by the UR_CTS input signal. If the UR_CTS pin is forced to a logic low state, the URTXEN bit will automatically be set to 1 to enable the data transmission. However, if the UR_CTS pin is forced to a logic high state, the URTXEN bit will be cleared to 0 and then the data transmission will also be disabled.

When the UR_CTS pin is forced to a logic high state during a data transmission, the current data transmission will be continued until the stop bit is completed. The figure 148 shows an example of communication with CTS flow control.

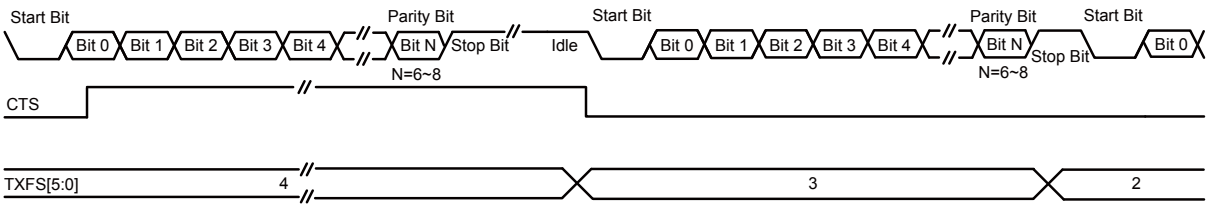


Figure 149. USART CTS flow control

Interrupts and Status

The USART module can generate an interrupt when the following event occurs:

- Receiver Line Status Interrupt (Irpt_RLSI): Occurrence of USART overrun error, parity error, framing error, or break events.
- Receiver FIFO Threshold Level Interrupt (Irpt_RFTLI): When the FIFO received data amount has reached the specified threshold level.
- Receiver FIFO Time-out Interrupt (Irpt_RTOI): When the USART receiver FIFO does not receive a new data package during the specified time-out interval.
- Transmitter FIFO Threshold Level Interrupt (Irpt_TFTLI): When the data to be transmitted in the USART transmitter FIFO is less than the specified threshold level.
- MODEM Status Interrupt (Irpt_MODSI): When the DCD, RI, DSR, or CTS bits states in the in the MODSR register have changed.

PDMA Interface

The PDMA interface is integrated in the USART module. The PDMA function can be enabled by setting the TXDMAEN or RXDMAEN bit in the MDR register to 1 in the transmitter or receiver mode respectively. When the data to be transmitted in the USART transmitter FIFO is less than the TX FIFO threshold level specified by the TFTL field in the FCR register and the TXDMAEN bit is set to 1, the PDMA function will be activated to move data from a certain memory location into the USART TX FIFO.

Similarly, when the received data amount in the receiver FIFO is equal to the RX FIFO threshold level specified by the RFTL field in the FCR register and the RXDMAEN bit is set to 1, the PDMA function will be activated to move data from the USART RX FIFO to a specific memory location.

For a mode detailed description on the PDMA configurations, refer to the PDMA chapter.

Register Map

The following table shows the USART registers and reset values.

Table 51. USART Register Map

Register	Offset	Description	Reset Value
USART0 Base Address=0x4000_0000 USART1 Base Address=0x4004_0000			
RBRn	0x000	USARTn Receiver Buffer Register	0x0000_0000
TBRn	0x000	USARTn Transmitter Buffer Register	0x0000_0000
IERn	0x004	USARTn Interrupt Enable Register	0x0000_0000
IIRn	0x008	USARTn Interrupt Identification Register	0x0000_0001
FCRn	0x00C	USARTn FIFO Control Register	0x0000_0001
LCRn	0x010	USARTn Line Control Register	0x0000_0000
MODCRn	0x014	USARTn Modem Control Register	0x0000_0000
LSRn	0x018	USARTn Line Status Register	0x0000_0060
MODSRn	0x01C	USARTn Modem Status Register	0x0000_0000
TPRn	0x020	USARTn Timing Parameter Register	0x0000_0000
MDRn	0x024	USARTn Mode Register	0x0000_0000
IrDACRn	0x028	USARTn IrDA Control Register	0x0000_0000
RS485CRn	0x02C	USARTn RS485 Control Register	0x0000_0000
SYNCRn	0x030	USARTn Synchronous Control Register	0x0000_0000
FSRn	0x034	USARTn FIFO Status Register	0x0000_0000
DLRn	0x038	USARTn Divider Latch Register	0x0000_0010
DEGTSTRn	0x040	USARTn Debug/Test Register	0x0000_0000

Register Descriptions

USARTn Receiver Buffer Register – RBRn, n=0 or 1

The register is used to store the USARTn received data.

Offset: 0x000

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							RD
Type/Reset								RO 0
	7	6	5	4	3	2	1	0
	RD							
Type/Reset	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0

Bits	Field	Descriptions
[8:0]	RD	Reading the data via this receiver buffer register will return the data from the receiver FIFO. The receiver FIFO has a capacity of up to 16×9 bits. By reading this register, the USART will return a 7, 8 and 9-bit received data. The RD field bit 8 is valid for 9-bit mode only and is fixed at 0 for the 8-bit mode. For the 7-bit mode, the receiver buffer register RD[6:0] contain the available bits.

USARTn Transmitter Buffer Register – TBRn, n=0 or 1

The register is used to specify the USARTn transmitted data.

Offset: 0x000

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							TD
Type/Reset								WO 0
	7	6	5	4	3	2	1	0
	TD							
Type/Reset	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0

Bits	Field	Descriptions
[8:0]	TD	Writing data to this transmitter buffer register will load data into the transmitter FIFO. The transmitter FIFO has a capacity of up to 16×9 bits. By writing to this register, the USART will send out 7,8 or 9-bit transmitted data. The TD field bit 8 is valid for the 9-bit mode only and will be ignored for the 8-bit mode. For the 7-bit mode, the transmitter buffer register TD [6:0] contains the available bits.

USARTn Interrupt Enable Register – IERn, n=0 or 1

This register is used to enable or disable the related USARTn interrupt function. The USARTn module generates interrupts to the controller when the corresponding events occur and the corresponding interrupt enable bits are set.

Offset: 0x004

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved				MODSIE	RLSIE	TFTLIE	RFTLI_RTOIE
Type/Reset					RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[3]	MODSIE	MODEM Status Interrupt Enable (Irpt_MODSI) 0: Mask Irpt_MODSI 1: Enable Irpt_MODSI
[2]	RLSIE	Receive Line Status Interrupt Enable (Irpt_RLSI) 0: Mask Irpt_RLSI 1: Enable Irpt_RLSI
[1]	TFTLIE	Transmitter FIFO Threshold Level Interrupt (Irpt_TFTLI) Enable 0: Mask Irpt_TFTLI 1: Enable Irpt_TFTLI
[0]	RFTLI_RTOIE	Receiver FIFO Threshold Level Interrupt Enable (Irpt_RFTLI) or receiver FIFO Time-Out Interrupt Enable (Irpt_RTOI) 0: Mask Irpt_RFTLI and Irpt_RTOI 1: Enable Irpt_RFTLI or Irpt_RTOI

USARTn Interrupt Identification Register – IIRn, n=0 or 1

This register is used to identify the interrupt source including the FIFO threshold and USARTn Receiver/Transmitter status.

Offset: 0x008

Reset value: 0x0000_0001

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved				IID			NIP
Type/Reset					RO 0	RO 0	RO 0	RO 1

Bits	Field	Descriptions
[3:1]	IID	Interrupt Identification The detailed interrupt descriptions are shown in the accompanying table. The IID and NIP bits indicate the current USART interrupt request.
[0]	NIP	No Interrupt Pending 1: No pending USRAT interrupt 0: Pending USART interrupts

Table 52. USART Interrupt Control Function

IID & NIP	Priority	Interrupt Type	Interrupt Source	Interrupt Reset control
xxx1	NA	None	None	NA
0110	Highest	Receiver Line Status Interrupt (Irpt_RLSI)	USART occurs overrun error, parity error, framing error, or break events. [note] In RS485 mode, it can indicate the address detection.	Reading the LSR register
0100	Second	Receiver FIFO Threshold Level Interrupt (Irpt_RFTLI)	Receiver FIFO threshold level is reached	Read the RBR register to decrease the receiver FIFO level to less than the specified threshold
1100	Second	Receiver FIFO Time-out Interrupt (Irpt_RTOI)	Receiver FIFO is not empty and no activities have occurred in the receiver FIFO during the RTOIC time-out duration	Reading the RBR register
0010	Third	Transmitter FIFO Threshold Level Interrupt (Irpt_TFTLI)	Transmitter FIFO level is less than the transmitter FIFO threshold level which is set by the TFTL field in the FIFO Control Register named FCR	Writing data into the TBR register
0000	Fourth	MODEM Status Interrupt (Irpt_MODSI)	The DCDS, RIS, DSRS, or CTSS bits in the MODSR register have changing state.	Reading the MODSR register – optional

USARTn FIFO Control Register – FCRn, n=0 or 1

This register specifies the USARTn FIFO control and configurations including threshold level and reset function.

Offset: 0x00C

Reset value: 0x0000_0001

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved						URRXEN	URTXEN
Type/Reset							RW 0	RW 0
	7	6	5	4	3	2	1	0
		RFTL		TFTL	Reserved	TFR	RFR	FME
Type/Reset	RW 0	RW 0	RW 0	RW 0		WO 0	WO 0	RO 1

Bits	Field	Descriptions
[9]	URRXEN	USART RX Enable 0: Disable 1: Enable
[8]	URTXEN	USART TX Enable 0: Disable 1: Enable
[7:6]	RFTL	RX FIFO Threshold Level Setting The RFTL field defines the RX FIFO trigger level. 00: 1 byte 01: 4 bytes 10: 8 bytes 11: 14 bytes
[5:4]	TFTL	TX FIFO Threshold Level Setting The TFTL field determines the TX FIFO trigger level. 00: 0 byte 01: 2 bytes 10: 4 bytes 11: 8 bytes
[2]	TFR	TX FIFO Reset Setting this bit will generate a reset pulse to reset TX FIFO which will empty the TX FIFO. i.e., the TX pointer will be reset to 0, after a reset signal. This bit returns to 0 automatically after the reset pulse is generated.
[1]	RFR	RX FIFO Reset Setting this bit will generate a reset pulse to reset the RX FIFO which will empty the RX FIFO. i.e., the RX pointer will be reset to 0, after a reset signal. This bit returns to 0 automatically after the reset pulse is generated.
[0]	FME	FIFO Mode Enable Because the USART module is always operated in the FIFO mode, writing to this bit will have no effect.

USARTn Line Control Register – LCRn, n=0 or 1

The line control register specifies the serial parameters such as data length, parity, and stop bit for the USARTn module.

Offset: 0x010

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved	BCB	SPE	EPE	PBE	NSB		WLS
Type/Reset		RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[6]	BCB	Break Control Bit When this bit is set 1, the serial data output on the UR_TX pin will be forced to the Spacing State (logic 0). This bit acts only on UR_TX output pin and has no effect on the transmitter logic.
[5]	SPE	Stick Parity Enable 0: Disable stick parity 1: Stick Parity bit is transmitted This bit is only available when the PBE bit is set to 1. If both the PBE and SPE bits are set to 1 and the EPE bit is cleared to 0, the transmitted parity bit will be set to 1. However, when the PBE and SPE bits are set to 1 and also the EPE bit is set to 1, the transmitted parity bit will be cleared to 0.
[4]	EPE	Even Parity Enable 0: Odd number of logic 1's are transmitted or checked in the data word and parity bits 1: Even number of logic 1's are transmitted or checked in the data word and parity bits This bit is only available when PBE is set to 1.
[3]	PBE	Parity Bit Enable 0: Parity bit is not generated (transmitted data) or checked (receive data) during transfer 1: Parity bit is generated or checked during transfer **Note:** When the WLS field is set to "10" to select the 9-bit data format, writing to the PBE bit has no effect.
[2]	NSB	Number of "STOP bit" 0: One "STOP bit" is generated in the transmitted data 1: Two "STOP bit" is generated when 8-bit and 9-bit word length is selected
[1:0]	WLS	Word Length Select 00: 7 bits 01: 8 bits 10: 9 bits 11: Reserved

USARTn Modem Control Register – MODCRn, n=0 or 1

This register contains a related modem control.

Offset: 0x014

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved					HFCEN	RTS	DTR
Type/Reset						RW 0	RW 0	RW 0

Bits	Field	Descriptions
[2]	HFCEN	Hardware Flow Control Function Enable 0: Disabled 1: Enabled
[1]	RTS	RTS – Request-To-Send Signal 0: Drive UR_RTS pin to logic 1 1: Drive UR_RTS pin to logic 0 Note that the RTS bit is used to control the UR_RTS pin status when the HFCEN bit is set.
[0]	DTR	DTR – Data-Terminal-Ready Signal 0: Drive DTR pin to logic 1 1: Drive DTR pin to logic 0

USARTn Line Status Register – LSRn, n=0 or 1

This register contains the corresponding USARTn status.

Offset: 0x018

Reset value: 0x0000_0060

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							RSADDEF
Type/Reset								RC 0
	7	6	5	4	3	2	1	0
	ERRRX	TXEMPT	TXFEMPT	BII	FEI	PEI	OEI	RFDR
Type/Reset	RC 0	RO 1	RO 1	RC 0	RC 0	RC 0	RC 0	RO 0

Bits	Field	Descriptions
[8]	RSADDEF	RS485 Address Detection Flag 0: Address is not detected 1: Address is detected This bit is set to 1 when the receiver detects the address and is cleared to 0 when the LSR register is read. **Note:** This bit is only used In the RS485 mode by setting the MDR field to “b10”.
[7]	ERRRX	RX FIFO Error 0: RX FIFO works normally 1: There is at least one parity error (PE), framing error (FE), or break indication (BI) in the receiver FIFO The ERRRX bit is cleared when the CPU reads the LSR register and if there are no subsequent errors in the RX FIFO.
[6]	TXEMPT	Transmitter Empty 0: Either Transmitter FIFO (TX FIFO) or Transmitter Shift Register (TSR) is not empty 1: Both the TX FIFO and TSR register are empty
[5]	TXFEMPT	Transmitter FIFO Empty 0: TX FIFO is not empty 1: TX FIFO is empty The TXFEMPT bit is set when the last data package in the TX FIFO is transferred to the Transmitter Shift Register (TSR). This bit is reset when the TBR (or TX FIFO) is loaded with new data. This bit also causes the USART to issue an interrupt (Irpt_TFTLI) to the CPU when the TFTLIE bit in the IER register is set to 1 to enable the relevant interrupt and when the TFTL field in the FCR register is set to the value 0.
[4]	BII	Break Interrupt Indicator This bit is set to 1 whenever the received data input is held in the "spacing state" (logic 0) for longer than a full word transmission time, which is the total time of "start bit" + data bits + "parity" + "stop bits" duration, and is reset whenever the CPU reads the contents of this LSR register.

Bits	Field	Descriptions
[3]	FEI	Framing Error Indicator This bit is set 1 whenever the received character does not have a valid "stop bit" , which means, the stop bit following the last data bit or parity bit is detected as a logic 0, and is reset whenever the CPU reads the contents of this LSR register.
[2]	PEI	Parity Error Indicator This bit is set to 1 whenever the received character does not have a valid "parity bit" and is reset whenever the CPU reads the contents of this LSR register.
[1]	OEI	Overrun Error Indicator An overrun error will occur only after the RX FIFO is full and when the next character has been completely received in the RX shift register. The character in the shift register is overwritten, when an overrun event occurs, but it is not transferred to the RX FIFO. The OEI bit is used to indicate to the CPU as soon as it happens and is reset whenever the CPU reads the contents of this LSR register.
[0]	RFDR	RX FIFO Data Ready 0: RX FIFO is empty 1: RX FIFO contains at least 1 received data word

USARTn Modem Status Register – MODSRn, n=0 or 1

This register contains the USARTn modem status bits.

Offset: 0x01C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	DCDS	RIS	DSRS	CTSS	DDCD	DRI	DDSR	DCTS
Type/Reset	RO 0	RO 0	RO 0	RO 0	RC 0	RC 0	RC 0	RC 0

Bits	Field	Descriptions
[7]	DCDS	DCD – Data-Carrier-Detect Status 0: UR_DCD pin is inactive 1: UR_DCD pin is active and kept at 0
[6]	RIS	UR_RI Ring-Indicator Status 0: UR_RI pin is inactive 1: UR_RI pin is active and kept at 0
[5]	DSRS	UR_DSR Data-Set-Ready Status 0: UR_DSR pin is inactive 1: UR_DSR pin is active and kept at 0
[4]	CTSS	UR_CTS Clear-To-Send Status 0: UR_CTS pin is inactive 1: UR_CTS pin is active and kept at 0
[3]	DDCD	Detect UR_DCD Status Change This bit is set whenever the UR_DCD input pin status has been changed and will be reset if the CPU reads this MODSR register. When the DDCD bit is set to 1, a modem status interrupt is generated if the MODSIE bit in the IER register is set to 1.
[2]	DRI	Detect UR_RI Status Change This bit is set whenever the UR_RI input pin status has been changed and will be reset if the CPU reads the MODSR register. When the DIR bit is set to 1, a modem status Interrupt is generated if the MODSIE bit in the IER register is set to 1.
[1]	DDSR	Detect UR_DSR Status Change This bit is set whenever the UR_DSR input pin status has been changed and will be reset if the CPU reads the MODSR register. When the DDSR bit is set to 1, a modem status Interrupt is generated if the MODSIE bit in the IER register is set to 1.
[0]	DCTS	Detect UR_CTS Status Change This bit is set whenever the UR_CTS input pin status has been changed and will be reset if the CPU reads the MODSR register. When the DCTS bit is set to 1, a modem status Interrupt is generated if the MODSIE bit in the IER register is set to 1.

USARTn Timing Parameter Register – TPRn, n=0 or 1

This register contains the USARTn timing parameters including the transmitter time guard parameters and the receiver FIFO time-out value together with the RX FIFO time-out interrupt enable control.

Offset: 0x020

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	TG							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	RTOIE	RTOIC						
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:8]	TG	Transmitter Time Guard The transmitter time guard counter is driven by the baud rate clock. When the TX FIFO transmits data, the counter is reset and then starts to count. Only when the counter content is equal to the TG value, are further word transmission transactions allowed.
[7]	RTOIE	Receiver FIFO Time Out Interrupt Enable The receiver FIFO time-out interrupt is enabled only when the RFTLI_RTOIE bit in the IER register is set to 1.
[6:0]	RTOIC	Receiver FIFO Time-Out Interrupt Compare value The RX FIFO time-out counter, TOUT_CNT, is driven by the baud rate clock. When the RX FIFO receives new data, the counter is reset and then starts to count. Once the time-out counter content is equal to the time-out interrupt compare RTOIC value, a receiver FIFO time-out interrupt, Irpt_RTOI, is generated if the RFTLI_RTOIE bit in the IER register is set to 1. New received data or the empty RX FIFO after being read will clear the RX FIFO time-out counter.

USARTn Mode Register – MDRn, n=0 or 1

This register specifies the USARTn mode and the data transfer mode selections.

Offset: 0x024

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
		Reserved	RXDMAEN	TXDMAEN	Reserved	TRSM	MODE	
Type/Reset			RW 0	RW 0		RW 0	RW 0	RW 0

Bits	Field	Descriptions
[5]	RXDMAEN	USART RX PDMA Enable 0: Disabled 1: Enabled
[4]	TXDMAEN	USART TX PDMA Enable 0: Disabled 1: Enabled
[2]	TRSM	Transfer Mode Selection This bit is used to select the data transfer protocol. 0: LSB first 1: MSB first
[1:0]	MODE	USART Mode Selection. 00: Normal operation 01: IrDA 10: RS485 11: Synchronous

USARTn IrDA Control Register – IrDACRn, n=0 or 1

This register specifies the corresponding USARTn enable control and mode selections for the IrDA mode operation.

Offset: 0x028

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	IrDAPSC							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
		Reserved	RXINV	TXINV	LB	TXSEL	IrDALP	IrDAEN
Type/Reset			RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:8]	IrDAPSC	IrDA Prescaler value This field contains the 8-bit debounce prescaler value. The debounce count-down counter is driven by the USART clock, named as CK_USART. The counting period is specified by the IrDAPSC field. The IrDAPSC field must be set to a value equal to or greater than 0x01 to for normal debounce counter operation. If the pulse width is less than the duration specified by the IrDAPSC field, the pulse will be considered as glitch noise and discarded. 00000000: Reserved – can not be used 00000001: CK_USART clock divided by 1 00000010: CK_USART clock divided by 2 00000011: CK_USART clock divided by 3 ...
[5]	RXINV	RX Signal Inverse Control 0: No inversion 1: RX input signal is inversed
[4]	TXINV	TX Signal Inverse Control 0: No inversion 1: TX output signal is inversed
[3]	LB	IrDA Loop Back Mode 0: Disable IrDA loop back mode 1: Enable IrDA loop back mode for self testing
[2]	TXSEL	Transmit Select 0: Enable IrDA receiver 1: Enable IrDA transmitter
[1]	IrDALP	IrDA Low Power Mode Select the IrDA operation mode. 0: Normal mode 1: IrDA low power mode
[0]	IrDAEN	IrDA Enable control 0: Disable IrDA mode 1: Enable IrDA mode

USARTn RS485 Control Register – RS485CRn, n=0 or 1

This register contains the USARTn UR_RTS/TXE pin polarity for the RS485 mode.

Offset: 0x02C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	ADDMATCH							
Type/Reset	RW 0							
	7	6	5	4	3	2	1	0
	Reserved					RSAAD	RSNMM	TXENP
Type/Reset						RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:8]	ADDMATCH	RS485 Auto Address Match value The field contains the address match value for the RS485 auto address detection operation mode.
[2]	RSAAD	RS485 Auto Address Detection Operation Mode Control 0: Disable 1: Enable
[1]	RSNMM	RS485 Normal Multi-drop Operation Mode Control 0: Disable 1: Enable
[0]	TXENP	UR_RTS/TXE Pin Polarity 0: UR_RTS/TXE is active high in the RS485 transmission mode 1: UR_RTS/TXE is active low in the RS485 transmission mode

USARTn Synchronous Control Register – SYNCRn, n=0 or 1

This register is used to control the USARTn synchronous clock pin and the clock polarity together with the clock phase for the synchronous mode.

Offset: 0x030

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved				CPO	CPS	Reserved	CLKEN
Type/Reset					RW 0	RW 0		RW 0

Bits	Field	Descriptions
[3]	CPO	Clock Polarity Selects the polarity of the clock output on the UR_CTS/SCK pin in the synchronous mode. Works in conjunction with the CPS bit to specify the desired clock idle state. 0: UR_CTS/SCK pin idle state is low 1: UR_CTS/SCK pin idle state is high
[2]	CPS	Clock Phase This bit allows the user to select the phase of the clock output on the UR_CTS/SCK pin in the synchronous mode. Works in conjunction with the CPO bit to determine the data capture edge. 0: Data is captured on the first clock edge 1: Data is captured on the second clock edge
[0]	CLKEN	Clock Enable Enable/disable the UR_CTS/SCK pin. 0: UR_CTS/SCK pin disabled 1: UR_CTS/SCK pin enabled

USARTn FIFO Status Register – FSRn, n=0 or 1

This register is the USARTn FIFO status register.

Offset: 0x034

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved			RXFS				
Type/Reset				RO 0	RO 0	RO 0	RO 0	RO 0
	7	6	5	4	3	2	1	0
	Reserved			TXFS				
Type/Reset				RO 0	RO 0	RO 0	RO 0	RO 0

Bits	Field	Descriptions
[12:8]	RXFS	RX FIFO Status The RXFS field shows the current number of data contained in the RX FIFO. 00000: Rx FIFO is empty 00001: Rx FIFO contains 1 data ... 10000: Rx FIFO contains 16 data Others: Reserved
[4:0]	TXFS	TX FIFO Status The TXFS field shows the current number of data contained in the TX FIFO. 00000: TX FIFO is empty 00001: TX FIFO contains 1 data ... 10000: TX FIFO contains 16 data Others: Reserved

USARTn Divider Latch Register – DLRn, n=0 or 1

The register is used to determine the USARTn clock divided ratio to generate the appropriate baud rate.

Offset: 0x038

Reset value: 0x0000_0010

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	BRD							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	BRD							
Type/Reset	RW 0	RW 0	RW 0	RW 1	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	BRD	Baud Rate Divider The 16 bits define the USART clock divider ratio. Baud Rate=CK_USART/BRD Where the CK_USART clock is the system clock connected to the USART module. The BRD field can be set from 16 to 65535.

USARTn Debug/Test Register – DEGTSTRn, n=0 or 1

This register controls the USARTn debug mode.

Offset: 0x040

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved						LBM	
Type/Reset							RW 0	RW 0

Bits	Field	Descriptions
[1:0]	LBM	Loopback Test Mode Select 00: Normal Operation 01: Reserved 10: Automatic Echo Mode 11: Loopback Mode

22 Smart Card Interface (SCI)

Introduction

The Smart Card Interface, SCI, is compatible with the ISO 7816-3 standard. This interface includes functions for card Insertion/Removal detection, SCI data transfer control logic and data buffers, internal Timer Counters and corresponding control logic circuits to perform the required Smart Card operations. The Smart Card interface acts as a Smart Card Reader to facilitate communication with the external Smart Card. The overall functions of the Smart Card interface are controlled by a series of registers including control and status registers together with several corresponding interrupts which are generated to get the attention of the microcontroller for SCI transfer status.

As the complexity of ISO7816-3 standard data protocol does not permit comprehensive specifications to be provided in this datasheet, the reader should therefore consult other external information for a detailed understanding of this standard.

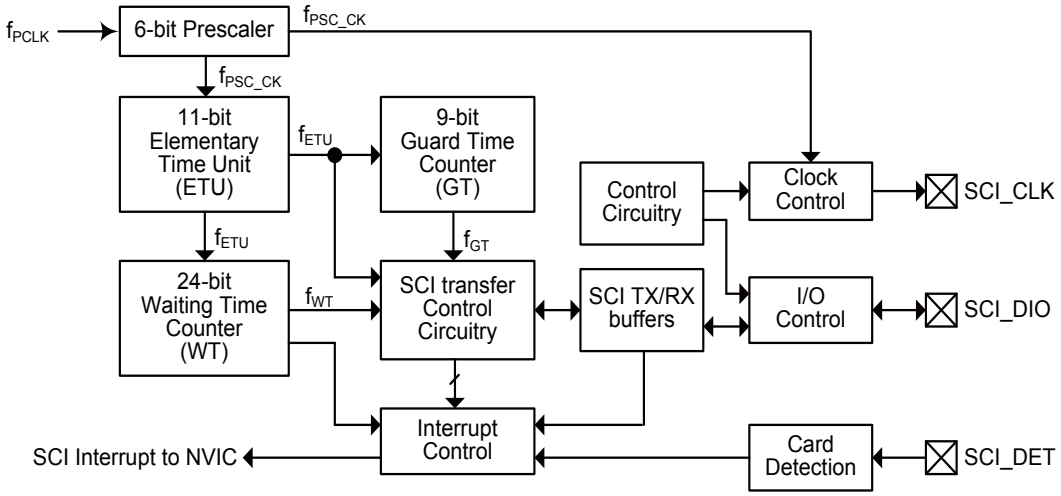


Figure 150. SCI Block Diagram

Features

- Supports ISO 7816-3 standard
- Character Transfer Mode
- 1 transmit buffer and 1 receive buffer
- 11-bit ETU (elementary time unit) counter
- 9-bit guard time counter
- 24-bit general purpose waiting time counter
- Parity generation and checking
- Automatic character repetition on parity error detection in transmission and reception modes
- Supports PDMA access at a transmission or reception completion

Functional Descriptions

To communicate with an external Smart Card, the integrated Smart Card Interface has a series of external pins known as SCI_CLK, SCI_DIO and SCI_DET. The SCI_CLK pin is the clock output signal used to communicate with the external Smart Card together with the serial data pin named SCI_DIO. The operation of the SCI_CLK and SCI_DIO pins can be selected to be the SCI data Transfer Mode which is driven automatically by the SCI control circuits or to be the Manual mode which is controlled by configuring the internal CLK and DIO register bits respectively by the application program. The SCI_DET pin is the external card detection input pin. Insertion or removal of the external Smart Card can be automatically detected and generate an interrupt signal which is sent to the microcontroller if the corresponding interrupt function is enabled.

For proper data transfer, some timing related procedures must be executed before the Smart Card Interface can begin to communicate with the external card. There are three counters named Elementary Time Unit, ETU, Guard Time Counter, GT, and Waiting Time Counter, WT, which are used for the timing related functions in Smart Card Interface data transfer operations.

Elementary Time Unit Counter

The Elementary Time Unit, ETU, is an 11-bit up-counting counter which generates a clock denoted as f_{ETU} to be used as the operating frequency source for the SCI data transmission and reception. The clock source of the ETU comes from the Smart Card clock, named f_{PSC_CK}, which is derived from the 6-bit prescaler. The data transfer of the SCI is a character frame based protocol, which basically consists of a Start bit, 8-bit of data and a Parity bit. The time period, t_{ETU} ($1/f_{ETU}$), generated by the ETU, is the time unit for a character bit. There is a register related to the Elementary Time Unit known as the ETUR register which stores the expected contents of the ETU. Each time the ETUR register is written, the ETU circuitry will reload the new written value and restart counting. The elementary time unit t_{ETU} is obtained from the following formula which defines the bit rate in the ISO 7816-3 standard specification.

$$1 \text{ etu} = t_{ETU} = \frac{F_i}{D_i} \times \frac{1}{f}$$

where:

- **etu** is the nominal duration of the data bit on the signal SCI_DIO provided to the card by the interface
- $\mathbf{D_i}$ is the bit-rate adjustment factor
- $\mathbf{F_i}$ is the clock rate conversion factor
- **f** is the frequency value of the clock signal SCI_CLK provided to the card by the interface

D_i is an encoded decimal value based on a 4-bit field, named DI, as represented in the accompanying table.

Table 53. DI Field Based D_i Encoded Decimal Values

DI field	0001	0010	0011	0100	0101	0110	1000	1001
D_i (decimal)	1	2	4	8	16	32	12	20

F_i is an encoded decimal value based on a 4-bit field, named FI, as represented in the following table.

Table 54. FI Field Based F_i Encoded Decimal Values

FI field	0000	0001	0010	0011	0100	0101	0110	1001	1010	1011	1100	1101
F_i (decimal)	372	372	558	744	1116	1488	1860	512	768	1024	1536	2048

The values of FI and DI, as they appear in the preceding tables, will be obtained from the Answer-to-Reset packet sent from the external Smart Card to the Smart Card Interface the first time the external Smart Card is inserted. When the SCI receives the FI and DI information, the F_i and D_i values can be obtained by looking up the preceding two tables. After the F_i and D_i values are obtained, the value which should be written into the ETUR register can be calculated by F_i/D_i. The following table shows the possible ETU values obtained by the F_i/D_i ratio.

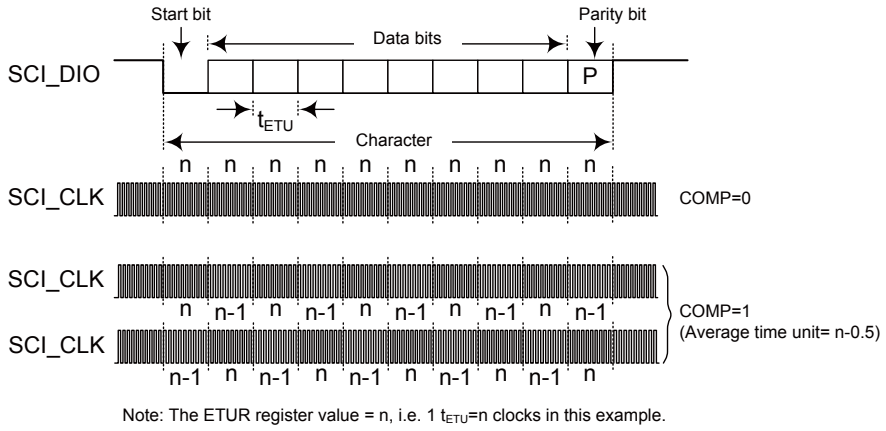
Table 55. Possible ETU Values Obtained with the F_i/D_i Ratio

D_i \ F_i	372	558	774	1116	1488	1860	512	768	1024	1536	2048
1	372	558	744	1116	1488	1860	512	768	1024	1536	2048
2	186	279	372	558	744	930	256	384	512	768	1024
4	93	139.5	186	279	372	465	128	192	256	384	512
8	46.5	69.75	93	139.5	186	232.5	64	96	128	192	256
16	23.25	34.87	46.5	69.75	93	116.2	32	48	64	96	128
32	22.62	17.43	23.25	34.87	46.5	58.13	16	24	32	48	64
12	31	46.5	62	93	124	155	42.66	64	85.33	128	170.6
20	18.6	27.9	37.2	55.8	74.4	93	25.6	38.4	51.2	76.8	102.4

Compensation mode

As the value of the ETUR register is obtained by the above procedure, the calculation results of the value may not be an integer. If the calculation result is not an integer and is less than the integer n but greater than the integer (n-1), either the integer n or (n-1) should be written into the ETUR register depending upon whether the result is closer to integer n or (n-1). The integer n mentioned here is a decimal.

If the calculation result is close to the value of (n-0.5), the compensation mode should be enabled by setting the compensation enable control bit, COMP, in the ETUR register to 1 for successful data transfer. When the result is close to the value of (n-0.5) and the compensation mode is enabled, the value written into the ETUR register should be n. The ETU circuitry will then generate the time unit sequence with n clock cycles and next (n-1) clock cycles alternately and so on. This results in an average time unit of (n-0.5) clock cycles and allows a time granularity down to a half clock cycle. Note that the ETU will reload the ETUR register value and restart counting at the time when the Start bit appears in the SCI data Transfer Mode.



Note: The ETUR register value = n, i.e. 1 t_{ETU}=n clocks in this example.

Figure 151. Character Frame and Compensation Mode

Guard Time Counter

The Guard Time Counter, GT, is a 9-bit up-counting counter which generates a minimum time duration known as a character frame, denoted as t_{GT}, between the leading edges of two consecutive characters in the SCI data transfer. The clock source of the guard time counter comes from the ETU, named f_{ETU} in the block diagram. There is a register related to the guard time counter known as the GTR register, which stores the expected value of the guard time counter. The guard time value will be reloaded at the end of the current guard time period. Note that the guard time between the last character received from the Smart Card and the next character transmitted by the SCI circuitry which should be properly managed by the application program. There is no guard time insertion when the first character is transmitted.

Waiting Time Counter

The Waiting Time counter, WT, is a 24-bit down counting counter which generates a maximum time duration, denoted as t_{WT}, for data transfer. The clock source of the waiting time counter comes from the ETU and is named f_{ETU}.

There is a register for the waiting time counter known as the WTR register which stores the expected waiting time counter value. The waiting time counter can be used in both the SCI data Transfer Mode and Manual Mode and can reload the value for specific conditions. The function of the waiting time counter is controlled by the WTEN bit in the CR register. When the SCI is configured to be operated in the SCI data Transfer Mode and the waiting time counter is enabled by setting the WTEN bit to 1, the updated WTR register value will be loaded into the waiting time counter when the Start bit is detected. Note that the WTEN bit should not be set to 1 to enable the waiting time counter in the SCI data Transfer Mode until after the external Smart Card is inserted.

If the SCI is configured to operate in the Manual Mode, the waiting time counter can be used as a general purpose timer and this timer is enabled or disabled by setting or clearing the WTEN bit. The updated WTR register value will not be loaded into the waiting time counter if the waiting time counter is enabled. When the waiting time counter is disabled by setting the WTEN bit to 0 and an updated value is written into the WTR register, the new value will immediately be loaded into the waiting time counter and then the counter will start to count after the WTEN bit is again set to 1.

Software can change the Waiting Time value on-the-fly. For example, in T=1 mode, the value of the Block Waiting Time, t_{BWT}, should be written into the WTR register before the Start bit of the last transmitted character occurs. After the transmission of the last character is completed, software should write the Character Waiting Time value, t_{CWT}, into the WTR register.

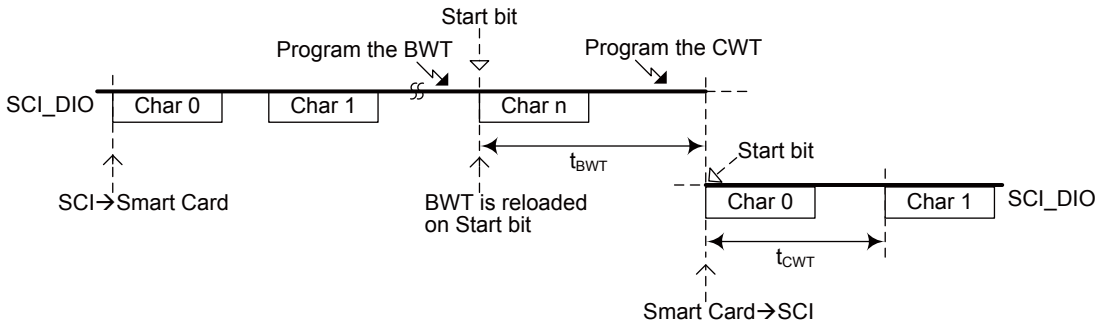


Figure 152. Character and Block Waiting Time Duration – CWT and BWT

Card Clock and Data Selection

The SCI communicates with an external Smart Card using a series of external pins. These are the serial data pin, SCI_DIO, output clock pin, SCI_CLK, and the Card Detection input pin, SCI_DET.

The SCI serial data pin, named SCI_DIO, can be controlled by the SCI hardware circuitry or the software control bits depending upon whether the SCI is operated in the SCI Transfer Mode or in the Manual Mode. The mode selection is determined by the SCIM bit in the CR register. The SCI_DIO pin status is controlled by the CDIO bit in the CCR register when the SCI is configured to operate in the Manual mode by clearing the SCIM bit in the CR register. In the Manual Mode the SCI_DIO pin status is a copy of the CDIO bit. However, when the SCI is configured to operate in the SCI Transfer Mode, the SCI_DIO pin status is determined by the SCI transfer circuitry.

The SCI clock output pin named SCI_CLK can be controlled by the 6-bit SCI prescaler or the software control bits depending upon the condition of the CLKSEL bit in the CCR register. The SCI_CLK pin status is controlled by the CCLK bit in the CCR register when the CLKSEL bit is cleared to 0. The SCI_CLK pin status is a copy of the CCLK bit. However, when the CLKSEL bit is set to 1, the SCI_CLK signal is sourced from the 6-bit prescaler output. The prescaler division ratio is determined by the PSC field in the PSCR register.

Card Detection

When an external Smart Card is inserted, the internal card detector can detect this insertion operation and generate a card insertion interrupt if the corresponding interrupt enable control bit, CARDIRE, in the IER register is set to 1. Similarly, if the card is removed, the internal card detector can also detect the removal and consequently generate a card removal interrupt when the corresponding interrupt function is enabled by setting the control bit, CARDIRE, in the IER register, to 1.

The card detector can support two kinds of card detect switch mechanisms. One is a normally open switch mechanism when the card is not present and the other is a normally closed switch mechanism. After noting which card detect switch mechanism type is used, the card switch selection should be configured by setting the selection bit, DETCNF, in the CR register to correctly detect the card presence. No matter what type of the card switch is selected, by configuring the DETCNF bit, the card Insertion/Removal flag, CPREF, in the SR register will be set to 1 when the card is actually present on the SCI_DET pin. Note that there are no hardware de-bounce circuits in the card detector. Any change of the SCI_DET pin level will cause the CPREF bit to change. The required de-bounce time should be handled by the application program.

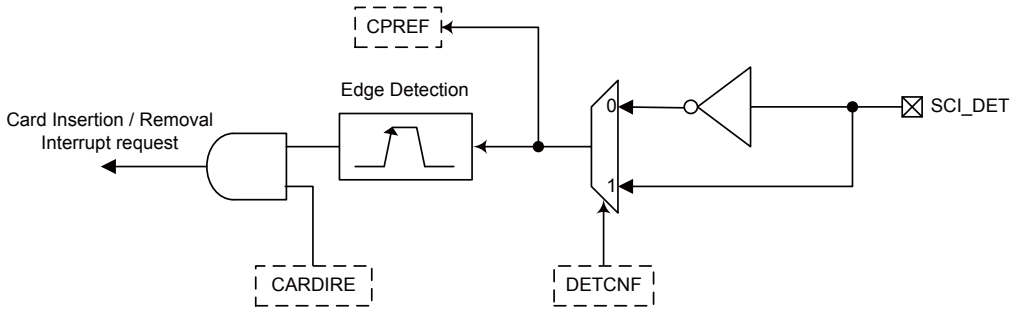


Figure 153. SCI Card Detection Diagram

SCI Data Transfer Mode

The SCI data transfer with the external Smart Card is implemented with two operating modes. One is the SCI mode while the other is the Manual Mode. The data Transfer Mode is selected by the SCI mode selection bit, SCIM, in the CR register. When the SCIM bit is set to 1, the SCI mode is enabled and data will automatically be transferred by the SCI transfer circuitry. Otherwise, data transfer operates in the Manual Mode if the SCIM bit is cleared to 0. The SCI transfer interface is a half-duplex interface and communicates with the external Smart Card via the SCI_CLK and SCI_DIO pins. After a reset condition the SCI transfer interface is in the reception mode but the SCI transfer operation is disabled. When the SCI mode is enabled, data transfer is driven by the SCI transfer circuitry automatically through the SCI_CLK and SCI_DIO pins.

There are two data registers related to data transmission and reception, TXB and RXB, which store the data to be transmitted and received respectively. If a character is written into the TXB register in the SCI Transfer Mode, the SCI transfer interface will automatically switch to the transmission mode from the reception mode after a reset. When the SCI transmission or reception has finished, the corresponding request flag, named TXCF or RXCF, in the SR register is set to 1. If the transmit buffer is empty, the transmit buffer empty flag, TXBEF, in the SR register will be set to 1.

Parity Check Function

The SCI transfer interface supports a parity generator and a parity check function. As the parity error occurs during a data transfer, the corresponding request flag, named PARF in the SR register, will be set to 1. Once the PARF bit is set to 1, the parity error pending flag, PARP, in the IPR register will also be set to 1 if the relevant interrupt control bit, PARE, in the IER register is enabled.

If the data transmitted by the SCI is received by the external Smart Card without a parity error, the SCI transmission request flag, TXCF, will be set to 1 and the SCI parity error request flag, PARF, will be cleared to 0. If the data transmitted by the external Smart Card is received by the SCI without a parity error, the SCI reception request flag, RXCF, will be set to 1 and the parity error flag, PARF, will be cleared to 0.

Repetition Function

There is a Character Repetition function supported by the SCI transfer circuitry when a parity error occurs. The Character Repetition function is enabled by setting the CREP bit in the CR register to 1. A repetition function will then be activated when a parity error occurs during a data transfer. The repetition time number can be selected to be 4 or 5 by configuring the RETRY bit in the CR register.

When the CREP bit is set to 1, the character repetition function will be activated. Taking a 4 time repetition as an example, when the CREP bit is set to 1 and the RETRY bit is set to 1, in the transmission mode, the SCI will repeatedly transmit the data a maximum of 4 times when an error signal occurs. However, if the SCI is informed that there is still an error signal during the 4 transmissions, the parity error flag PARF will be set to 1 after the same data has been transmitted 4 times but the TXCF flag will not be set. At this time the data in the transmit buffer will be loaded into the transmit shift register and the transmit buffer will be empty which will result in the TXBEF flag being set to 1.

Similarly, when the SCI operates in the reception mode, it will inform the external Smart Card that there is a parity error for a maximum of 4 times if the character repetition function is enabled. If the SCI informs the external Smart Card that there is still an error signal for the 4 receptions, the parity error flag, PARF, will be set to 1 together with the reception request flag, RXCF.

If the CREP bit is cleared to 0, the character repetition function will be disabled. When the SCI operates in the reception mode, both the PARF and RXCF bits will be set to 1 as data with a parity error has been received. If the SCI is informed that there is a parity error in the transmission mode, the PARF bit will be set to 1 but the TXCF bit will not be set.

Manual Data Transfer Mode

When the SCIM bit is cleared to 0, data will be transferred in the Manual Mode. In the Manual Mode, the data is controlled by the control bit, CDIO, in the CCR register. The CDIO bit value will be reflected immediately on the SCI_DIO pin in the Manual Mode. Note that in the Manual Mode the character repetition function can not be used as well as the related flags and all the data transfer is handled by the application program. The clock used to drive the external Smart Card that appears on the SCI_CLK pin can be derived from the internal clock source, which is the 6-bit prescaler output, f_{PSC_CK}, or from the control bit, CCLK, in the CCR register. The clock source is selected using the bit, CLKSEL, in the CCR register. When CLKSEL bit is set to 1, the clock used to drive the Smart Card will be sourced from the 6-bit prescaler output, f_{PSC_CK}. If the clock is to be managed manually, the CLKSEL bit should first be cleared to 0 and then the value of the CCLK bit will be present in the SCI_CLK pin.

Data Transfer Direction Convention

If the direction convention used by the Smart Card is the same as the convention used by the SCI, the SCI will generate a reception interrupt if the reception interrupt is enabled without a parity error flag. Otherwise, the SCI will generate a reception interrupt and the parity error flag will be asserted. By checking the parity error flag, the SCI can know if the data direction convention is correct or not.

Interrupt Generator

There are several conditions for the SCI to generate an SCI interrupt. When these conditions are met, an interrupt signal will be generated to obtain the attention of the microcontroller. These conditions are a Smart Card Insertion/Removal, a Waiting Time Counter Underflow, a Parity error, an end of a Character Transmission or Reception and an empty Transmit buffer. When a Smart Card interrupt is generated by any of these conditions, then if the SCI global interrupt in the NVIC and the corresponding SCI interrupt are together enabled, the program will jump to the corresponding interrupt vector where it can be serviced before returning to the main program.

For SCI interrupt events, there are corresponding pending flags which can be masked by the relevant interrupt enable control bit. When the related interrupt enable control is disabled, the corresponding interrupt pending flag will not be affected by the request flag and no interrupt will be generated. If the related interrupt enable control is enabled, the relevant interrupt pending flag will be affected by the request flag and then the interrupt will be generated. The pending flag register, named IPR, is read only and once the pending flag is read by the application program, it will be automatically cleared while the related request flag should be cleared by the application program manually.

For an SCI Interrupt to be serviced, in addition to the bits for the corresponding interrupt enable control in the SCI being set, the SCI global interrupt enable control bit in the NVIC must also be set. If this SCI global interrupt control bit is not set, then no SCI interrupt will be serviced.

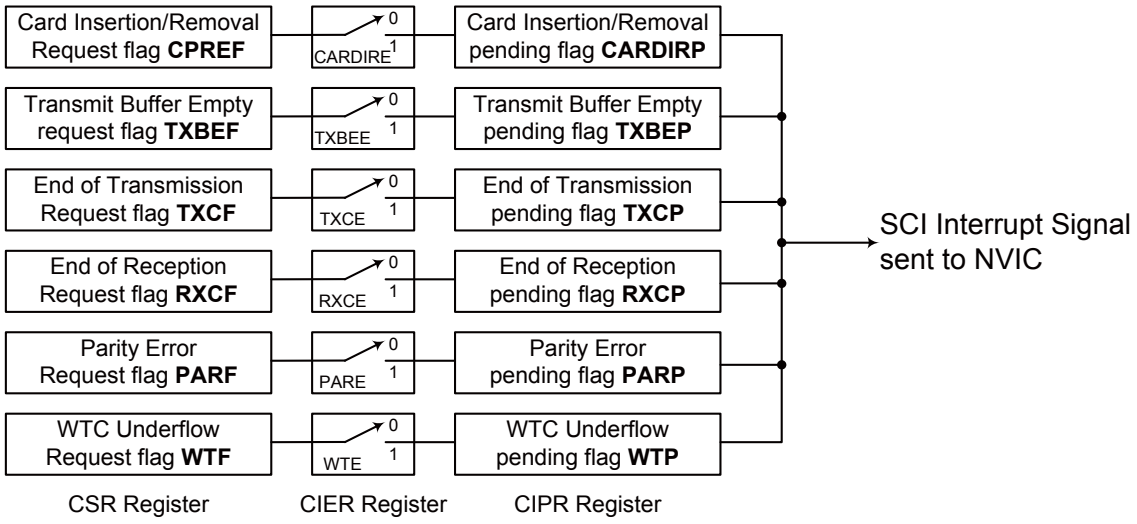


Figure 154. SCI Interrupt Structure

PDMA Interface

The PDMA interface is integrated in the SCI module. The PDMA function can be enabled by setting the TXDMA or RXDMA bit to 1 in the transmitter or receiver mode respectively. When the transmit buffer is empty which results in the transmit buffer empty flag, TXBEF, being asserted and the TXDMA bit is set to 1, the PDMA function will be activated to move data from a certain memory location into the SCI Transmit buffer. Similarly, when the SCI receives a character which results in the character received flag, RXCF, being asserted and the RXDMA bit is set to 1, the PDMA function will be activated to move data from the SCI Receive buffer to a specific memory location.

For a mode detailed descriptions on the PDMA configurations, refer to the PDMA chapter.

Register Map

There are several registers associated with the Smart Card function. Some of these registers control the SCI overall functions as well as the interrupts, while some of the registers contain the status bits which indicate the Smart Card data transfer situation and error conditions. Also there are two registers for the SCI transmission and reception respectively to store the data received from or to be transmitted to the external Smart Card. The following table shows the SCI register list and reset values.

Table 56. SCI Register Map

Register	Offset	Description	Reset Value
SCI Base Address=0x4004_3000			
CR	0x000	SCI Control Register	0x0000_0000
SR	0x004	SCI Status Register	0x0000_0080
CCR	0x008	SCI Contact Control Register	0x0000_0008
ETUR	0x00C	SCI Elementary Time Unit Register	0x0000_0174
GTR	0x010	SCI Guard Time Register	0x0000_000C
WTR	0x014	SCI Waiting Time Register	0x0000_2580
IER	0x018	SCI Interrupt Enable Register	0x0000_0000
IPR	0x01C	SCI Interrupt Pending Register	0x0000_0000
TXB	0x020	SCI Transmit Buffer	0x0000_0000
RXB	0x024	SCI Receive Buffer	0x0000_0000
PSCR	0x028	SCI Prescaler Register	0x0000_0000

Register Descriptions

SCI Control Register – CR

This register contains the SCI control bits.

Offset: 0x000

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved						RXDMA	TXDMA
Type/Reset							RW 0	RW 0
	7	6	5	4	3	2	1	0
	Reserved	DETCNF	ENSCI	RETRY	SCIM	WTEN	CREP	CONV
Type/Reset		RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[9]	RXDMA	SCI reception PDMA request enable 0: SCI reception PDMA request is disabled 1: SCI reception PDMA request is enabled
[8]	TXDMA	SCI transmission PDMA request enable control 0: SCI transmission PDMA request is disabled 1: SCI transmission PDMA request is enabled
[6]	DETCNF	Card switch type selection 0: Switch is normally opened if no card is present 1: Switch is normally closed if no card is present

DETCNT	SCI_DET pin	STATUS
0	1	No card insert
0	0	Card insert
1	1	Card insert
1	0	No card insert

This bit is set and cleared by the application program to configure the card detector switch type.

[5]	ENSCI	SCI finite state machine enable bit 0: SCI FSM is disabled and forced to its initial state 1: SCI FSM is enabled

Bits	Field	Descriptions
[4]	RETRY	Character transfer repetition time selection for a parity error condition 0: Data transfer 5 times when parity error occurs 1: Data transfer 4 times when parity error occurs The bit is available only when the CREP bit is set to 1. When this bit is set to 1, the data will be transmitted or received 4 times once a parity error occurs. If the bit is cleared to 0, the data will be transferred 5 times if a parity error occurs.
[3]	SCIM	SCI Mode Selection 0: SCI data transfer in manual mode 1: SCI data transfer in SCI mode This bit is set and cleared by the application program to select the SCI data Transfer Mode. If it is cleared to 0, the SCI_DIO pin status is the same as the value of the CDIO bit in the CCR register. If it is set to 1, the SCI_DIO pin is driven by the internal SCI control circuitry. Before the data transfer type is switched from the Manual Mode to the SCI Mode, the CDIO bit must be set to 1 to avoid an SCI malfunction.
[2]	WTEN	Waiting Time Counter enable control 0: Waiting Time Counter stops counting 1: Waiting Time Counter starts counting The WTEN bit is set and cleared by the application program. When the WTEN bit is cleared to 0, a write access to the WTR register will load the value into the waiting time counter. If it is set to 1, the waiting time counter is enabled and automatically reloaded with the value at each start bit occurrence.
[1]	CREP	Automatic character repetition enable control for a parity error condition 0: No retry on parity error 1: Automatic retry on parity error The CREP bit is set and cleared by the application program. When the CREP bit is cleared to 0, both the RXCF and PARF flags will be set when a parity error occurs in the reception mode after the data is received. However, in the transmission mode, the PARF flag will be set but the TXCF flag will not be set when a parity error occurs. If the CREP bit is set to 1, a character transfer will automatically be activated 4 or 5 times depending upon the RETRY bit value. In the transmission mode the character will be re-transmitted if the transmitted data has a parity error. Here the parity error flag, PARF, will be set at the end of the 4th or 5th transmission without the TXCF bit being set. In the reception mode if the received data has a parity error, the SCI will inform the external Smart Card for 4 or 5 times and then the PARF and RXCF flags will both be set at the end of the 4th or 5th reception.
[0]	CONV	Data direction convention select 0: LSB is transferred first; a data “1” is a logic high level on the SCI_DIO pin and the parity bit is added after the MSB 1: MSB is transferred first; a data “1” is a logic low level on the SCI_DIO pin and the parity bit is added after the LSB This bit is set and cleared by the application program to select if the data is transmitted LSB or MSB first. When the data direction convention is the same as the data direction specified by the external Smart Card, only the RXCF flag will be set to 1 without a parity error. Otherwise, both the RXCF and PARF flags will be set to 1 after the data is received.

SCI Status Register – SR

This register contains the SCI status bits.

Offset: 0x004

Reset value: 0x0000_0080

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								

	7	6	5	4	3	2	1	0
	TXBEF	CPREF		reserved	WTF	TXCF	RXCF	PARF
Type/Reset	RO 1	RO 0			RO 0	W0C 0	RO 0	W0C 0

Bits	Field	Descriptions
[7]	TXBEF	Transmit Buffer Empty Request Flag 0: Transmit buffer is not empty 1: Transmit buffer is empty This bit is used to indicate if the transmit buffer is empty and is set or cleared by hardware automatically.
[6]	CPREF	Card Presence Request Flag 0: No card is present 1: A card is present This bit is used to indicate if a card is present and is set or cleared by hardware automatically. The card presence detection function is enabled after the ENSCI bit is set.
[3]	WTF	Waiting Time Counter Underflow Request Flag 0: No Waiting Time Counter underflows 1: The Waiting Time Counter underflows This bit is set and cleared by the application program and indicates if the Waiting Time Counter underflows.
[2]	TXCF	Character Transmission Request Flag 0: No character transmitted 1: A character has been transmitted This bit is set by hardware and cleared by writing 0 into it.
[1]	RXCF	Character Received Request Flag 0: No character received 1: A character has been received This bit is set by hardware and cleared after a read access to the RXB register by the application program. The RXCF bit will be set to 1 when a character is received regardless of the result of the parity check. When the character has been received, the received data stored in the RXB register should be moved to the data memory as specified by the application program. If the contents of the RXB register are not read before the end of the next character to be shifted in, the data stored in the RXB register will be overwritten.

Bits	Field	Descriptions
[0]	PARF	Parity Error Request Flag 0: No parity error occurs 1: Parity error has occurred This bit is set by hardware and cleared by writing 0 into it. When a character is received, the parity check circuitry will check that the parity is correct or not. If the result of the parity check is not correct, the parity error request flag, PARF, will be set to 1. Otherwise, the PARF bit will remain zero. In the transmission mode when the SCI is informed that there is a parity error in the transmitted character by the external Smart Card, the PARF bit will also be set to 1.

SCI Contact Control Register – CCR

This register specifies the SCI pin setting and clock selection.

Offset: 0x008

Reset value: 0x0000_0008

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	CLKSEL	Reserved			CDIO	CCLK	Reserved	
Type/Reset	RW 0				RW 1	RW 0		

Bits	Field	Descriptions
[7]	CLKSEL	Card Clock Selection 0: The CCLK bit content is present on the external SCI_CLK pin 1: The clock output on the external SCI_CLK pin is sourced from the f_{PSC_CK} clock This bit is used to select the external SCI_CLK pin clock source. It is set and cleared by the application program. It is recommended that to activate the clock at a known level a certain value should be first programmed into the CCLK bit before the CLKSEL bit is switched from 1 to 0.
[3]	CDIO	SCI_DIO pin control 0: SCI_DIO pin is logic level 0 1: SCI_DIO pin in open-drain condition This bit is available only when the SCIM bit in the CR register is cleared to 0 to configure the SCI to operate in the Manual Transfer Mode. It is set and cleared by application program to control the external SCI_DIO pin status in the Manual Mode. Reading this bit will return the present status of the SCI_DIO pin.
[2]	CCLK	SCI_CLK pin control 0: SCI_CLK pin is logic level 0 1: SCI_CLK pin is logic level 1 This bit is available only when the SCIM bit in the CR register is cleared to 0 to configure the SCI to operate in the Manual Transfer Mode. It is set and cleared by application program to control the external SCI_CLK pin status in the Manual Mode. Reading this bit will return the current value in the register and not the present status of the external SCI_CLK pin. To ensure that the clock remains at a known level a certain value should be first programmed into the CCLK bit before the CLKSEL bit is switched from 1 to 0.

SCI Elementary Time Unit Register – ETUR

The register specifies the value determined by the formula described in the ETU section. It also includes the Compensation function enable control bit for the ETU time granularity.

Offset: 0x00C

Reset value: 0x0000_0174

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	COMP	Reserved				ETU		
Type/Reset	RW 0					RW 0	RW 0	RW 1
	7	6	5	4	3	2	1	0
	ETU							
Type/Reset	RW 0	RW 1	RW 1	RW 1	RW 0	RW 1	RW 0	RW 0

Bits	Field	Descriptions
[15]	COMP	Elementary Time Unit Compensation mode enable control 0: Compensation mode is disabled 1: Compensation mode is enabled This bit is set and cleared by application program and used to control the ETU compensation function. For more details regarding the compensation function consult the Elementary Time Unit section.
[10:0]	ETU	ETU value for a character data bit This field is configured by the application program to modify the ETU time duration. Note that the value of ETU must be in the range of 0x00C to 0x7FF. To obtain the maximum ETU decimal value of 2048, a 0x000 value should be written into this bit field.

SCI Guard Time Register – GTR

This register specifies the guard time value.

Offset: 0x010

Reset value: 0x0000_000C

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							GT
Type/Reset								RW 0
	7	6	5	4	3	2	1	0
	GT							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 1	RW 1	RW 0	RW 0

Bits	Field	Descriptions
[8:0]	GT	Character Guard Time value This field is configured by the application program to modify the guard time duration. The updated GT value will be loaded into the GT counter at the end of the current guard time period. Note that the GT value must be in the range from 0x00C to 0x1FF.

SCI Waiting Time Register – WTR

This register specifies the waiting time value.

Offset: 0x014

Reset value: 0x0000_2580

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	WT							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	WT							
Type/Reset	RW 0	RW 0	RW 1	RW 0	RW 0	RW 1	RW 0	RW 1
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	WT							
Type/Reset	RW 1	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[23:0]	WT	Character Waiting Time value expressed in ETU (0/16777215). This field is configured by the application program to modify the waiting time duration. The reload conditions of the updated waiting time counter value are described in the waiting time counter section. Refer to the waiting time counter section for more details. Note that the WT value can range from 0x00_0000 to 0xFF_FFFF.

SCI Interrupt Enable Register – IER

This register specifies the interrupt enable control bits for all of the interrupt events in the SCI.

Offset: 0x018

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	TXBEE	CARDIRE	Reserved		WTE	TXCE	RXCE	PARE
Type/Reset	RW 0	RW 0			RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[7]	TXBEE	Transmit buffer empty interrupt enable control 0: Disabled 1: Enabled This bit is set and cleared by application program and is used to control the Transmit Buffer Empty interrupt. If this bit is set to 1, the transmit buffer empty interrupt will be generated when the transmit buffer is empty.
[6]	CARDIRE	Card Insertion/Removal interrupt enable control 0: Disabled 1: Enabled This bit is set and cleared by application program and is used to control the card insertion/removal interrupt. If this bit is set to 1, the card insertion/removal interrupt will be generated when the external Smart Card is inserted or removed.
[3]	WTE	Waiting Timer Underflow interrupt enable control 0: Disabled 1: Enabled This bit is set and cleared by the application program and is used to control the Waiting Timer underflow interrupt. If this bit is set to 1, the waiting time counter underflow interrupt will be generated when the waiting time counter underflows.
[2]	TXCE	Character Transmission Completion interrupt enable control 0: Disabled 1: Enabled This bit is set and cleared by the application program and is used to control the Character Transmission Completion interrupt. If this bit is set to1, the Character Transmission Completion interrupt will be generated at the end of the character transmission.

Bits	Field	Descriptions
[1]	RXCE	Character Reception Completion interrupt enable control 0: Disabled 1: Enabled This bit is set and cleared by the application program and is used to control the Character Reception Completion interrupt. If this bit is set to 1, the Character Reception Completion interrupt will be generated at the end of the character reception.
[0]	PARE	Parity Error interrupt enable control 0: Disabled 1: Enabled This bit is set and cleared by the application program and is used to control the parity error interrupt. if this bit is set to 1, the Parity Error interrupt will be generated when a parity error occurs.

SCI Interrupt Pending Register – IPR

This register contains the interrupt pending flags for all of the interrupt events in the SCI. These pending flags can be masked by the corresponding interrupt enable control bits.

Offset: 0x01C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	TXBEP	CARDIRP		Reserved	WTP	TXCP	RXCP	PARP
Type/Reset	RC 0	RC 0			RC 0	RC 0	RC 0	RC 0

Bits	Field	Descriptions
[7]	TXBEP	Transmit Buffer Empty interrupt pending flag 0: No interrupt pending 1: Interrupt pending This bit is set by hardware and cleared by a read access to this register using the application program. This bit is used to indicate if there is a Transmit Buffer Empty interrupt pending or not. If the Transmit Buffer is empty and the corresponding interrupt enable control bit is set to 1, this bit will be set to 1 to indicate that the transmit buffer empty interrupt is pending.
[6]	CARDIRP	Card Insertion/Removal interrupt pending flag 0: No interrupt pending 1: Interrupt pending This bit is set by hardware and cleared by a read access to this register using the application program. It is used to indicate if there is an external Smart Card insertion/removal interrupt pending or not. If an external Smart Card is inserted or removed and the corresponding interrupt enable control bit is set to 1, this bit will be set to 1 to indicate that the Card insertion/removal interrupt is pending.
[3]	WTP	Waiting Timer Underflow interrupt pending flag 0: No interrupt pending 1: Interrupt pending This bit is set by hardware and cleared by a read access to this register using the application program. It is used to indicate if there is a waiting time counter underflow interrupt pending or not. If the waiting time counter underflows and the corresponding interrupt enable control bit is set to 1, this bit will be set to 1 to indicate that the waiting time counter underflow interrupt is pending.
[2]	TXCP	Character Transmission Completion interrupt pending flag 0: No interrupt pending 1: Interrupt pending This bit is set by hardware and cleared by a read access to this register using the application program. It is used to indicate if there is a Character Transmission Completion interrupt pending or not. If a character has been transmitted and the related interrupt enable control bit is set to 1, this bit will be set to 1 to indicate that the character transmission completion interrupt is pending.
[1]	RXCP	Character Reception Completion interrupt pending flag 0: No interrupt pending 1: Interrupt pending This bit is set by hardware and cleared by a read access to this register using the application program. It is used to indicate if there is a Character Reception Completion interrupt pending or not. If a character has been received and the relevant interrupt enable control bit is set to 1, this bit will be set to 1 to indicate that the character reception completion interrupt is pending.
[0]	PARP	Parity Error interrupt pending flag 0: No interrupt pending 1: Interrupt pending This bit is set by hardware and cleared by a read access to this register using the application program. It is used to indicate if there is a Parity Error interrupt pending or not. If the parity error occurs and its interrupt enable control bit is set to 1, this bit will be set to 1 to indicate that the parity error interrupt is pending.

SCI Transmit Buffer – TXB

This register is used to store the SCI data to be transmitted.

Offset: 0x020

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	TB							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[7:0]	TB	SCI data byte to be transmitted

SCI Receive Buffer – RXB

This register is used to store the SCI received data.

Offset: 0x024

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	RB							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[7:0]	RB	SCI Received data byte

SCI Prescaler Register – PSCR

This register specifies the prescaler division ratio which is used the SCI internal clock.

Offset: 0x028

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved		PSC					
Type/Reset			RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[5:0]	PSC	SCI prescaler division ratio 0: $f_{PSC\_CK}=f_{PCLK}$ 1~63: $f_{PSC\_CK} = \frac{f_{PCLK}}{2\times PSC}$

23 USB Device Controller

Introduction

The USB device controller is compliant with the USB 2.0 full-speed specification. There is one control endpoint known as Endpoint 0 and seven configurable endpoints (EP1~EP7). A 1024-byte EP-SRAM is used for the endpoint buffers. Each endpoint buffer size is programmable by corresponding registers, which provides maximum flexibility for various applications. The integrated USB full-speed transceiver helps to minimise the overall system complexity and cost. The USB also contains the suspend and resume features to meet the low-power consumption requirement. The accompanying figure shows the USB block diagram.

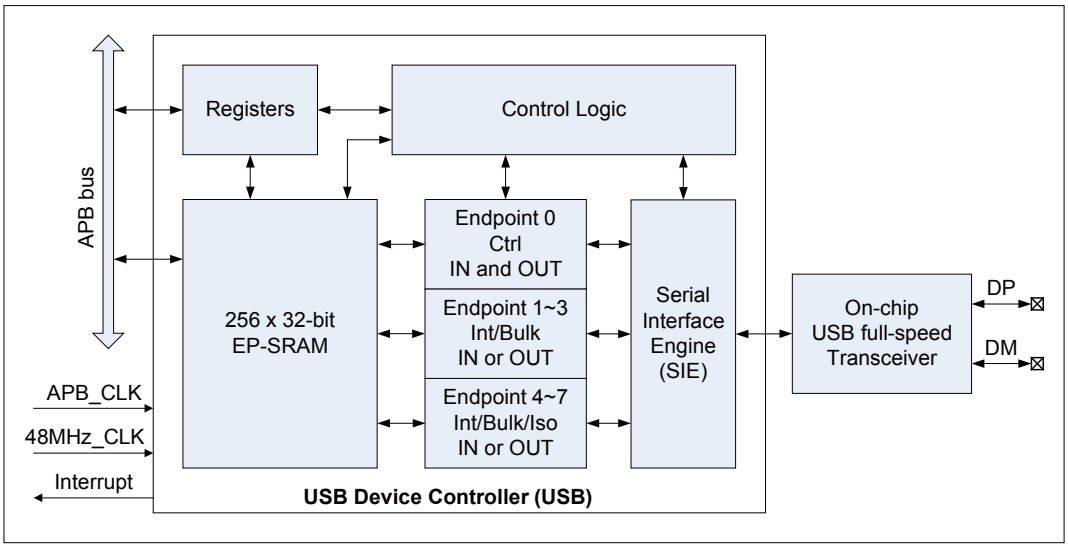


Figure 155. USB Block Diagram

Features

- Complies with USB 2.0 full-speed (12Mbps) device specification
- Fully integrated USB full-speed transceiver
- 1 control endpoint (EP0) for control transfer
- 3 single-buffered endpoints (EP1~EP3) for bulk and interrupt transfer
- 4 double-buffered endpoints (EP4~EP7) for bulk, interrupt and isochronous transfer
- 1,024 bytes EP-SRAM used as endpoint data buffers

Functional Descriptions

Endpoints

The USB Endpoint 0 is the only bidirectional endpoint dedicated to USB control transfer. The device also contains seven unidirectional endpoints for other USB transfer types. There are three endpoints (EP1~EP3) which supports a single buffering function which is used for Bulk and Interrupt IN or OUT data transfer. There are four other endpoints (EP4~EP7) which supports single or double buffering functions for Bulk, Interrupt and Isochronous IN or OUT data transfer. The addresses of the seven unidirectional endpoints (EP1~EP7) can be configured by the application software. The following table lists the endpoint characteristics.

Table 57. Endpoint Characteristics

Endpoint Number	Number Address	Transfer Type	Direction	Buffer Type
0	Fixed	Control	IN and OUT	Single buffering
1~3	Configurable	Interrupt/Bulk	IN or OUT	Single buffering
4~7	Configurable	Interrupt/Bulk/Isochronous	IN or OUT	Single or Double buffering

EP-SRAM

The USB controller contains a dedicated memory space, EP-SRAM, which is used for the USB endpoint buffers. The EP-SRAM, which is connected to the APB bus, can be accessed by the CPU and the PDMA. The EP-SRAM base address is 0x4004_E400 with an offset which ranges from 0x000 to 0x3FF. The EP-SRAM first two words are reserved for Endpoint 0 to temporarily store the 8-byte SETUP data. Therefore the valid start address of the endpoint buffer should start from 0x008 and align to a 4-byte boundary. Each endpoint buffer size is programmable. The following table lists the maximum USB endpoint buffer size which is compliant with USB 2.0 full-speed device specification.

Table 58. USB Data Types and Buffer Size

Transfer Type	Direction	Supported Buffer Size	Bandwidth	CRC	Retrying
Control	Bidirectional	8, 16, 32, 64	Not guaranteed	Yes	Automatic
Bulk	Unidirectional	8, 16, 32, 64	Not guaranteed	Yes	Yes
Interrupt	Unidirectional	≤64	Not guaranteed	Yes	Yes
Isochronous	Unidirectional	<512	Guaranteed	Yes	No

In the following endpoint buffer allocation example, the Endpoint “4” is configured as a double-buffered Bulk IN endpoint while the Endpoint “5” is configured as a double-buffered Bulk OUT endpoint. Each endpoint buffer size is set to 64 bytes.

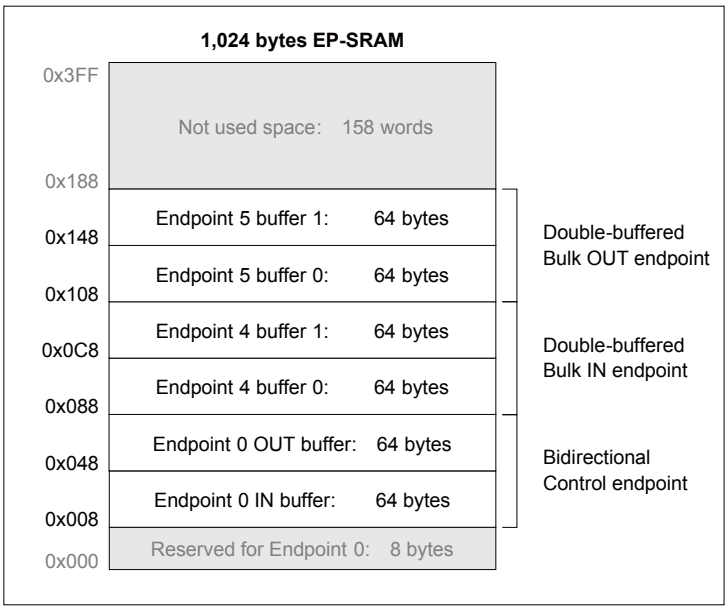


Figure 156. Endpoint Buffer Allocation Example

Serial Interface Engine – SIE

The Serial Interface Engine, SIE, which is connected to the USB full-speed transceiver and internal USB control circuitry provides a temporal buffer for the transmitted and received data. The SIE also decodes the SE0 signal, SE1 signal, J-state, K-state, USB RESET event and End of Packet event signals, EOP, when the USB module receives data, transmits data or transmits the resume signal for remote control. The SIE detects the number of SOF packets and generates the SOF interrupt signal to the USB control circuitry which includes data format conversion from parallel to serial or serial to parallel. It also includes, CRC checking and generation, PID decoder, bit-stuffing and debit-stuffing functions.

Double-Buffering

The Double buffering function is recommended to be enabled when the corresponding endpoint is specified to be used for Isochronous transfer or high throughput Bulk transfer. The double buffering function stores the preceding data packet sent by the USB host in a single buffer for the MCU to process and the hardware will ensure that it continues to receive the current data packet in the other buffer during a OUT transaction ,and vice versa. Using a double buffering function can achieve the highest possible data transfer rate. The details regarding double buffering usage is provided in the corresponding UDBTG and MDBTG control bit description in the USBEPnCSR register where the denotation n ranges from 4 to 7.

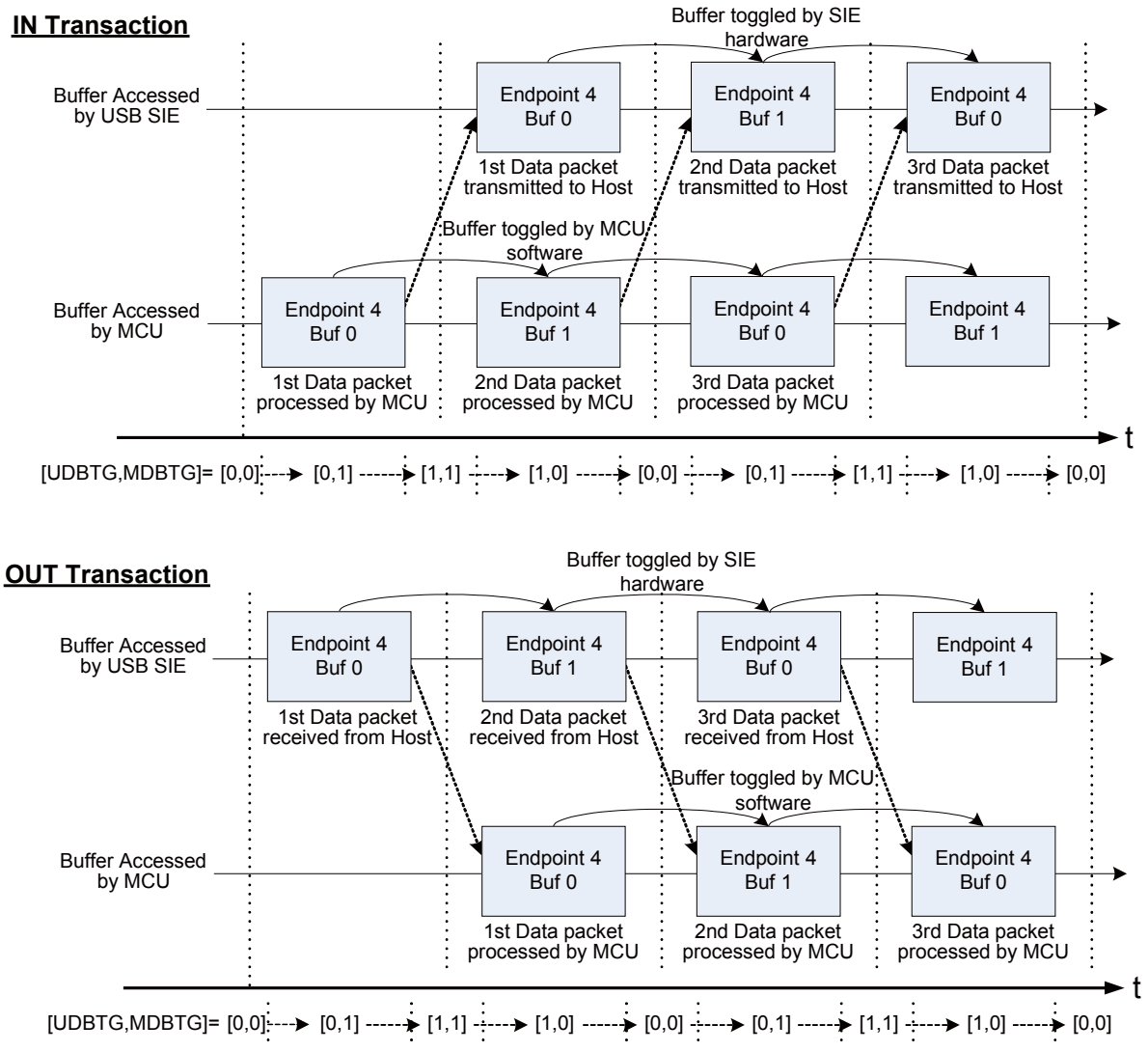


Figure 157. Double-buffering Operation Example

Suspend Mode and Wake-Up

According to USB specifications, the device must enter the suspend mode after a 3ms bus idle time. When the USB device enters the suspend mode, the suspend mode current drawn from the USB bus must not be greater than 500μA to meet the specification suspend mode current requirements. The USB control circuitry will generate a suspend interrupt if the bus is in the idle state for 3ms. Here the software should set the LPMODE and PDWN bits in the USBCSR register to 1. The LPMODE bit is used to determine whether the USB controller enters the low power mode or not by holding the USB bus in a reset condition while the PDWN bit is used to determine if the integrated USB full-speed transceiver is turned off or not.

There are two ways for the USB host to wake up the USB device, one is to send a USB reset signal, SE0, and the other is to send a USB resume signal known as the K-state. After a wake-up signal, regardless of whether a SE0 signal or a K-state, is detected, the USB device will be woken up and will generate a resume interrupt if the resume interrupt is enabled by setting the RSMIE bit to 1.

Remote Wake-Up

As the USB device has a remote wake-up function, it can wake up the USB host by sending a resume request signal by setting the GENRSM bit in the USBCSR register to 1. Once the USB host receives the remote wake-up signal from the USB device, it will send a resume signal to the USB device.

Register Map

The following table shows the USB registers and reset values.

Table 59. USB Register Map

Register	Offset	Description	Reset Value
USB Base Address=0x4004_E000			
USBCSR	0x000	USB Control and Status Register	0x0000_00X6
USBIER	0x004	USB Interrupt Enable Register	0x0000_0000
USBISR	0x008	USB Interrupt Status Register	0x0000_0000
USBFCR	0x00C	USB Frame Count Register	0x0000_0000
USBDEVAR	0x010	USB Device Address Register	0x0000_0000
USBEP0CSR	0x014	USB Endpoint 0 Control and Status Register	0x0000_0002
USBEP0IER	0x018	USB Endpoint 0 Interrupt Enable Register	0x0000_0000
USBEP0ISR	0x01C	USB Endpoint 0 Interrupt Status Register	0x0000_0000
USBEP0TCR	0x020	USB Endpoint 0 Transfer Count Register	0x0000_0000
USBEP0CFGR	0x024	USB Endpoint 0 Configuration Register	0x8000_0002
USBEP1CSR	0x028	USB Endpoint 1 Control and Status Register	0x0000_0002
USBEP1IER	0x02C	USB Endpoint 1 Interrupt Enable Register	0x0000_0000
USBEP1ISR	0x030	USB Endpoint 1 Interrupt Status Register	0x0000_0000
USBEP1TCR	0x034	USB Endpoint 1 Transfer Count Register	0x0000_0000
USBEP1CFGR	0x038	USB Endpoint 1 Configuration Register	0x1000_03FF
USBEP2CSR	0x03C	USB Endpoint 2 Control and Status Register	0x0000_0002
USBEP2IER	0x040	USB Endpoint 2 Interrupt Enable Register	0x0000_0000
USBEP2ISR	0x044	USB Endpoint 2 Interrupt Status Register	0x0000_0000

Register	Offset	Description	Reset Value
USBEP2TCR	0x048	USB Endpoint 2 Transfer Count Register	0x0000_0000
USBEP2CFGR	0x04C	USB Endpoint 2 Configuration Register	0x1000_03FF
USBEP3CSR	0x050	USB Endpoint 3 Control and Status Register	0x0000_0002
USBEP3IER	0x054	USB Endpoint 3 Interrupt Enable Register	0x0000_0000
USBEP3ISR	0x058	USB Endpoint 3 Interrupt Status Register	0x0000_0000
USBEP3TCR	0x05C	USB Endpoint 3 Transfer Count Register	0x0000_0000
USBEP3CFGR	0x060	USB Endpoint 3 Configuration Register	0x1000_03FF
USBEP4CSR	0x064	USB Endpoint 4 Control and Status Register	0x0000_0002
USBEP4IER	0x068	USB Endpoint 4 Interrupt Enable Register	0x0000_0000
USBEP4ISR	0x06C	USB Endpoint 4 Interrupt Status Register	0x0000_0000
USBEP4TCR	0x070	USB Endpoint 4 Transfer Count Register	0x0000_0000
USBEP4CFGR	0x074	USB Endpoint 4 Configuration Register	0x1000_03FF
USBEP5CSR	0x078	USB Endpoint 5 Control and Status Register	0x0000_0002
USBEP5IER	0x07C	USB Endpoint 5 Interrupt Enable Register	0x0000_0000
USBEP5ISR	0x080	USB Endpoint 5 Interrupt Status Register	0x0000_0000
USBEP5TCR	0x084	USB Endpoint 5 Transfer Count Register	0x0000_0000
USBEP5CFGR	0x088	USB Endpoint 5 Configuration Register	0x1000_03FF
USBEP6CSR	0x08C	USB Endpoint 6 Control and Status Register	0x0000_0002
USBEP6IER	0x090	USB Endpoint 6 Interrupt Enable Register	0x0000_0000
USBEP6ISR	0x094	USB Endpoint 6 Interrupt Status Register	0x0000_0000
USBEP6TCR	0x098	USB Endpoint 6 Transfer Count Register	0x0000_0000
USBEP6CFGR	0x09C	USB Endpoint 6 Configuration Register	0x1000_03FF
USBEP7CSR	0x0A0	USB Endpoint 7 Control and Status Register	0x0000_0002
USBEP7IER	0x0A4	USB Endpoint 7 Interrupt Enable Register	0x0000_0000
USBEP7ISR	0x0A8	USB Endpoint 7 Interrupt Status Register	0x0000_0000
USBEP7TCR	0x0AC	USB Endpoint 7 Transfer Count Register	0x0000_0000
USBEP7CFGR	0x0B0	USB Endpoint 7 Configuration Register	0x1000_03FF

Register Descriptions

USB Control and Status Register – USBCSR

This register specifies the USB control bits and USB data line status.

Offset: 0x000

Reset value: 0x0000_00X6

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							ADRSET
Type/Reset								RW 0
	7	6	5	4	3	2	1	0
	RXDM	RXDP	GENRSM	Reserved	LPMODE	PDWN	FRES	Reserved
Type/Reset	RO X	RO X	RW 0		RW 0	RW 1	RW 1	

Bits	Field	Descriptions
[8]	ADRSET	Device Address Setting Control This bit is used to determine when the USB SIE updates the device address with the value of the USBDEVA register. 0: The SIE updates the device address immediately after an address is written into the UDEVA register 1: The SIE updates the device address after the USB Host has successfully read the data from the device by the IN operation. This bit is cleared by the SIE after the device address is updated
[7]	RXDM	Received DM Line Status This bit is used to observe the DM data line status at the end of the suspend routines to determine whether a wakeup event has occurred.
[6]	RXDP	Received DP Line Status This bit is used to observe the DP data line status during at end of the suspend routines to determine whether a wakeup event has occurred.
[5]	GENRSM	Resume Request Generation Control This bit is used to generate a resume request which is sent to the USB host by writing 1 into this bit location. The USB remote wakeup function is always enabled. This bit will be cleared to 0 after a resume signal, sent by the USB host, has been received.
[3]	LPMODE	Low-power Mode Control This bit is used to determine the USB operating mode. Setting this bit will force the USB to enter the low-power mode. When USB bus traffic, known as a wakeup event, is detected by the hardware, this bit should be cleared by software. 0: Exit the Low-power mode 1: Enter the Low-power mode

Bits	Field	Descriptions
[2]	PDWN	Power Down Mode Control This bit is used to switch off the USB bus function. Setting this bit will power down the full-speed USB transceiver. This will disconnect the USB transceiver from the USB bus. 0: Exit the Power-Down mode 1: Enter the Power-Down mode
[1]	FRES	Force USB Reset Control This bit is used to reset the USB circuitry. Setting this bit will force the USB into a reset state until the software clears it. A USB reset interrupt will be generated if the corresponding interrupt enable bit in the USBIER register is set to 1. All related USB registers are reset to their default values. 0: Release USB reset 1: Force USB reset

Table 60. Resume Event Detection

[RXDP, RXDM] Status	Wakeup Event	Required Resume Software Action
00	Root reset	None
10	None (noise on bus)	Go back to suspend mode
01	Root resume	None
11	Not allowed (noise on bus)	Go back to suspend mode

USB Interrupt Enable Register – USBIER

This register specifies the USB interrupt enable control.

Offset: 0x004

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	EP7IE	EP6IE	EP5IE	EP4IE	EP3IE	EP2IE	EP1IE	EP0IE
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	Reserved		ESOFIE	SUSPIE	RSMIE	URSTIE	SOFIE	UGIE
Type/Reset			RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:8]	EPnIE	Endpoint n Interrupt Enable Control (n = 7~0) 0: Disable interrupt 1: Enable interrupt
[5]	ESOFIE	Expected Start Of Frame (ESOF) Interrupt Enable Control 0: Disable ESOF interrupt 1: Enable ESOF interrupt
[4]	SUSPIE	Suspend Interrupt Enable Control 0: Disable Suspend interrupt 1: Enable Suspend interrupt
[3]	RSMIE	Resume Interrupt Enable Control 0: Disable Resume interrupt 1: Enable Resume interrupt
[2]	URSTIE	USB Reset Interrupt Enable Control 0: Disable USB Reset interrupt 1: Enable USB Reset interrupt
[1]	SOFIE	Start Of Frame (SOF) Interrupt Enable Control 0: Disable SOF interrupt 1: Enable SOF interrupt
[0]	UGIE	USB Global Interrupt Enable Control 0: USB Global interrupt is disabled 1: USB Global interrupt Is enabled This bit must be set to 1 to enable the corresponding USB interrupt function. If this bit is cleared to 0, the relevant USB interrups will not be generated, however, the corresponding interrupt flags will still be asserted.

USB Interrupt Status Register – USBISR

This register specifies the USB interrupt status.

Offset: 0x008

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	EP7IF	EP6IF	EP5IF	EP4IF	EP3IF	EP2IF	EP1IF	EP0IF
Type/Reset	WC 0	WC 0	WC 0	WC 0	WC 0	WC 0	WC 0	WC 0
	7	6	5	4	3	2	1	0
	Reserved		ESOFIF	SUSPIF	RSMIF	URSTIF	SOFIF	Reserved
Type/Reset			RW 0	WC 0	WC 0	WC 0	WC 0	

Bits	Field	Descriptions
[15:8]	EPnIF	Endpoint n Interrupt Flag (n = 7~0) This bit is set by the hardware to indicate the generation of the relevant endpoint interrupt. Writing 1 into this bit will clear it. It is important to note that the interrupt flag can only be cleared when the endpoint interrupt status bit in the USBEPnISR register is equal to 0.
[5]	ESOFIF	Expected Start Of Frame Interrupt Flag This bit is set by the hardware when an SOF packet is expected to be received. The USB host sends an SOF (Start Of Frame) packet each millisecond. If the USB device hardware does not receive it properly, an ESOF interrupt will be generated when the ESOFIE bit in the USBIER register is set to 1. If three consecutive ESOF interrupts are generated, which means that the SOF packet has been missed 3 times, the SUSPIF bit will be set to 1. This bit will be set to 1 when the missing SOF packets occur if the timer is not yet locked. This bit can be read or written. However, only 0 can be written into this bit. Writing 1 has no effect.
[4]	SUSPIF	Suspend Interrupt Flag This bit is set by the hardware when no data transfer has occurred for 3ms, indicating that a suspend request has been sent from the USB host. The suspend condition check is enabled immediately after a USB reset. This bit is cleared to 0 by writing 1.
[3]	RSMIF	Resume Interrupt Flag This bit is set by the hardware. When this bit is set to 1, this means that a device resume has occurred. This bit is cleared to 0 by writing 1.

Bits	Field	Descriptions
[2]	URSTIF	USB Reset Interrupt Flag This bit is set by the hardware when a USB reset has been detected. When a USB reset occurs, the internal protocol state machine will be reset and an USB reset interrupt will be generated if the URSTIE bit in the USBIER register is set to 1. Data reception and transmission are disabled until the URSTIF bit is cleared to 0. The USB configuration related registers (USBCSR, USBIER, USBISR, USBFCR and USBDEVAR) will not be reset by a USB reset event except for the USB device address (USBDEVAR), this is to ensure that a USB reset interrupt can be safely executed and any data transactions immediately followed by the USB reset can be completely accessed by the software. Therefore the microcontroller must properly reset these registers. The USB endpoint related registers (USBEPnCSR, USBEPnISR and USBEPnTCR) are also reset by a USB reset event, however, the endpoint configuration (USBEPnCFGR) and interrupt enable (USBEPnIER) registers are not affected by the USB reset event and will remain unchanged. This bit is cleared to 0 by writing 1.
[1]	SOFIF	Start of Frame (SOF) Interrupt Flag This bit is set by the hardware when a start-of-frame packet has been received. Writing 1 into this bit will clear it to 0.

USB Frame Count Register – USBFCR

This register specifies the lost Start-of-Frame number and the USB frame count.

Offset: 0x00C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved					LSOF		SOFLCK
Type/Reset						RO 0	RO 0	RO 0
	15	14	13	12	11	10	9	8
	Reserved					FRNUM		
Type/Reset						RO 0	RO 0	RO 0
	7	6	5	4	3	2	1	0
	FRNUM							
Type/Reset	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0

Bits	Field	Descriptions
[18:17]	LSOF	Lost Start-of-Frame number These bits are written and incremented by 1 by the hardware each time the ESOFIF bit is set. It is used to count the number of lost SOF packets. When a SOF packet has been received, these bits are cleared.
[16]	SOFLCK	Start-of-Frame Lock Flag This bit is set by the hardware when a SOF packet has been received before the frame timer times out. Once this flag is set to 1, the frame number which is sent from the USB host will be loaded into the Frame Number field in the USBFCR register. If there no SOF packet has been received during the 1ms frame time duration, this bit will be cleared to 0.
[10:0]	FRNUM	Frame Number This field stores the frame number received from the USB host.

USB Device Address Register – USBDEVA

This register specifies the USB device address.

Offset: 0x010

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved	DEVA						
Type/Reset		RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[6:0]	DEVA	Device Address This field is used to specify the USB device address. This field is cleared when a USB reset event occurs.

USB Endpoint 0 Control and Status Register – USBEP0CSR

This register specifies the Endpoint 0 control and status bits.

Offset: 0x014

Reset value: 0x0000_0002

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved		STLRX	NAKRX	DTGRX	STLTX	NAKTX	DTGTX
Type/Reset			RW 0	RW 0	RW 0	RW 0	RW 1	RW 0

Bits	Field	Descriptions
[5]	STLRX	STALL Status for reception (OUT) transfer This bit is set to 1 by the application software and then returns a STALL signal in the handshake phase of an OUT transaction if a functional error is detected. This means that a control request delivered from the USB host is not supported by the USB device. The STALL status is cleared by the hardware circuitry when a SETUP token is received. This bit can be read and written and can only be toggled by writing 1.
[4]	NAKRX	NAK Status for reception (OUT) transfer This bit is toggled from 0 to 1 by the hardware circuitry, which will result in a NAK signal in the handshake phase of an OUT transaction after an ACK signal has been transmitted. This means that the USB device will be temporarily unable to accept data from the USB host. Therefore, more time will be required for the received data to be properly processed. This bit can be read and written and can only be toggled by writing 1.
[3]	DTGRX	Data Toggle Status for reception (OUT) transfer This bit contains the expected value of the data toggle bit (0=DATA0, 1=DATA1) for the next data packet to be received. When the current valid data packet is received and the corresponding ACK signal is sent to the USB host by the USB device, the hardware circuitry will toggle this bit and the device will be ready to receive the next data packet. For Endpoint 0, the hardware circuitry will toggle this bit to 1 after the SETUP token is received as Endpoint is addressed. This bit can also be toggled by the software to initialise its value for certain applications. This bit can be read and written and can only be toggled by writing 1.
[2]	STLTX	STALL Status for transmission (IN) transfer This bit is set to 1 by the application software and then returns a STALL signal in response to an IN token if a functional error is detected. This means that the USB device is unable to transmit data. The STALL status is cleared by the hardware circuitry when a SETUP token is received. This bit can be read and written and can only be toggled by writing 1.

Bits	Field	Descriptions
[1]	NAKTX	NAK Status for transmission (IN) transfer This bit is toggled from 0 to 1 by the hardware circuitry, which will result in a NAK signal in the handshake phase of an IN transaction after an ACK signal has been received. It indicates that the USB device is temporarily unable to transmit data to the USB host. Therefore, there will be more time for the application software to properly prepare the data to be transmitted. This bit can be read and written and can only be toggled by writing 1.
[0]	DTGTX	Data Toggle Status for transmission (IN) transfer This bit contains the required value of the data toggle bit (0=DATA0, 1=DATA1) for the next data packet to be transmitted. When the current data packet is transmitted by the USB device and the corresponding ACK signal sent by the USB host is received, the hardware circuitry will toggle this bit and the next data packet will be transmitted. For Endpoint 0, the hardware circuitry will toggle this bit to 1 after the SETUP token is received as Endpoint 0 is addressed. This bit can also be toggled by the software to initialise its value for certain applications. This bit can be read and written and can only be toggled by writing 1.

USB Endpoint 0 Interrupt Enable Register – USBEP0IER

This register specifies the Endpoint 0 interrupt enable control bits.

Offset: 0x018

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved				ZLRXIE	SDERIE	SDRXIE	STRXIE
Type/Reset					RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	UERIE	STLIE	NAKIE	IDTXIE	ITRXIE	ODOVIE	ODRXIE	OTRXIE
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[11]	ZLRXIE	Zero Length Data Received Interrupt Enable Control 0: Disable interrupt 1: Enable interrupt
[10]	SDERIE	SETUP Data Error Interrupt Enable Control 0: Disable interrupt 1: Enable interrupt
[9]	SDRXIE	SETUP Data Received Interrupt Enable Control 0: Disable interrupt 1: Enable interrupt
[8]	STRXIE	SETUP Token Received Interrupt Enable Control 0: Disable interrupt 1: Enable interrupt
[7]	UERIE	USB Error Interrupt Enable Control 0: Disable interrupt 1: Enable interrupt
[6]	STLIE	STALL Transmitted Interrupt Enable Control 0: Disable interrupt 1: Enable interrupt
[5]	NAKIE	NAK Transmitted Interrupt Enable Control 0: Disable interrupt 1: Enable interrupt
[4]	IDTXIE	IN Data Transmitted Interrupt Enable Control 0: Disable interrupt 1: Enable interrupt
[3]	ITRXIE	IN Token Received Interrupt Enable Control 0: Disable interrupt 1: Enable interrupt

Bits	Field	Descriptions
[2]	ODOVIE	OUT Data Buffer Overrun Interrupt Enable Control 0: Disable interrupt 1: Enable interrupt
[1]	ODRXIE	OUT Data Received Interrupt Enable Control 0: Disable interrupt 1: Enable interrupt
[0]	OTRXIE	OUT Token Received Interrupt Enable Control 0: Disable interrupt 1: Enable interrupt

USB Endpoint 0 Interrupt Status Register – USBEP0ISR

This register specifies the Endpoint 0 interrupt status.

Offset: 0x01C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved				ZLRXIF	SDERIF	SDRXIF	STRXIF
Type/Reset					WC 0	WC 0	WC 0	WC 0
	7	6	5	4	3	2	1	0
	UERIF	STLIF	NAKIF	IDTXIF	ITRXIF	ODOVIF	ODRXIF	OTRXIF
Type/Reset	WC 0	WC 0	WC 0	WC 0	WC 0	WC 0	WC 0	WC 0

Bits	Field	Descriptions
[11]	ZLRXIF	Zero Length Data Received Interrupt Flag This bit is set by the hardware when a zero length data packet is received. This bit is cleared by the hardware when a SETUP Token is received or by writing 1.
[10]	SDERIF	SETUP Data Error Interrupt Flag This bit is set by the hardware when the SETUP data packet length is not 8 bytes. This bit is cleared by the hardware when a SETUP Token is received or by writing 1.
[9]	SDRXIF	SETUP Data Received Interrupt Flag This bit is set by the hardware when a SETUP data packet from the USB host has been received. This bit is cleared by the hardware when a SETUP Token is received or by writing 1. If the received SETUP data is not accessed by the application software before the next SETUP packet is received, the SETUP data buffer will be overwritten.
[8]	STRXIF	SETUP Token Received Interrupt Flag This bit is set by the hardware when a SETUP token is received and is cleared by writing 1.
[7]	UERIF	USB Error Interrupt Flag This bit is set by the hardware when an error occurs during the Endpoint 0 transaction. This bit is cleared by the hardware when a SETUP Token is received or by writing 1.
[6]	STLIF	STALL Transmitted Interrupt Flag This bit is set by the hardware when a STALL signal is sent in response to an IN or OUT transaction. This bit is cleared by the hardware when a SETUP Token is received or by writing 1.
[5]	NAKIF	NAK Transmitted Interrupt Flag This bit is set by the hardware when a NAK signal is sent in response to an IN or OUT transaction. This bit is cleared by the hardware when a SETUP Token is received or by writing 1.

Bits	Field	Descriptions
[4]	IDTXIF	IN Data Transmitted Interrupt Flag This bit is set by the hardware when a data packet is transmitted to and then an ACK signal is received from the USB host. This bit is cleared by the hardware when a SETUP Token is received or by writing 1.
[3]	ITRXIF	IN Token Received Interrupt Flag This bit is set by the hardware when the IN token is received from the USB host. This bit is cleared by the hardware when a SETUP Token is received or by writing 1.
[2]	ODOVIF	OUT Data Buffer Overrun Interrupt Flag This bit is set by the hardware when the number of received data bytes is larger than the endpoint buffer size. This bit is cleared by the hardware when a SETUP Token is received or by writing 1.
[1]	ODRXIF	OUT Data Received Interrupt Flag This bit is set by the hardware when a data packet is successfully received from and then an ACK signal is sent to the USB host. This bit is cleared by the hardware when a SETUP Token is received or by writing 1.
[0]	OTRXIF	OUT Token Received Interrupt Flag This bit is set by the hardware when the OUT token is received from the USB host. This bit is cleared by the hardware when a SETUP Token is received or by writing 1.

USB Endpoint 0 Transfer Count Register – USBEP0TCR

This register specifies the Endpoint 0 data transfer byte count.

Offset: 0x020

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved	RXCNT						
Type/Reset		RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved	TXCNT						
Type/Reset		RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[22:16]	RXCNT	Reception Byte Count The bit field contains the number of data bytes received by Endpoint 0 in the preceding SETUP transaction.
[6:0]	TXCNT	Transmission Byte Count The bit field contains the number of data bytes to be transmitted by Endpoint 0 in the next IN token. If the value of this field is zero, it indicates that a zero length packet will be sent.

USB Endpoint 0 Configuration Register – USBEP0CFGR

This register specifies the Endpoint 0 configurations.

Offset: 0x024

Reset value: 0x8000_0002

	31	30	29	28	27	26	25	24
	EPEN	Reserved			EPADR			
Type/Reset	RO 1				RO 0	RO 0	RO 0	RO 0
	23	22	21	20	19	18	17	16
	Reserved							EPLEN
Type/Reset								RW 0
	15	14	13	12	11	10	9	8
	EPLEN						EPBUFA	
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	EPBUFA							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[31]	EPEN	Endpoint Enable Control This bit is always set to 1 by the hardware circuitry to always enable Endpoint 0.
[27:24]	EPADR	Endpoint Address This field is always set to 0 by the hardware circuitry.
[16:10]	EPLEN	Endpoint Buffer Length This field is used to specify the control transfer packet size which can be 8, 16, 32 or 64 bytes as defined in the USB full-speed standard specification.
[9:0]	EPBUFA	Endpoint Buffer Start Address This field is used to specify the start address of the Endpoint 0 buffer allocated in the EP-SRAM. It starts from 0x008 and should be aligned to a 4-byte boundary. Start address of Endpoint 0 IN buffer=EPBUFA Start address of Endpoint 0 OUT buffer=EPBUFA + EPLEN

USB Endpoint 1~3 Control and Status Register – USBEPnCSR, n=1~3

This register specifies the Endpoint 1~3 control and status bits.

Offset: 0x028 (n=1), 0x03C (n=2), 0x050 (n=3)

Reset value: 0x0000_0002

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved		STLRX	NAKRX	DTGRX	STLTX	NAKTX	DTGTX
Type/Reset			RW 0	RW 0	RW 0	RW 0	RW 1	RW 0

Bits	Field	Descriptions
[5]	STLRX	STALL bit for reception transfers This bit is set to 1 by the application software if a functional error has been detected. This bit can be read and written and can only be toggled by writing 1. It can also be toggled by the software to initialise the value under certain conditions.
[4]	NAKRX	NAK bit for reception transfers This bit is toggled from 0 to 1 by the hardware circuitry, which will result in a NAK signal, when a data packet has been received and an ACK signal has been transmitted to the host in the handshake phase of an OUT transaction. It means that the USB device will be temporarily unable to accept data from the USB host until the received data is properly processed. This bit can be read and written and can be only toggled by writing 1.
[3]	DTGRX	Data Toggle bit for reception transfers This bit contains the expected value of the data toggle bit (0=DATA0, 1=DATA1) for the next data packet to be received. When the current valid data packet is received and the corresponding ACK signal is sent to the USB host by the USB device, the hardware circuitry will toggle this bit and the device will be ready to receive the next data packet. This bit can be read and written and can only be toggled by writing 1. This bit can also be toggled by the software to initialise its value under certain conditions.
[2]	STLTX	STALL bit for transmission transfers This bit is set to 1 by the application software if a functional error has been detected. This bit can be read and written and can be only toggled by writing 1. It can also be toggled by the software to initialise its value under certain conditions.
[1]	NAKTX	NAK bit for transmission transfers This bit is toggled from 0 to 1 by the hardware circuitry, which will result in a NAK signal, when a data packet has been transmitted and an ACK signal sent from the host has been received in the handshake phase of an IN transaction. It means that the USB device will be temporarily unable to transmit data packet until the data to be transmitted is appropriately prepared by the application software. This bit can be read and written and can be only toggled by writing 1.

Bits	Field	Descriptions
[0]	DTGTX	Data Toggle bit for transmission transfers This bit contains the required value of the data toggle bit (0=DATA0, 1=DATA1) for the next data packet to be transmitted. When the current data packet is transmitted by the USB device and the corresponding ACK signal sent from the USB host is received, the hardware circuitry will toggle this bit and then the next data packet will be transmitted. This bit can be read and written and can only be toggled by writing 1. It can also be toggled by the software to initialise its value under certain conditions.

USB Endpoint 1~3 Interrupt Enable Register – USBEPnIER, n=1~3

This register specifies the Endpoint 1~3 interrupt enable control bits.

Offset: 0x02C (n=1), 0x040 (n=2), 0x054 (n=3)

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	UERIE	STLIE	NAKIE	IDTXIE	ITRXIE	ODOVIE	ODRXIE	OTRXIE
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[7]	UERIE	USB Error Interrupt Enable Control 0: Disable interrupt 1: Enable interrupt
[6]	STLIE	STALL Transmitted Interrupt Enable Control 0: Disable interrupt 1: Enable interrupt
[5]	NAKIE	NAK Transmitted Interrupt Enable Control 0: Disable interrupt 1: Enable interrupt
[4]	IDTXIE	IN Data Transmitted Interrupt Enable Control 0: Disable interrupt 1: Enable interrupt
[3]	ITRXIE	IN Token Received Interrupt Enable Control 0: Disable interrupt 1: Enable interrupt
[2]	ODOVIE	OUT Data Buffer Overrun Interrupt Enable Control 0: Disable interrupt 1: Enable interrupt
[1]	ODRXIE	OUT Data Received Interrupt Enable Control 0: Disable interrupt 1: Enable interrupt
[0]	OTRXIE	OUT Token Received Interrupt Enable Control 0: Disable interrupt 1: Enable interrupt

USB Endpoint 1~3 Interrupt Status Register – USBEPnISR, n=1~3

This register specifies the Endpoint 1~3 interrupt status.

Offset: 0x030 (n=1), 0x044 (n=2), 0x058 (n=3)

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	UERIF	STLIF	NAKIF	IDTXIF	ITRXIF	ODOVIF	ODRXIF	OTRXIF
Type/Reset	WC 0	WC 0	WC 0	WC 0	WC 0	WC 0	WC 0	WC 0

Bits	Field	Descriptions
[7]	UERIF	USB Error Interrupt Flag This bit is set by the hardware when an error occurs during the transaction. Writing 1 into this status bit will clear it to 0.
[6]	STLIF	STALL Transmitted Interrupt Flag This bit is set by hardware circuitry when a STALL-token is sent in response to an IN or OUT token and is cleared to 0 by writing 1 into it.
[5]	NAKIF	NAK Transmitted Interrupt Flag This bit is set by the hardware circuitry when a NAK-token is sent in response to an IN or OUT token and is cleared to 0 by writing 1.
[4]	IDTXIF	IN Data Transmitted Interrupt Flag This bit is set by the hardware circuitry when a data packet is successfully transmitted to the host in response to an IN-token and an ACK-token is received. Writing 1 into this status bit will clear it to 0.
[3]	ITRXIF	IN Token Received Interrupt Flag This bit is set by the hardware circuitry when the endpoint receives an IN token from the host and is cleared to 0 by writing 1.
[2]	ODOVIF	OUT Data Buffer Overrun Interrupt Flag This bit is set by the hardware circuitry when the received data byte count is larger than the corresponding endpoint OUT data buffer size. Writing 1 into this status bit will clear it to 0.
[1]	ODRXIF	OUT Data Received Interrupt Flag This bit is set by the hardware circuitry when a data packet is successfully received from the host for an OUT-token and when an endpoint n ACK signal is sent to the host. Writing 1 into this status bit will clear it to 0.
[0]	OTRXIF	OUT Token Received Interrupt Flag This bit is set by the hardware circuitry when the endpoint receives an OUT token from the host and is cleared to 0 by writing 1.

USB Endpoint 1~3 Transfer Count Register – USBEPnTCR, n=1~3

This register specifies the Endpoint 1~3 transfer byte count.

Offset: 0x034 (n=1), 0x048 (n=2), 0x05C (n=3)

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							TCNT
Type/Reset								RW 0
	7	6	5	4	3	2	1	0
	TCNT							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[8:0]	TCNT	Transfer Byte Count This bit field contains the number of data bytes received by the endpoint n in the preceding OUT transaction or the number of data bytes to be transmitted by the endpoint n in the next IN transaction.

USB Endpoint 1~3 Configuration Register – USBEPnCFGR, n=1~3

This register specifies the Endpoint 1~3 configurations.

Offset: 0x038 (n=1), 0x04C (n=2), 0x060 (n=3)

Reset value: 0x1000_03FF

	31	30	29	28	27	26	25	24
	EPEN	Reserved	EPTYPE	EPDIR	EPADR			
Type/Reset	RW 0		RW 0	RW 1	RW 0	RW 0	RW 0	RW 0
	23	22	21	20	19	18	17	16
	Reserved							EPLEN
Type/Reset								RW 0
	15	14	13	12	11	10	9	8
	EPLEN						EPBUFA	
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 1	RW 1
	7	6	5	4	3	2	1	0
	EPBUFA							
Type/Reset	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1

Bits	Field	Descriptions
[31]	EPEN	Enable Control 0: Disable the endpoint n 1: Enable the endpoint n
[29]	EPTYPE	Transfer Type This bit is set to 0 by the hardware circuitry to specify that the endpoint n transfer type is an Interrupt or Bulk transfer type.
[28]	EPDIR	Transfer Direction 0: OUT 1: IN
[27:24]	EPADR	Endpoint Address The EPADR field value can be assigned by the application software to specify the address of the endpoint n. It is important to note that this EPADR field should not be set to 0, otherwise, the endpoint will be disabled.
[16:10]	EPLEN	Buffer Length This field is used to specify the endpoint n data packet size. The field value must be word-aligned to a 4-byte boundary. The maximum size in this field can be 64 bytes which is the maximum payload as defined in the USB full-speed standard specification. Note that the EPLEN value should not be assigned to 0 which will result in the endpoint being disabled.
[9:0]	EPBUFA	Buffer Start Address This field is used to specify the endpoint n data buffer start address which ranges from 0x008 to 0x3FC in the EP-SRAM which has a capacity of 1024 bytes and whose field value must be a multiple of 4.

USB Endpoint 4~7 Control and Status Register – USBEPnCSR, n=4~7

This register specifies the Endpoint 4~7 control and status bits.

Offset: 0x064 (n=4), 0x078 (n=5), 0x08C (n=6), 0x0A0 (n=7)

Reset value: 0x0000_0002

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	UDBTG	MDBTG	STLRX	NAKRX	DTGRX	STLTX	NAKTX	DTGTX
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 1	RW 0

Bits	Field	Descriptions
[7]	UDBTG	USB Double Buffer Toggle bit The UDBTG and MDBTG bits are used to indicate which data buffer is accessed by the USB SIE hardware and which data buffer is accessed by the MCU software if the double buffering function is enabled. The UDBTG bit will be toggled by the SIE hardware circuitry after the current buffer operation is complete. After the UDBTG bit is toggled by the SIE, a NAK signal will be sent automatically to the USB host by the hardware circuitry. Therefore, the data transfer will be stopped temporarily until the data in the other buffer has been properly setup after which the MDBTG bit is toggled by the MCU application software. The following tables show the double buffering operation and the UDBTG and MDBTG bit status for an IN or OUT transaction.

Transaction Type	UDBTG	MDBTG	Buffer read by SIE	Buffer written by MCU
IN	0	0	None*	EP_BUF0
	0	1	EP_BUF0	EP_BUF1
	1	1	None*	EP_BUF1
	1	0	EP_BUF1	EP_BUF0

Transaction Type	UDBTG	MDBTG	Buffer written by SIE	Buffer read by MCU
OUT	0	0	None*	EP_BUF0
	0	1	EP_BUF0	EP_BUF1
	1	1	None*	EP_BUF1
	1	0	EP_BUF1	EP_BUF0

* Means the USB device sends a NAK signal to the USB host using the hardware circuitry.

The UDBTG and MDBTG bits setting procedure for the double buffering function is shown in the following example:

[UDBTG, MDBTG]=[0, 0] → [0, 1] → [1, 1] → [1, 0] → [0, 0] → [0, 1] → [1, 1] → [1, 0] →...

[6]	MDBTG	MCU Double Buffer Toggle bit The MDBTG bit is used to indicate which data buffer is accessed by the MCU if the double buffering function is enabled. It can be toggled to switch to the other buffer by the MCU application software after the data in the current buffer accessed by the MCU has been properly setup. The double buffering operation together with the UDBTG and MDBTG bits are shown in the preceding two tables for the UDBTG bit definition.
[5]	STLRX	STALL bit for reception transfers This bit is set to 1 by the application software if a functional error has been detected. This bit can be read and written and can only be toggled by writing 1. It can also be toggled by software to initialise its value under certain conditions.
[4]	NAKRX	NAK bit for reception transfers This bit is toggled from 0 to 1 by the hardware circuitry, which will result in a NAK signal, when a data packet has been received and an ACK signal has been transmitted to the host in the handshake phase of an OUT transaction addressed to this endpoint. It means that the USB device will be temporarily unable to accept data from the USB host until the received data is properly processed. If the endpoint is defined as an Isochronous transfer type, this bit is not available for use. The hardware will not change the NAKRX bit status after a complete transaction. This bit can be read and written and can be only toggled by writing 1.

Bits	Field	Descriptions
[3]	DTGRX	Data Toggle bit for reception transfers If the endpoint is not used for Isochronous transfer, this bit is available for use. This bit contains the expected value of the data toggle bit (0=DATA0, 1=DATA1) for the next data packet to be received. When the current valid data packet is received and the corresponding ACK signal is sent to the USB host by the USB device, the hardware circuitry will toggle this bit and the device will be ready to receive the next data packet. If the endpoint is defined as an Isochronous transfer type, this bit is not used since no data toggling is used and only the DATA0 packet will be transferred for normal Isochronous transfers. This bit can be read and written and can only be toggled by writing 1. This bit can also be toggled by the software to initialise its value under certain conditions.
[2]	STLTX	STALL bit for transmission transfers This bit is set to 1 by the application software if there a functional error has been detected. This bit can be read and written and can be only toggled by writing 1. It can be toggled by the software to initialise its value under certain conditions.
[1]	NAKTX	NAK bit for transmission transfers This bit is toggled from 0 to 1 by the hardware circuitry. This will result in a NAK signal when a data packet has been transmitted and an ACK signal sent from the host has been received in the handshake phase of an IN transaction addressed to this endpoint. It means that the USB device will be temporarily unable to transmit a data packet until the data to be transmitted is properly setup by the application software. If the endpoint is defined as an Isochronous transfer type, then this bit is not available for use. The hardware will not change the NAKTX bit status after a complete transaction. This bit can be read and written and can be only toggled by writing 1. It can also be toggled by the software to initialise its value under certain conditions.
[0]	DTGTX	Data Toggle bit for transmission transfers If the endpoint is not used for Isochronous transfer, this bit is available for use. This bit contains the required value of the data toggle bit (0=DATA0, 1=DATA1) for the next data packet to be transmitted. When the current data packet is transmitted by the USB device and the corresponding ACK signal sent from the USB host is received, the hardware circuitry will toggle this bit and then the next data packet will be transmitted. If the endpoint is used for Isochronous transfer, this bit is not used since no data toggling is used and only the DATA0 packet will be transferred for normal Isochronous transfer. This bit can be read and written and can only be toggled by writing 1. It can also be toggled by the software to initialise its value under certain conditions.

USB Endpoint 4~7 Interrupt Enable Register – USBEPnIER, n=4~7

This register specifies the Endpoint 4~7 interrupt enable control bits.

Offset: 0x068 (n=4), 0x07C (n=5), 0x090 (n=6), 0x0A4 (n=7)

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	UERIE	STLIE	NAKIE	IDTXIE	ITRXIE	ODOVIE	ODRXIE	OTRXIE
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[7]	UERIE	USB Error Interrupt Enable Control 0: Disable interrupt 1: Enable interrupt
[6]	STLIE	STALL Transmitted Interrupt Enable Control 0: Disable interrupt 1: Enable interrupt
[5]	NAKIE	NAK Transmitted Interrupt Enable Control 0: Disable interrupt 1: Enable interrupt
[4]	IDTXIE	IN Data Transmitted Interrupt Enable Control 0: Disable interrupt 1: Enable interrupt
[3]	ITRXIE	IN Token Received Interrupt Enable Control 0: Disable interrupt 1: Enable interrupt
[2]	ODOVIE	OUT Data Buffer Overrun Interrupt Enable Control 0: Disable interrupt 1: Enable interrupt
[1]	ODRXIE	OUT Data Received Interrupt Enable Control 0: Disable interrupt 1: Enable interrupt
[0]	OTRXIE	OUT Token Received Interrupt Enable Control 0: Disable interrupt 1: Enable interrupt

USB Endpoint 4~7 Interrupt Status Register – USBEPnISR, n=4~7

This register specifies the Endpoint 4~7 interrupt status.

Offset: 0x06C (n=4), 0x080 (n=5), 0x094 (n=6), 0x0A8 (n=7)

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	UERIF	STLIF	NAKIF	IDTXIF	ITRXIF	ODOVIF	ODRXIF	OTRXIF
Type/Reset	WC 0	WC 0	WC 0	WC 0	WC 0	WC 0	WC 0	WC 0

Bits	Field	Descriptions
[7]	UERIF	USB Error Interrupt Flag This bit is set by the hardware circuitry when an error occurs during the transaction. Writing 1 into this status bit will clear it to 0.
[6]	STLIF	STALL Transmitted Interrupt Flag This bit is set by the hardware circuitry when a STALL-token is sent in response to an IN or OUT token and is cleared to 0 by writing 1.
[5]	NAKIF	NAK Transmitted Interrupt Flag This bit is set by the hardware circuitry when a NAK-token is sent in response to an IN or OUT token and is cleared to 0 by writing 1.
[4]	IDTXIF	IN Data Transmitted Interrupt Flag This bit is set by the hardware circuitry when a data packet is successfully transmitted to the host in response to an IN-token and an ACK-token is received. Writing 1 into this status bit will clear it to 0.
[3]	ITRXIF	IN Token Received Interrupt Flag This bit is set by the hardware circuitry when the endpoint receives an IN token from the host and is cleared to 0 by writing 1.
[2]	ODOVIF	OUT Data Buffer Overrun Interrupt Flag This bit is set by the hardware circuitry when the received data byte count is larger than the endpoint OUT data buffer size. Writing 1 into this status bit will clear it to 0.
[1]	ODRXIF	OUT Data Received Interrupt Flag This bit is set by the hardware circuitry when a data packet is successfully received from the host for an OUT-token and an ACK signal is sent to the host. Writing 1 into this status bit will clear it to 0.
[0]	OTRXIF	OUT Token Received Interrupt Flag This bit is set by the hardware circuitry when the endpoint receives an OUT token from the host ad is cleared to 0 by writing 1.

USB Endpoint 4~7 Transfer Count Register – USBEPnTCR, n=4~7

This register specifies the Endpoint 4~7 transfer byte count.

Offset: 0x070 (n=4), 0x084 (n=5), 0x098 (n=6), 0x0AC (n=7)

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved						TCNT1	
Type/Reset							RW 0	RW 0
	23	22	21	20	19	18	17	16
	TCNT1							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
	Reserved						TCNT0	
Type/Reset							RW 0	RW 0
	7	6	5	4	3	2	1	0
	TCNT0							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[25:16]	TCNT1	Buffer 1 Transfer Byte Count This bit field contains the number of data bytes received by the endpoint n buffer 1 in the preceding OUT transaction or the number of data bytes to be transmitted by the endpoint n buffer 1 in the next IN transaction.
[9:0]	TCNT0	Buffer 0 Transfer Byte Count This bit field contains the number of data bytes received by the endpoint n buffer 0 in the preceding OUT transaction or the number of data bytes to be transmitted by the endpoint n buffer 0 in the next IN transaction. Only the TCNT0 field is used for the endpoint data transfer count when the endpoint is configured as a single-buffering transfer type.

USB Endpoint 4~7 Configuration Register – USBEPnCFGR, n=4~7

This register specifies the Endpoint 4~7 configurations.

Offset: 0x074 (n=4), 0x088 (n=5), 0x09C (n=6), 0x0B0 (n=7)

Reset value: 0x1000_03FF

	31	30	29	28	27	26	25	24
	EN	Reserved	TYPE	DIR	EPADR			
Type/Reset	RW 0		RW 0	RW 1	RW 0	RW 0	RW 0	RW 0
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	SDBS	Reserved			LEN			
Type/Reset	RW 0				RW 0	RW 0	RW 0	RW 0
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	LEN						BUFA	
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 1	RW 1
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	BUFA							
Type/Reset	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1

Bits	Field	Descriptions
[31]	EN	Enable Control 0: Disable the endpoint n 1: Enable the endpoint n
[29]	TYPE	Transfer Type 0: Interrupt or Bulk transfer type 1: Isochronous transfer type
[28]	DIR	Transfer Direction 0: OUT 1: IN
[27:24]	EPADR	Endpoint Address The EPADR field can be configured by the application software to specify the address of endpoint n. It is important to note that this EPADR field should not be set to 0, otherwise, the endpoint n will be disabled.
[23]	SDBS	Single-Buffering or Double-Buffering Selection 0: Single-buffering 1: Double-buffering If the SDBS bit is set to 1, the endpoint buffer size is twice that of the LEN value: – Endpoint Buffer 0 start address is BUFA – Endpoint Buffer 1 start address is (BUFA + LEN)
[19:10]	LEN	Buffer Length This field is used to specify the endpoint n data packet size whose field value must be word-aligned to a 4-byte boundary. Note that the endpoint will be disabled if the LEN value is assigned to 0.
[9:0]	BUFA	Buffer Start Address This field is used to specify the endpoint n data buffer start address which ranges from 0x008 to 0x3FC in the EP-SRAM which has a capacity of 1024 bytes where the endpoint transfer data is stored. Note that the buffer start address value must be a multiple of 4.

24 Peripheral Direct Memory Access (PDMA)

Introduction

The Peripheral Direct Memory Access circuitry, PDMA, provides 12 unidirectional channels for dedicated peripherals to implement the peripheral-to-memory and memory-to-peripheral data transfer. The memory-to-memory data transfer such as the FLASH-to-SRAM or SRAM-to-SRAM type is also supported and requested by the application program. Each PDMA channel configuration is independent. The PDMA channel transfer is split into multiple block transactions and the size of a block is equal to the block length multiplied by the data width.

Features

- 12 unidirectional PDMA channels
- Memory-to-peripheral, peripheral-to-memory and memory-to-memory data transfer
- 8-bit, 16-bit and 32-bit width data transfer
- Software and hardware requested data transfer with configurable channel priority
- Linear, circular and non-increment address modes
- 4 transfer event flags – Transfer complete, Half Transfer, Block End and Transfer Error
- Auto-Reload function

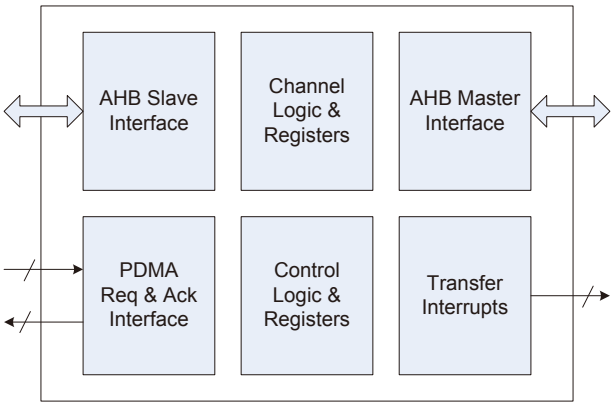


Figure 158. PDMA Block Diagram

Functional Descriptions

AHB Master

The PDMA is an AHB master connected to other AHB peripherals such as the FLASH memory, the SRAM memory and the AHB-to-APB bridges through the bus-matrix. The Cortex™-M3 and PDMA can access different AHB slaves at the same time via the bus-matrix.

PDMA Channel

There are 12 unidirectional PDMA channels used to support data transfer between the peripherals and the memory. The configuration and operation of each PDMA channel is independent. For a bidirectional transfer application, two PDMA channels are required. Each PDMA channel is designed to support the dedicated multiple peripherals with the same registers. Therefore, one PDMA channel only can service one peripheral at the same time. The related registers of the PDMA channel are limited to be accessed with 32-bit operations, otherwise a system hard fault event will occur.

Table 61. PDMA Channel Assignments

IP	PDMA Channel Number											
	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8	CH9	CH10	CH11
CSIF	CSIF											
ADC		ADC										
SPIx			SPI0_TX	SPI0_RX			SPI1_TX	SPI1_RX				
USARTx					UR0_TX	UR0_RX			UR1_TX	UR1_RX		
SCI											SCI_TX	SCI_RX
I2Cx	I2C1_TX	I2C1_RX									I2C0_TX	I2C0_RX
MCTM			MT_CH0	MT_CH1	MT_CH3 MT_TRIG MT_UP2	MT_UP1	MT_CH2					
GPTMx	GT0_CH1 GT0_CH3	GT0_CH2	GT0_UP					GT0_CH0 GT0_TRIG	GT1_CH0	GT1_CH2 GT1_UP	GT1_CH1	GT1_CH3 GT1_TRIG

Channel transfer

A PDMA channel transfer is split into multiple block transactions with PDMA arbitration occurring at the end of each block transaction. Although these 12 channel transfers can all be activated, there is only one block transaction being transferred through the bus at a time. The channel transfer sequence depends upon the channel priority setting of each PDMA channel. The total transfer size is calculated from the block transaction count and block size. The block size is equal to the product of the block length and data bit width. For an efficient transfer, it is recommended that the block length is set as a multiple of 4.

Channel Priority

The PDMA provides four priority levels, known as very high, high, medium and low, which can be configured by the application software. The PDMA also provides two methods to determine the channel priority. One is determined by application software configuration and the other is determined by the fixed hardware channel number. The PDMA arbitration processor will first check the software configuring channel priority level used to request the PDMA to provide the data transfer services. If more than one channel has the same priority, the channel with a smaller channel number will have priority over one with a larger channel number after arbitration.

Note that the highest priority channel will not occupy the PDMA service all the time when other lower priority channel requests are pending. The highest priority channel will be skipped for one block transaction time duration after one block transaction is complete. Then a block transaction requested by the second priority channel will be performed. After a block transaction of the second priority channel is complete, the PDMA arbitration processor will re-check all of the requested channel priority with the exception of the second priority channel since the second priority channel will be excluded after the end of a block transaction. Therefore, a block data transaction of the higher priority channel will be serviced and this channel will be excluded from the priority arbitration at the end of the block transaction. The PDMA will keep transferring the data using the method described above until all of the requested channel data transfer is complete. Refer to the accompanying figure for an example which shows the PDMA channel arbitration and scheduling.

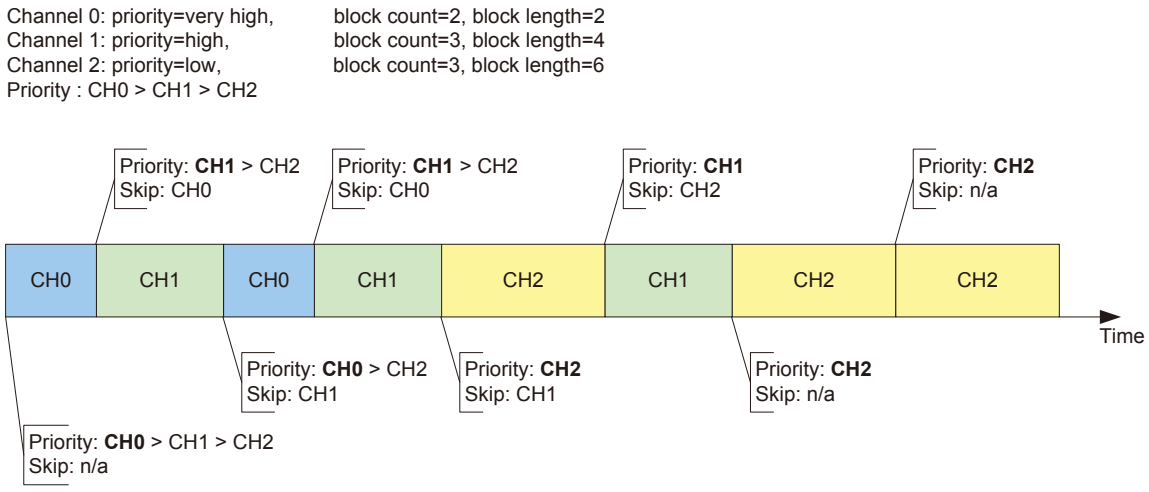


Figure 159. PDMA Channel Arbitration and Scheduling Example

Transfer Request

For a peripheral-to-memory or memory-to-peripheral transfer, one peripheral hardware request will trigger one block transaction of the dedicated PDMA channel. However, a complete data transfer of the relevant dedicated PDMA channel will be triggered when a software request occurs. It is recommended that the PDMA channel is configured to have a lower priority level and a smaller block length which is requested by the software for memory-to-memory data copy applications.

Address Mode

The PDMA provides three kinds of address modes which are the linear address, circular address and fixed address modes. These different address modes are used to support different kinds of source and destination address arrangements. The following table shows the detailed address mode combinations.

Table 62. PDMA Address Modes

Source Address Mode	Destination Address Mode
Linear Increment/Decrement Address	Linear Increment/Decrement Address
Linear Increment/Decrement Address	Circular Increment/Decrement Address
Linear Increment/Decrement Address	Fixed Address
Circular Increment/Decrement Address	Linear Increment/Decrement Address
Circular Increment/Decrement Address	Circular Increment/Decrement Address
Fixed Address	Linear Increment/Decrement Address
Fixed Address	Fixed Address

Linear Address Mode

After data is transferred, the current address will be increased or decreased by 1, 2 or 4 depending upon the data bit width setting.

Circular Address Mode

After data is transferred, the current address will be increased or decreased by 1, 2 or 4 depending upon the data bit width setting. When a block transaction is complete, the current address is loaded with the configured start address.

Fixed Address Mode

After data is transferred, the current address remains unchanged.

Auto-Reload

When the auto-reload control bit, AUTORLn, in the PDMA channel n control register named PDMACHnCR is set, both the channel n current address stored in the PDMACHnCADR register and the channel n current transfer size in the PDMACHnCTSR register will be automatically reloaded with the corresponding start value after the current PDMA channel data transfer has totally completed. The channel n will still be activated and the next relative PDMA request can be serviced without any re-configuration using the application software.

Transfer Interrupt

There are five transfer events during which the interrupts can be asserted for each PDMA channel. These are the block transaction end (BE), half-transfer (HT), transfer complete (TC), transfer error (TE) and global transfer event (GE). Setting the corresponding control bits in the PDMA interrupt enable register named PDMAIER will enable the relevant interrupt events. The global interrupt event, GE, will be generated if any of the four interrupt events including the BE, HT, TC or TE occurs. Clearing the BE, HT, TC or TE event flags will also clear the GE flag. Clearing the GE flag will automatically clear all other event flags. The TE interrupt event will occur when the PDMA accesses a system reserved address space or the PDMA receives a request but when the corresponding transfer size setting is equal to zero.

Register Map

The following table shows the PDMA registers and the reset values.

Table 63. PDMA Register Map

Register	Offset	Description	Reset Value
PDMA Base Address=0x4009_0000			
PDMA Channel 0 Registers			
PDMACH0CR	0x000	PDMA Channel 0 Control Register	0x0000_0000
PDMACH0SADR	0x004	PDMA Channel 0 Source Address Register	0x0000_0000
PDMACH0DADR	0x008	PDMA Channel 0 Destination Address Register	0x0000_0000
PDMACH0CADR	0x00C	PDMA Channel 0 Current Address Register	0x0000_0000
PDMACH0TSR	0x010	PDMA Channel 0 Transfer Size Register	0x0000_0000
PDMACH0CTSR	0x014	PDMA Channel 0 Current Transfer Size Register	0x0000_0000
PDMA Channel 1 Registers			
PDMACH1CR	0x018	PDMA Channel 1 Control Register	0x0000_0000
PDMACH1SADR	0x01C	PDMA Channel 1 Source Address Register	0x0000_0000
PDMACH1DADR	0x020	PDMA Channel 1 Destination Address Register	0x0000_0000
PDMACH1CADR	0x024	PDMA Channel 1 Current Address Register	0x0000_0000
PDMACH1TSR	0x028	PDMA Channel 1 Transfer Size Register	0x0000_0000
PDMACH1CTSR	0x02C	PDMA Channel 1 Current Transfer Size Register	0x0000_0000
PDMA Channel 2 Registers			
PDMACH2CR	0x030	PDMA Channel 2 Control Register	0x0000_0000
PDMACH2SADR	0x034	PDMA Channel 2 Source Address Register	0x0000_0000
PDMACH2DADR	0x038	PDMA Channel 2 Destination Address Register	0x0000_0000
PDMACH2CADR	0x03C	PDMA Channel 2 Current Address Register	0x0000_0000
PDMACH2TSR	0x040	PDMA Channel 2 Transfer Size Register	0x0000_0000
PDMACH2CTSR	0x044	PDMA Channel 2 Current Transfer Size Register	0x0000_0000
PDMA Channel 3 Registers			
PDMACH3CR	0x048	PDMA Channel 3 Control Register	0x0000_0000
PDMACH3SADR	0x04C	PDMA Channel 3 Source Address Register	0x0000_0000
PDMACH3DADR	0x050	PDMA Channel 3 Destination Address Register	0x0000_0000
PDMACH3CADR	0x054	PDMA Channel 3 Current Address Register	0x0000_0000
PDMACH3TSR	0x058	PDMA Channel 3 Transfer Size Register	0x0000_0000

Register	Offset	Description	Reset Value
PDMA Base Address=0x4009_0000			
PDMACH3CTSR	0x05C	PDMA Channel 3 Current Transfer Size Register	0x0000_0000
PDMA Channel 4 Registers			
PDMACH4CR	0x060	PDMA Channel 4 Control Register	0x0000_0000
PDMACH4SADR	0x064	PDMA Channel 4 Source Address Register	0x0000_0000
PDMACH4DADR	0x068	PDMA Channel 4 Destination Address Register	0x0000_0000
PDMACH4CADR	0x06C	PDMA Channel 4 Current Address Register	0x0000_0000
PDMACH4TSR	0x070	PDMA Channel 4 Transfer Size Register	0x0000_0000
PDMACH4CTSR	0x074	PDMA Channel 4 Current Transfer Size Register	0x0000_0000
PDMA Channel 5 Registers			
PDMACH5CR	0x078	PDMA Channel 5 Control Register	0x0000_0000
PDMACH5SADR	0x07C	PDMA Channel 5 Source Address Register	0x0000_0000
PDMACH5DADR	0x080	PDMA Channel 5 Destination Address Register	0x0000_0000
PDMACH5CADR	0x084	PDMA Channel 5 Current Address Register	0x0000_0000
PDMACH5TSR	0x088	PDMA Channel 5 Transfer Size Register	0x0000_0000
PDMACH5CTSR	0x08C	PDMA Channel 5 Current Transfer Size Register	0x0000_0000
PDMA Channel 6 Registers			
PDMACH6CR	0x090	PDMA Channel 6 Control Register	0x0000_0000
PDMACH6SADR	0x094	PDMA Channel 6 Source Address Register	0x0000_0000
PDMACH6DADR	0x098	PDMA Channel 6 Destination Address Register	0x0000_0000
PDMACH6CADR	0x09C	PDMA Channel 6 Current Address Register	0x0000_0000
PDMACH6TSR	0x0A0	PDMA Channel 6 Transfer Size Register	0x0000_0000
PDMACH6CTSR	0x0A4	PDMA Channel 6 Current Transfer Size Register	0x0000_0000
PDMA Channel 7 Registers			
PDMACH7CR	0x0A8	PDMA Channel 7 Control Register	0x0000_0000
PDMACH7SADR	0x0AC	PDMA Channel 7 Source Address Register	0x0000_0000
PDMACH7DADR	0x0B0	PDMA Channel 7 Destination Address Register	0x0000_0000
PDMACH7CADR	0x0B4	PDMA Channel 7 Current Address Register	0x0000_0000
PDMACH7TSR	0x0B8	PDMA Channel 7 Transfer Size Register	0x0000_0000
PDMACH7CTSR	0x0BC	PDMA Channel 7 Current Transfer Size Register	0x0000_0000
PDMA Channel 8 Registers			
PDMACH8CR	0x0C0	PDMA Channel 8 Control Register	0x0000_0000
PDMACH8SADR	0x0C4	PDMA Channel 8 Source Address Register	0x0000_0000
PDMACH8DADR	0x0C8	PDMA Channel 8 Destination Address Register	0x0000_0000
PDMACH8CADR	0x0CC	PDMA Channel 8 Current Address Register	0x0000_0000
PDMACH8TSR	0x0D0	PDMA Channel 8 Transfer Size Register	0x0000_0000
PDMACH8CTSR	0x0D4	PDMA Channel 8 Current Transfer Size Register	0x0000_0000
PDMA Channel 9 Registers			
PDMACH9CR	0x0D8	PDMA Channel 9 Control Register	0x0000_0000
PDMACH9SADR	0x0DC	PDMA Channel 9 Source Address Register	0x0000_0000
PDMACH9DADR	0x0E0	PDMA Channel 9 Destination Address Register	0x0000_0000

Register	Offset	Description	Reset Value
PDMA Base Address=0x4009_0000			
PDMACH9CADR	0x0E4	PDMA Channel 9 Current Address Register	0x0000_0000
PDMACH9TSR	0x0E8	PDMA Channel 9 Transfer Size Register	0x0000_0000
PDMACH9CTSR	0x0EC	PDMA Channel 9 Current Transfer Size Register	0x0000_0000
PDMA Channel 10 Registers			
PDMACH10CR	0x0F0	PDMA Channel 10 Control Register	0x0000_0000
PDMACH10SADR	0x0F4	PDMA Channel 10 Source Address Register	0x0000_0000
PDMACH10DADR	0x0F8	PDMA Channel 10 Destination Address Register	0x0000_0000
PDMACH10CADR	0x0FC	PDMA Channel 10 Current Address Register	0x0000_0000
PDMACH10TSR	0x100	PDMA Channel 10 Transfer Size Register	0x0000_0000
PDMACH10CTSR	0x104	PDMA Channel 10 Current Transfer Size Register	0x0000_0000
PDMA Channel 11 Registers			
PDMACH11CR	0x108	PDMA Channel 11 Control Register	0x0000_0000
PDMACH11SADR	0x10C	PDMA Channel 11 Source Address Register	0x0000_0000
PDMACH11DADR	0x110	PDMA Channel 11 Destination Address Register	0x0000_0000
PDMACH11CADR	0x114	PDMA Channel 11 Current Address Register	0x0000_0000
PDMACH11TSR	0x118	PDMA Channel 11 Transfer Size Register	0x0000_0000
PDMACH11CTSR	0x11C	PDMA Channel 11 Current Transfer Size Register	0x0000_0000
PDMA Global Register			
PDMAISR0	0x120	PDMA Interrupt Status Register 0	0x0000_0000
PDMAISR1	0x124	PDMA Interrupt Status Register 1	0x0000_0000
PDMAICLR0	0x128	PDMA Interrupt Status Clear Register 0	0x0000_0000
PDMAICLR1	0x12C	PDMA Interrupt Status Clear Register 1	0x0000_0000
PDMAIER0	0x130	PDMA Interrupt Enable Register 0	0x0000_0000
PDMAIER1	0x134	PDMA Interrupt Enable Register 1	0x0000_0000

Register Descriptions

PDMA Channel n Control Register – PDMACHnCR, n=0~11

This register is used to specify the PDMA channel n data transfer configuration.

Offset: 0x000 (0), 0x018 (1), 0x030 (2), 0x048 (3), 0x060 (4), 0x078 (5), 0x090 (6), 0x0A8 (7), 0x0C0 (8), 0x0D8 (9), 0x0F0 (10), 0x108 (11)

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved				AUTORLn	FIXAENn	CHnPRI	
Type/Reset					RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	SRCAMODn	SRCAINCn	DSTAMODn	DSTAINCn	DWIDTHn		SWTRIGn	CHnEN
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[11]	AUTORLn	Channel n Auto Reload Enable Control 0: Disable Auto Reload function 1: Enable Auto Reload function If this bit is set to 1 to enable the auto-reload function, the PDMACHnCADR and PDMACHnCTSR registers will be reloaded with the relevant start value and the PDMA channel n will be activated when a transfer is complete. If this bit is cleared to 0, the PDMACHnCADR and PDMACHnCTSR registers will remain unchanged and the PDMA channel n will be disabled after a transfer completion.
[10]	FIXAENn	Channel n Fixed Address Enable control 0: Disable fixed address function in the circular address mode 1: Enable fixed address function in the circular address mode Note that this bit is only available when the source or destination address mode is set to be in the circular address mode. For example, the source address mode is set as in the linear address mode and the destination address mode is set as in the circular mode. If this bit is set to enable the fixed address function, then the source address mode will still be in the linear address but the destination address mode will be in the fixed address mode instead of the circular address mode.
[9:8]	CHnPRI	Channel n Priority 00: Low 01: Medium 10: High 11: Very high The CHnPRI field is used to configure the channel priority using the application program. If there are more than one channels which have the same software configured priority level, the channel with the smaller channel number will have priority to transfer one block of data after the arbitration.

Bits	Field	Descriptions
[7]	SRCAMODn	Channel n Source Address Mode selection 0: Linear address mode 1: Circular address mode In the linear address mode, the current source address field value, CSADR, in the PDMACHnCADR register can be incremented or decremented, determined by the SRCAINCn bit value during a complete transfer. In the circular address mode, the CSADR field value can be incremented or decremented which is also determined by the SRCAINCn bit value during a block transfer and will be loaded with the lower 16-bit value of the PDMACHnSADR register when a block transaction has completed.
[6]	SRCAINCn	Channel n Source Address Increment control 0: Increment 1: Decrement This bit is used to determine whether the current source address in the CSADR field is increased or decreased during a complete transfer in the linear address mode or a block transfer in the circular address mode.
[5]	DSTAMODn	Channel n Destination Address Mode selection 0: Linear address mode 1: Circular address mode In linear address mode, the current destination address field value, CDADR, in the PDMACHnCADR register can be incremented or decremented, determined by the DSTAINCn bit value during a complete transfer. In the circular address mode, the CDADR field value can be incremented or decremented which is also determined by the DSTAINCn bit value during a block transfer and will be loaded with the lower 16-bit value of the PDMACHnDADR register when a block transfer has completed.
[4]	DSTAINCn	Channel n Destination Address Increment Control 0: Increment 1: Decrement This bit is used to determine if the current destination address in the CDADR field is increased or decreased during a complete transfer in the linear address mode or a block transfer in the circular address mode.
[3:2]	DWIDTHn	Data Bit Width selection 00: 8-bit 01: 16-bit 10: 32-bit 11: Reserved The field is used to select the data bit width of the corresponding PDMA channel n.
[1]	SWTRIGn	Software Trigger control 0: No operation 1: Software triggered transfer request Setting this bit will generate a memory-to-memory software transfer request on the corresponding PDMA channel n. It is automatically cleared when a transfer has completely finished.
[0]	CHnEN	Channel n Enable control 0: Disable the PDMA channel n 1: Enable the PDMA channel n Setting this bit will enable a software or hardware transfer request on the PDMA channel n. It is automatically cleared by hardware when a transfer has completed with the auto-reload function being disabled. However, if the AUTORLn bit is set to 1 to enable the auto-reload function, this bit will be remain high to enable the PDMA channel n function for the next transfer request instead of automatically being cleared by hardware after a transfer has finished.

PDMA Channel n Source Address Register – PDMACHnSADR, n=0~11

This register specifies the source address of the PDMA channel n.

Offset: 0x004 (0), 0x01C (1), 0x034 (2), 0x04C (3), 0x064 (4), 0x07C (5), 0x094 (6), 0x0AC (7), 0x0C4 (8), 0x0DC (9), 0x0F4 (10), 0x10C (11)

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	SADRn							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	SADRn							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	SADRn							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	SADRn							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[31:0]	SADRn	Channel n Source Address The register is used to specify the 32-bit source address of the PDMA channel n.

PDMA Channel n Destination Address Register – PDMACHnDADR, n=0~11

This register specifies the destination address of the PDMA channel n.

Offset: 0x008 (0), 0x020 (1), 0x038 (2), 0x050 (3), 0x068 (4), 0x080 (5), 0x098 (6), 0x0B0 (7), 0x0C8 (8), 0x0E0 (9), 0x0F8 (10), 0x110 (11)

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	DADRn							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	DADRn							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	DADRn							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	DADRn							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[31:0]	DADRn	Channel n Destination Address The register is used to specify the 32-bit destination address of the PDMA channel n.

PDMA Channel n Current Address Register – PDMACHnCADR, n=0~11

This register is used to indicate the lower 16-bit of the PDMA channel n current source and destination address.

Offset: 0x00C (0), 0x024 (1), 0x03C (2), 0x054 (3), 0x06C (4), 0x084 (5), 0x09C (6), 0x0B4 (7), 0x0CC (8), 0x0E4 (9), 0x0FC (10), 0x114 (11)

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	CSADRn[15:8]							
Type/Reset	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	CSADRn[7:0]							
Type/Reset	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	CDADRn[15:8]							
Type/Reset	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	CDADRn[7:0]							
Type/Reset	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0

Bits	Field	Descriptions
[31:16]	CSADRn	Channel n Current Source Address The CSADRn field is a read only 16-bit address indicating the current address of the data being read. After the data has been read, the CSADRn field contains the next address which the data is to be read from. Writing a new value to the PDMACHnSADR register will update the CSADRn field with the lower 16-bit content of the PDMACHnSADR register rather than the complete 32-bit value in the PDMACHnSADR register. The CSADRn field will have 16-bit or 32-bit alignment according to the DWIDTHn field setting in the PDMACHnCR register. For example: If the DWIDTHn field is set as 16-bit, the last bit of the CSADRn field will be 0. If the DWIDTHn field is set as 32-bit, the last 2 bits of the CSADRn field will be 0.
[15:0]	CDADRn	Channel n Current Destination Address The CDADRn field is a read only 16-bit address indicating the current address of the data being written. After the data has been written, the CDADRn field contains the next address where the data is to be written. Writing a new value to the PDMACHnDADR register will update the CDADRn field with the lower 16-bit content of the PDMACHnDADR register rather than the whole 32-bit value in the PDMACHnDADR register. The CDADRn field will have 16-bit or 32-bit alignment according to the DWIDTHn field setting in the PDMACHnCR register. For example: If the DWIDTHn field is set as 16-bit, the last bit of the CDADRn field will be 0. If the DWIDTHn field is set as 32-bit, the last 2 bits of the CDADRn field will be 0.

PDMA Channel n Transfer Size Register – PDMACHnTSR, n=0~11

This register is used to specify the block transaction count and block transaction length.

Offset: 0x010 (0), 0x028 (1), 0x040 (2), 0x058 (3), 0x070 (4), 0x088 (5), 0x0A0 (6), 0x0B8 (7), 0x0D0 (8), 0x0E8 (9), 0x100 (10), 0x118 (11)

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	BLKCNTn [15:8]							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	BLKCNTn [7:0]							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	BLKLENn [15:8]							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	BLKLENn [7:0]							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[31:16]	BLKCNTn	Channel n Block Transaction Count BLKCNTn represents the number of block transactions for a channel n complete transfer. The capacity of a complete transfer is the product of the BLKCNTn and BLKLENn values. The maximum BLKCNTn value is 65,535.
[15:0]	BLKLENn	Channel n Block Length The BLKLENn represents the length of a data block. The data width is defined by the DWIDTHn field in the PDMACHnCR register. The maximum BLKLENn value is 65,535.

PDMA Channel n Current Transfer Size Register – PDMACHnCTSR, n=0~11

This register is used to indicate the current block transaction count and current block length.

Address: 0x014 (0), 0x02C (1), 0x044 (2), 0x05C (3), 0x074 (4), 0x08C (5), 0x0A4 (6), 0x0BC (7), 0x0D4 (8), 0x0EC (9), 0x104 (10), 0x11C (11)

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	CBLKCNTn [15:8]							
Type/Reset	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	CBLKCNTn [7:0]							
Type/Reset	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	CBLKLENn [15:8]							
Type/Reset	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	CBLKLENn [7:0]							
Type/Reset	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0

Bits	Field	Descriptions
[31:16]	CBLKCNTn	Channel n Current Block Count The CBLKCNTn field is a 16-bit read-only value indicating the number of data blocks that remain to be transferred. After a data block has transferred completely, the CBLKCNTn value will be decremented by 1. Writing a new value to the BLKCNTn field in the PDMACHnTSR register will update the CBLKCNTn field value.
[15:0]	CBLKLENn	Channel n Current Block Length The CBLKLENn field is a 16-bit read-only value that indicates how much data in the block remains to be transferred. After a block of data has transferred completely, the CBLKLENn field will be reloaded with the BLKLENn value. Writing a new value to the BLKLENn field in the PDMACHnTSR register will update the CBLKLENn field value.

PDMA Interrupt Status Register 0 – PDMAISR0

This register is used to indicate the corresponding interrupt status of the PDMA channel 0~5.

Offset: 0x120

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved		TEISTA5	TCISTA5	HTISTA5	BEISTA5	GEISTA5	TEISTA4
Type/Reset			RO 0	RO 0	RO 0	RO 0	RO 0	RO 0
	23	22	21	20	19	18	17	16
	TCISTA4	HTISTA4	BEISTA4	GEISTA4	TEISTA3	TCISTA3	HTISTA3	BEISTA3
Type/Reset	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0
	15	14	13	12	11	10	9	8
	GEISTA3	TEISTA2	TCISTA2	HTISTA2	BEISTA2	GEISTA2	TEISTA1	TCISTA1
Type/Reset	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0
	7	6	5	4	3	2	1	0
	HTISTA1	BEISTA1	GEISTA1	TEISTA0	TCISTA0	HTISTA0	BEISTA0	GEISTA0
Type/Reset	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0

Bits	Field	Descriptions
[29], [24], [19], [14], [9], [4]	TEISTAn	Channel n Transfer Error Interrupt Status (n=0~5) 0: No Transfer Error occurs 1: Transfer Error occurs This bit is set by hardware and is cleared by writing 1 into the corresponding interrupt status clear bit in the PDMAISR0 register. A Transfer error will occur when the PDMA accesses a system reserved address space or the PDMA receives a request but when the corresponding transfer capacity is equal to zero.
[28], [23], [18], [13], [8], [3]	TCISTAn	Channel n Transfer Complete Interrupt Status (n=0~5) 0: No Transfer Completion Occurs 1: Transfer Completion Occurs This bit is set by hardware and is cleared by writing 1 into the corresponding interrupt status clear bit in the PDMAISR0 register. The Transfer Completion event will occur when the PDMA has completed a data transfer task.
[27], [22], [17], [12], [7], [2]	HTISTAn	Channel n Half Transfer Interrupt Status (n=0~5) 0: No Half Transfer Event Occurs 1: Half Transfer Event Occurs This bit is set by hardware and is cleared by writing 1 into the corresponding interrupt status clear bit in the PDMAISR0 register. A Half Transfer event will occur when the PDMA has completed half of the data transfer task.
[26], [21], [16], [11], [6], [1]	BEISTAn	Channel n Block Transaction End Interrupt Status (n=0~5) 0: No Block Transaction End Event Occurs 1: Block Transaction End Event Occurs This bit is set by hardware and is cleared by writing 1 into the corresponding interrupt status clear bit in the PDMAISR0 register. A Block Transaction End event will occur when the PDMA completes a data block transaction task.
[25], [20], [15], [10], [5], [0]	GEISTAn	Channel n Global Transfer Interrupt Status (n=0~5) 0: No TE, TC, HT or BE event occurs 1: TE, TC, HT, or BE event occurs This bit is set by hardware and is cleared by writing 1 into the corresponding interrupt status clear bit, GEICLRn, in the PDMAISR0 register. A Global Transfer Event will occur if any of the BE, HT, TC or TE events occur. Also clearing any of the BE, HT, TC or TE event interrupt flags will clear the GE interrupt flag. Note that if 1 is written into the GEICLRn bit in the PDMAISR0 register to clear the GE interrupt flag, the BE, HT, TC and TE event interrupt flags will also be cleared to 0 together with the GE interrupt status flag.

PDMA Interrupt Status Register 1 – PDMAISR1

This register is used to indicate the corresponding interrupt status of the PDMA channel 6~11.

Offset: 0x124

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved		TEISTA11	TCISTA11	HTISTA11	BEISTA11	GEISTA11	TEISTA10
Type/Reset			RO 0	RO 0	RO 0	RO 0	RO 0	RO 0
	23	22	21	20	19	18	17	16
	TCISTA10	HTISTA10	BEISTA10	GEISTA10	TEISTA9	TCISTA9	HTISTA9	BEISTA9
Type/Reset	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0
	15	14	13	12	11	10	9	8
	GEISTA9	TEISTA8	TCISTA8	HTISTA8	BEISTA8	GEISTA8	TEISTA7	TCISTA7
Type/Reset	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0
	7	6	5	4	3	2	1	0
	HTISTA7	BEISTA7	GEISTA7	TEISTA6	TCISTA6	HTISTA6	BEISTA6	GEISTA6
Type/Reset	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0

Bits	Field	Descriptions
[29], [24], [19], [14], [9], [4]	TEISTAm	Channel m Transfer Error Interrupt Status (m=6~11) 0: No Transfer Error Occurs 1: Transfer Error Occurs This bit is set by hardware and is cleared by writing 1 into the corresponding interrupt status clear bit in the PDMAISR1 register. A Transfer error will occur when the PDMA accesses a system reserved address space or the PDMA has received a request but the corresponding transfer capacity is equal to zero.
[28], [23], [18], [13], [8], [3]	TCISTAm	Channel m Transfer Complete Interrupt Status (m=6~11) 0: No Transfer Completion occurs 1: Transfer Completion occurs This bit is set by hardware and is cleared by writing 1 into the corresponding interrupt status clear bit in the PDMAISR1 register. A Transfer Completion event will occur when the PDMA has completed a data transfer task.
[27], [22], [17], [12], [7], [2]	HTISTAm	Channel m Half Transfer Interrupt Status (m=6~11) 0: No Half Transfer Event Occurs 1: Half Transfer Event Occurs This bit is set by hardware and is cleared by writing 1 into the corresponding interrupt status clear bit in the PDMAISR1 register. A Half Transfer event will occur when the PDMA has completed half of the data transfer task.
[26], [21], [16], [11], [6], [1]	BEISTAm	Channel m Block Transaction End Interrupt Status (m=6~11) 0: No Block Transaction End Event Occurs 1: Block Transaction End Event Occurs This bit is set by hardware and is cleared by writing 1 into the corresponding interrupt status clear bit in the PDMAISR1 register. A Block Transaction End event will occur when the PDMA has completed a data block transaction task.
[25], [20], [15], [10], [5], [0]	GEISTAm	Channel m Global Transfer Event Interrupt Status (m=6~11) 0: No TE, TC, HT or BE Event Occurs 1: TE, TC, HT, or BE Event Occurs This bit is set by hardware and is cleared by writing 1 into the corresponding interrupt status clear bit, GEICLRm, in the PDMAISR1 register. A Global Transfer Event will occur if any of the BE, HT, TC or TE events occur. Also clearing any of the BE, HT, TC or TE event interrupt flags will also clear the GE interrupt flag. Note that if 1 is written into the GEICLRm bit in the PDMAISR1 register to clear the GE interrupt flag, the BE, HT, TC and TE event interrupt flags will also be cleared to 0 together with the GE interrupt status flag.

PDMA Interrupt Status Clear Register 0 – PDMAISCR0

This register is used to clear the corresponding interrupt status bits in the PDMAISR0 Register.

Offset: 0x128

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved		TEICLR5	TCICLR5	HTICLR5	BEICLR5	GEICLR5	TEICLR4
Type/Reset			RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	23	22	21	20	19	18	17	16
	TCICLR4	HTICLR4	BEICLR4	GEICLR4	TEICLR3	TCICLR3	HTICLR3	BEICLR3
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
	GEICLR3	TEICLR2	TCICLR2	HTICLR2	BEICLR2	GEICLR2	TEICLR1	TCICLR1
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	HTICLR1	BEICLR1	GEICLR1	TEICLR0	TCICLR0	HTICLR0	BEICLR0	GEICLR0
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[29], [24], [19], [14], [9], [4]	TEICLRn	Channel n Transfer Error Interrupt Status Clear (n=0~5) 0: No Operation 1: Clear the corresponding TEISTAn bit in the PDMAISR0 register Writing 1 into the TEICLRn bit will clear the TEISTAn status bit in the PDMAISR0 register. This bit will be automatically cleared to 0 after 1 is written.
[28], [23], [18], [13], [8], [3]	TCICLRn	Channel n Transfer Complete Interrupt Status Clear (n=0~5) 0: No Operation 1: Clear the corresponding TCISTAn bit in the PDMAISR0 register Writing 1 into the TCICLRn bit will clear the TCISTAn status bit in the PDMAISR0 register. This bit will be automatically cleared to 0 after 1 is written.
[27], [22], [17], [12], [7], [2]	HTRICLRn	Channel n Half Transfer Interrupt Status Clear (n=0~5) 0: No Operation 1: Clear the corresponding HTISTAn bit in the PDMAISR0 register Writing 1 into the HTRICLRn bit will clear the HTISTAn status bit in the PDMAISR0 register. This bit will be automatically cleared to 0 after 1 is written.
[26], [21], [16], [11], [6], [1]	BEICLRn	Channel n Block Transaction End Interrupt Status Clear (n=0~5) 0: No Operation 1: Clear the corresponding BEISTAn bit in the PDMAISR0 register Writing 1 into the BEICLRn bit will clear the BEISTAn status bit in the PDMAISR0 register. This bit will be automatically cleared to 0 after 1 is written.
[25], [20], [15], [10], [5], [0]	GEICLRn	Channel n Global Transfer Event Interrupt Status Clear (n=0~5) 0: No Operation 1: Clear the corresponding TEISTAn, TCISTAn, HTISTAn, BEISTAn, and GEISTAn bits in the PDMAISR0 register Writing 1 into the GEICLRn bit will clear the GEISTAn status bit together with the TEISTAn, TCISTAn, HTISTAn, BEISTAn bits in the PDMAISR0 register. This bit will be automatically cleared to 0 after 1 is written.

PDMA Interrupt Status Clear Register 1 – PDMAISCR1

This register is used to clear the corresponding interrupt status bits in the PDMAISR1 Register.

Offset: 0x12C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved		TEICLR11	TCICLR11	HTICLR11	BEICLR11	GEICLR11	TEICLR10
Type/Reset			RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	23	22	21	20	19	18	17	16
	TCICLR10	HTICLR10	BEICLR10	GEICLR10	TEICLR9	TCICLR9	HTICLR9	BEICLR9
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
	GEICLR9	TEICLR8	TCICLR8	HTICLR8	BEICLR8	GEICLR8	TEICLR7	TCICLR7
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	HTICLR7	BEICLR7	GEICLR7	TEICLR6	TCICLR6	HTICLR6	BEICLR6	GEICLR6
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[29], [24], [19], [14], [9], [4]	TEICLRm	Channel m Transfer Error Interrupt Status Clear (m=6~11) 0: No Operation 1: Clear the corresponding TEISTAm bit in the PDMAISR1 register Writing 1 into the TEICLRm bit will clear the TEISTAm status bit in the PDMAISR1 register. This bit will be automatically cleared to 0 after 1 is written.
[28], [23], [18], [13], [8], [3]	TCICLRm	Channel m Transfer Complete Interrupt Status Clear (m=6~11) 0: No Operation 1: Clear the corresponding TCISTAm bit in the PDMAISR1 register Writing 1 into the TCICLRm bit will clear the TCISTAm status bit in the PDMAISR1 register. This bit will be automatically cleared to 0 after 1 is written.
[27], [22], [17], [12], [7], [2]	HTICLRm	Channel m Half Transfer Interrupt Status Clear (m=6~11) 0: No Operation 1: Clear the corresponding HTISTAm bit in the PDMAISR1 register Writing 1 into the HTICLRm bit will clear the HTISTAm status bit in the PDMAISR1 register. This bit will be automatically cleared to 0 after 1 is written.
[26], [21], [16], [11], [6], [1]	BEICLRm	Channel m Block Transaction End Interrupt Status Clear (m=6~11) 0: No Operation 1: Clear the corresponding BEISTAm bit in the PDMAISR1 register Writing 1 into the BEICLRm bit will clear the BEISTAm status bit in the PDMAISR1 register. This bit will be automatically cleared to 0 after 1 is written.
[25], [20], [15], [10], [5], [0]	GEICLRm	Channel m Global Transfer Event Interrupt Status Clear (m=6~11) 0: No Operation 1: Clear the corresponding TEISTAm, TCISTAm, HTISTAm, BEISTAm, and GEISTAm bits in the PDMAISR1 register Writing 1 into the GEICLRm bit will clear the GEISTAm status bit together with the TEISTAm, TCISTAm, HTISTAm, BEISTAm bits in the PDMAISR1 register. This bit will be automatically cleared to 0 after 1 is written.

PDMA Interrupt Enable Register 0 – PDMAIER0

This register is used to enable or disable the related interrupts of the PDMA channel 0~5.

Offset: 0x130

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved		TEIE5	TCIE5	HTIE5	BEIE5	GEIE5	TEIE4
Type/Reset			RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	23	22	21	20	19	18	17	16
	TCIE4	HTIE4	BEIE4	GEIE4	TEIE3	TCIE3	HTIE3	BEIE3
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
	GEIE3	TEIE2	TCIE2	HTIE2	BEIE2	GEIE2	TEIE1	TCIE1
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	HTIE1	BEIE1	GEIE1	TEIE0	TCIE0	HTIE0	BEIE0	GEIE0
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[29], [24], [19], [14], [9], [4]	TEIEn	Channel n Transfer Error Interrupt Enable control (n=0~5) 0: Transfer Error interrupt is disabled 1: Transfer Error interrupt is enabled This bit is set and cleared by software.
[28], [23], [18], [13], [8], [3]	TCIEn	Channel n Transfer Complete Interrupt Enable control (n=0~5) 0: Transfer Completion interrupt is disabled 1: Transfer Completion interrupt is enabled This bit is set and cleared by software.
[27], [22], [17], [12], [7], [2]	HTIEn	Channel n Half Transfer Interrupt Enable control (n=0~5) 0: Half Transfer interrupt is disabled 1: Half Transfer interrupt is enabled This bit is set and cleared by software.
[26], [21], [16], [11], [6], [1]	BEIEn	Channel n Block Transaction End Interrupt Enable control (n=0~5) 0: Block Transaction End interrupt is disabled 1: Block Transaction End interrupt is enabled This bit is set and cleared by software.
[25], [20], [15], [10], [5], [0]	GEIEn	Channel n Global Transfer Event Interrupt Enable control (n=0~5) 0: Global Transfer Event interrupt is disabled 1: Global Transfer Event interrupt is enabled This bit is set and cleared by software.

PDMA Interrupt Enable Register 1 – PDMAIER1

This register is used to enable or disable the related interrupts of the PDMA channel 6~11.

Offset: 0x134

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved		TEIE11	TCIE11	HTIE11	BEIE11	GEIE11	TEIE10
Type/Reset			RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	23	22	21	20	19	18	17	16
	TCIE10	HTIE10	BEIE10	GEIE10	TEIE9	TCIE9	HTIE9	BEIE9
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
	GEIE9	TEIE8	TCIE8	HTIE8	BEIE8	GEIE8	TEIE7	TCIE7
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	HTIE7	BEIE7	GIE7	TEIE6	TCIE6	HTIE6	BEIE6	GEIE6
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[29], [24], [19], [14], [9], [4]	TEIEm	Channel m Transfer Error Interrupt Enable (m=6~11) 0: Transfer Error interrupt is disabled 1: Transfer Error interrupt is enabled This bit is set and cleared by software.
[28], [23], [18], [13], [8], [3]	TCIEm	Channel m Transfer Complete Interrupt Enable (m=6~11) 0: Transfer Completion interrupt is disabled 1: Transfer Completion interrupt is enabled This bit is set and cleared by software.
[27], [22], [17], [12], [7], [2]	HTIEm	Channel m Half Transfer Interrupt Enable (m=6~11) 0: Half Transfer interrupt is disabled 1: Half Transfer interrupt is enabled This bit is set and cleared by software.
[26], [21], [16], [11], [6], [1]	BEIEm	Channel m Block Transaction End Interrupt Enable (m=6~11) 0: Block Transaction End interrupt is disabled 1: Block Transaction End interrupt is enabled This bit is set and cleared by software.
[25], [20], [15], [10], [5], [0]	GEIEm	Channel m Global Transfer Event Interrupt Enable (m=6~11) 0: Global Transfer Event interrupt is disabled 1: Global Transfer Event interrupt is enabled This bit is set and cleared by software.

25 CMOS Sensor Interface (CSIF, for HT32F2755 Only)

Introduction

The CMOS Sensor Interface, otherwise known as the CSIF, provides an interface for image capture from CMOS sensors. The device can be connected to the CMOS sensor directly using its CMOS Sensor Interface. The CSIF supports both Vertical SYNC and Horizontal SYNC modes for image capture implementation. The CSIF consists of window capture and sub-sampling functions together with dual FIFOs, each with a capacity of 8×32 bits, to store data which can be moved to the internal SRAM via the Peripheral Direct Memory Access circuitry, PDMA. The CSIF does not support image data conversion or decode but rather transfer the image data received from the CMOS sensor to the internal SRAM transparently.

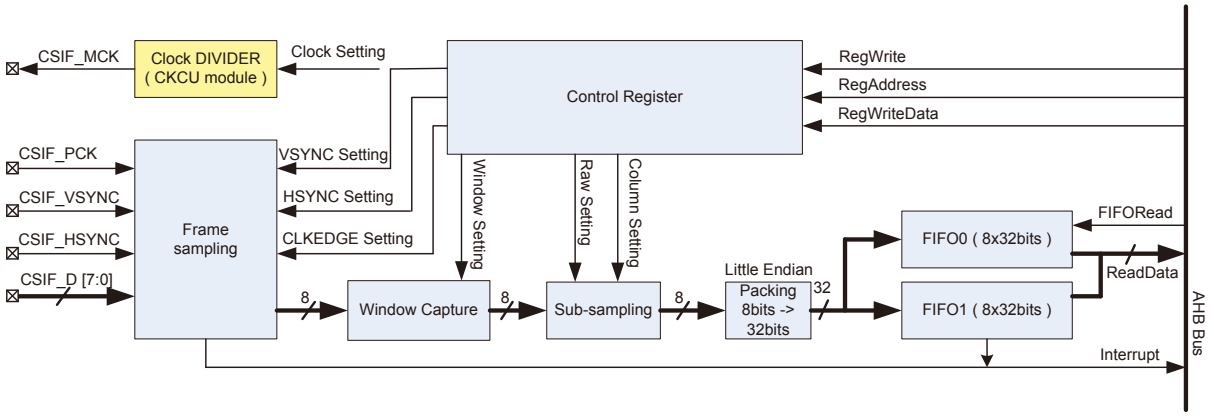


Figure 160. CSIF Block Diagram

Features

- Up to 2048×2048 input resolution
- Supports 8-bit YUV422 and Raw RGB formats
- Up to 24MHz input pixel clock frequency
- VSYNC and HSYNC various settings for image capture
- Hardware window capture function
- Fractional hardware sub-sample function
- Dual FIFOs each with a capacity of 8×32 bits which can be read by PDMA or CPU

Functional Descriptions

CSIF Signal

There are five CSIF signal types. The CSIF has different internal settings to capture the image in different formats.

Table 64. CSIF Signals

Signal	Direction	Description
CSIF_MCK	Output	Output clock to CMOS sensor
CSIF_PCK	Input	Pixel clock from CMOS sensor
CSIF_VSYNC	Input	Vertical SYNC signal from CMOS sensor
CSIF_HSYNC	Input	Horizontal SYNC signal from CMOS sensor
CSIF_D [7:0]	Input	Pixel Data from CMOS sensor

In order to obtain different image frame rates, the application software can setup the CSIFMPRE field in the GCFGR register in the Clock Control Unit, CKCU, to generate different clocks for the CMOS sensor. The CSIF_MCK prescaler is located in the CKCU due to power consumption considerations and other design issues. Refer to the CKCU Chapter for detailed CSIF_MCK prescaler setting information.

Table 65. CSIF_MCK Output Setup – refer to the CKCU Chapter

Register name	Register field	CSIF_MCK output
GCFGR	CSIFMPRE [4:0]	CK_PLL/(CSIFMPRE + 1)/2

CSIF Frame Timing

The module provides various settings for the Vertical SYNC mode, VSYNC, and the Horizontal SYNC mode, HSYNC. There are two types of VSYNC signal, one is short pulse active (no overlap with the HSYNC signal) and the other is active when the frame is valid (overlap with the HSYNC signal). The required type is selected using the VSYNCTYP bit. There are also two types of HSYNC signal, one is continuously active and the other is active when the frame is valid. The required type is selected using the HSYNCTYP bit. The VSYNCPOL and HSYNCPOL bits are used to determine the corresponding VSYNC and HSYNC signal polarity. The data can be sampled on the CSIF_PCK falling or rising edge determined by the CLKEDGE bit. The IMG_SFD field defines the number of lines to be skipped while the IMG_SLD field defines the number of pixels to be skipped. Users can use the IMG_SLD and the IMG_SFD fields to discard pixels and lines to obtain the actual valid image data. The image vertical height is equal to the IMG_HGH value incremented by one and the image horizontal width is equal to the IMG_WID field value incremented by one. Therefore, users can select different settings to match the CMOS sensor output timing to capture the image.

If the CSIF enable bit, CSIF_EN, is set to 1, the CSIF can start to capture the image data when the image frame starts and both the EOF_FLG and the CAP_STS flags are cleared. When the EOF_FLG bit is set or the CAP_STS bit is set, the CSIF will not capture the image data even though the image frame starts. There are two methods to capture the next image data. One is to clear the EOF_FLG and CAP_STS flags to zero, the other is to disable the CSIF function by clearing the CSIF_EN bit and then enable the CSIF function again by setting the CSIF_EN bit.

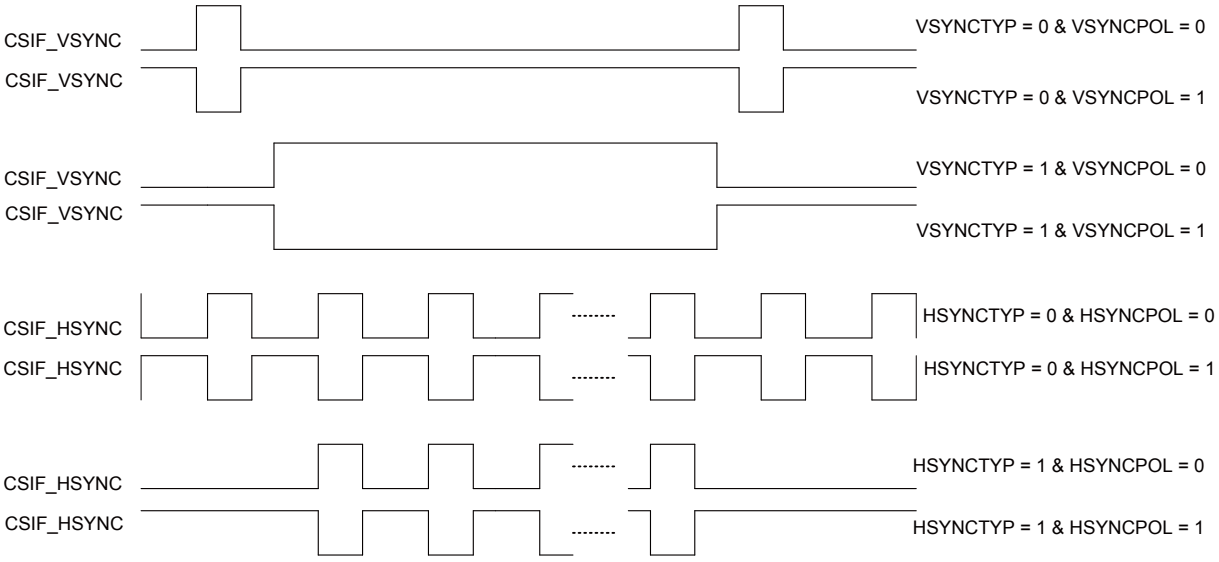


Figure 161. VSYNC & HSYNC Timing

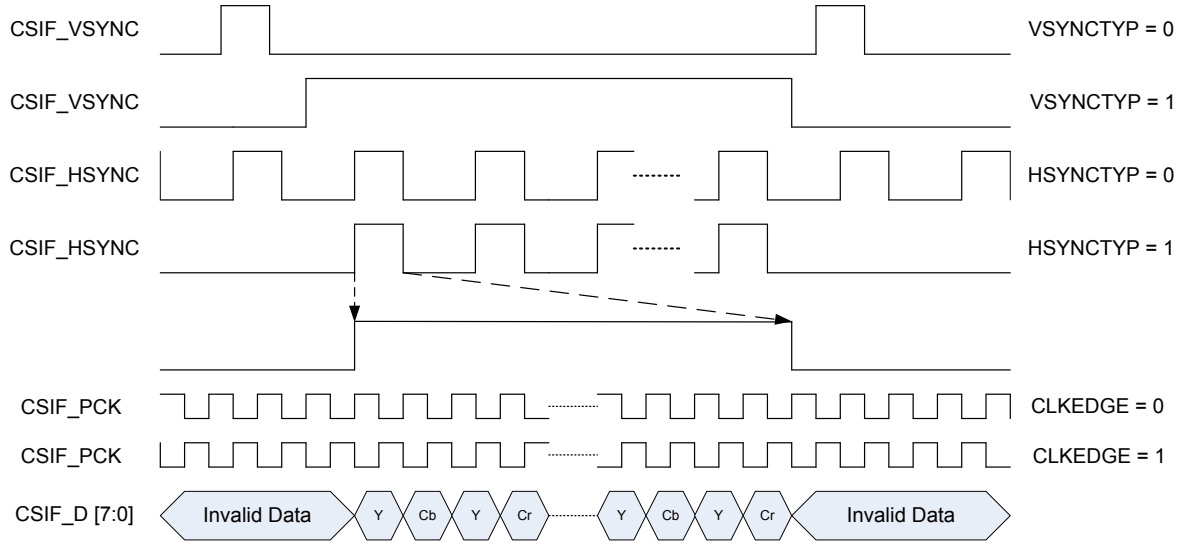


Figure 162. CSIF Frame Timing

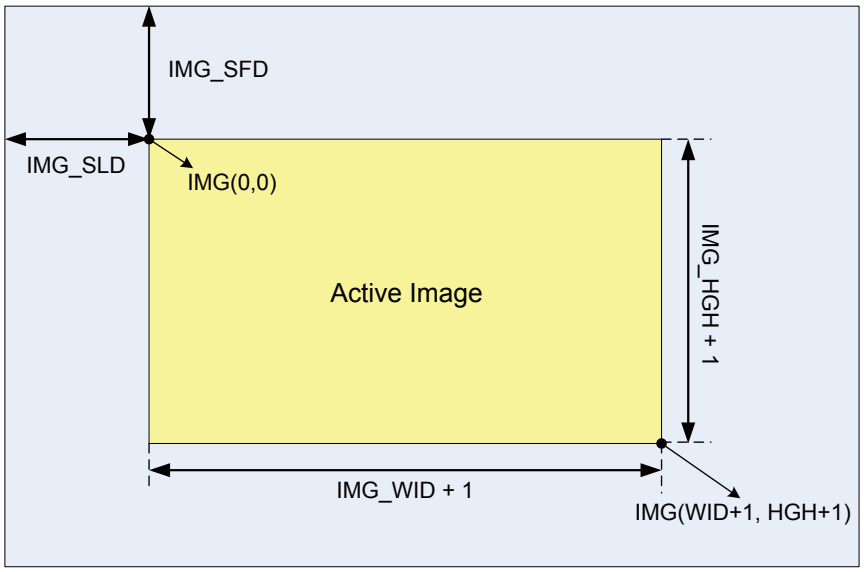


Figure 163. Image Structure

Pixel Data Format

The CSIF provides two pixel data format settings, the Raw RGB format and the YUV422 format. The Raw RGB format is one byte data per pixel while the YUV422 format is two bytes data per pixel. The pixel data bit is sampled on the CSIF_PCK clock falling or rising edge determined by the CLKEDGE bit. Each pixel data byte is considered as a data pack and every four bytes of data are packed in Little Endian mode (P3P2P1P0) to be stored in the FIFO. Software can use this setting to match the CMOS sensor data format.

Table 66. Pixel Data Format – without Window-capturing and Sub-sampling

MODE	BYTE3	BYTE2	BYTE1	BYTE0
Raw RGB 1 byte/pixel	R1	G1	R0	G0
	R3	G3	R2	G2
YUV422 2 bytes/pixel	V0	Y1	U0	Y0
	V1	Y3	U1	Y2

Window Capture

The CSIF provides a window capture function to scale down the image size to decrease memory utilisation. There are five registers to be configured to complete the window capture function. The location, defined by the WIN_HSTR and WIN_VSTR fields, is the start point in the active image region. The WIN_WID and WIN_HGH fields define the image capture region. Note that the window region defined by the WIN_WID and the WIN_HGH fields based on the window start point should be in the active image region defined by the IMG_WID and IMG_HGH fields respectively. If the specified window region is partially out of the active image region defined by the IMG_WID and IMG_HGH fields, the pixel data from the specified active image region will be discarded.

Table 67. Window Capture Setting

Setting	Register	Description
WIN_EN	CSIFWCR0[31]	Window Capture Enable
WIN_HSTR	CSIFWCR0[10:0]	Window Horizontal Start Point
WIN_VSTR	CSIFWCR0[26:16]	Window Vertical Start Point
WIN_WID	CSIFWCR1[10:0]	Window Width
WIN_HGH	CSIFWCR1[26:16]	Window Height

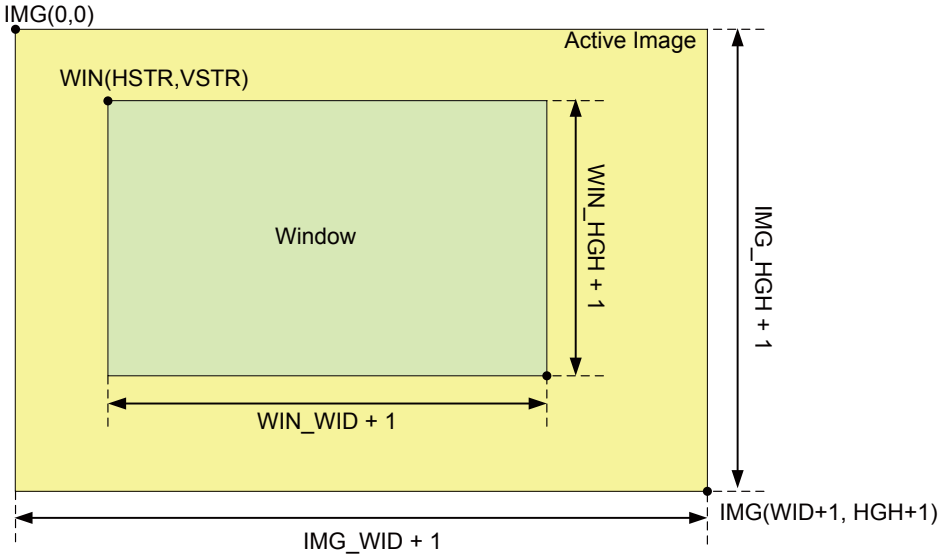


Figure 164. Proper Window Capture

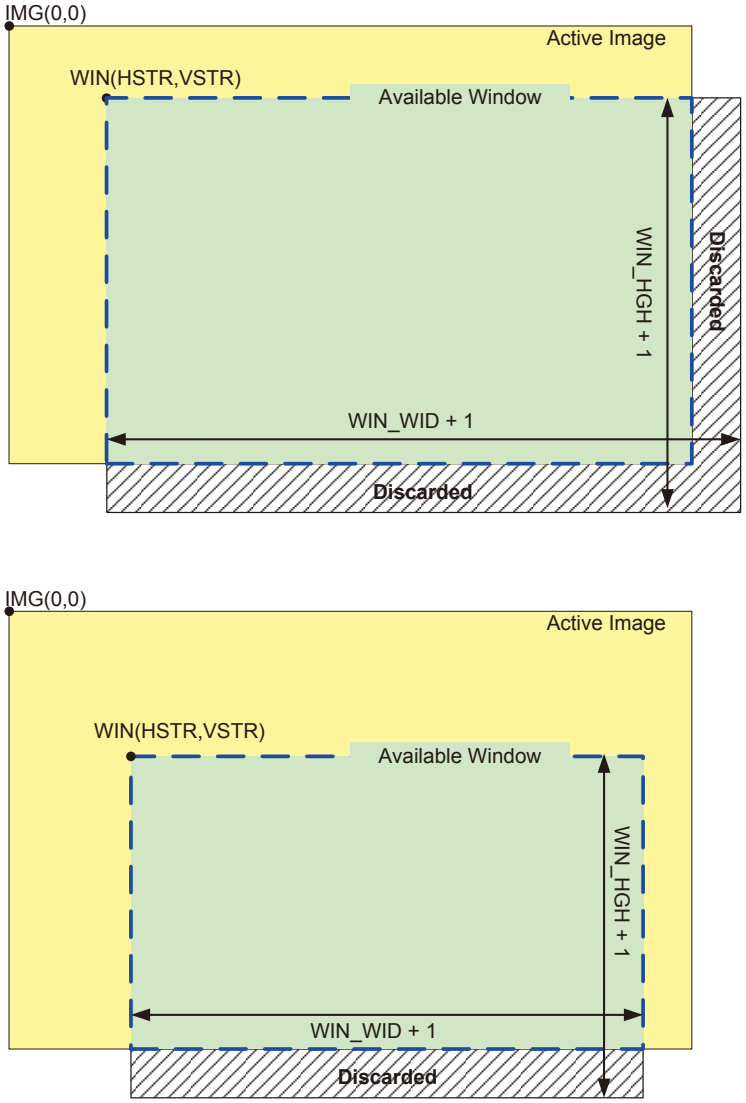


Figure 165. Improper Window Capture

Row & Column Sub-Sampling

The CSIF provides a fractional row and column sub-sampling function in the captured window. This function can be used to obtain fractional image samples according to the application algorithm. The CSML and RSML fields are used to define the sub-sampled column and row length. The CSM and RSM fields are used to control the sub-sampled column and row sample function. The CSIF will continuously sample the data according to the CSM and RSM enable bit and the sub-region defined by the CSML and RSML fields. When the CSM or RSM sample enable control bit is cleared, the CSIF will discard the corresponding data.

Table 68. Row & Column Sub-sampling Setting

Register Setting	Descriptions	Note
SMP_EN	Row & Column sub-sampling enable	CSIFSMP [31]
CSML [4:0]	Column Sub-sampled Length	Column Sub-sampled Length=CSML+1
CSM [31:0]	Column Sample Enable Control	Column n Sample Enable control: CSM [n], n=0~31 1: Enable sample 0: Disable sample
RSML [4:0]	Row Sub-sampled Length	Row Sub-sampled Length=RSML+1
RSM [31:0]	Row Sample Enable Control	Row n Sample Enable control: RSM [n], n=0~31 1: Enable sample 0: Disable sample

R \ C	0	1	2	3	4	5	6	7
0	G1	R	G1	R	G1	R	G1	R
1	B	G2	B	G2	B	G2	B	G2
2	G1	R	G1	R	G1	R	G1	R
3	B	G2	B	G2	B	G2	B	G2
4	G1	R	G1	R	G1	R	G1	R
5	B	G2	B	G2	B	G2	B	G2
6	G1	R	G1	R	G1	R	G1	R
7	B	G2	B	G2	B	G2	B	G2

Column Sample Length
CSML [4:0] = 0x07
Column Sample
CSM [7:0] = 0011_1111
C[7]·····C[0]

Row Sample Length
RSML [4:0] = 0x07
Row Sample
RSM [7:0] = 0011_1111
R[7]·····R[0]

R \ C	0	1	2	3	4	5	6	7	8	9
0	G1	R	G1	R	G1	R	G1	R	G1	R
1	B	G2	B	G2	B	G2	B	G2	B	G2
2	G1	R	G1	R	G1	R	G1	R	G1	R
3	B	G2	B	G2	B	G2	B	G2	B	G2
4	G1	R	G1	R	G1	R	G1	R	G1	R
5	B	G2	B	G2	B	G2	B	G2	B	G2
6	G1	R	G1	R	G1	R	G1	R	G1	R
7	B	G2	B	G2	B	G2	B	G2	B	G2
8	G1	R	G1	R	G1	R	G1	R	G1	R
9	B	G2	B	G2	B	G2	B	G2	B	G2

Column Sample Length
CSML [4:0] = 0x09
Column Sample
CSM [9:0] = 00_1100_1111
C[9] ·····C[0]

Row Sample Length
RSML [4:0] = 0x09
Row Sample
RSM [9:0] = 00_1100_1111
R[9] ·····R[0]

R \ C	0	1	2	3	4	5	6	7
0	Y	Cb	Y	Cr	Y	Cb	Y	Cr
1	Y	Cb	Y	Cr	Y	Cb	Y	Cr
2	Y	Cb	Y	Cr	Y	Cb	Y	Cr
3	Y	Cb	Y	Cr	Y	Cb	Y	Cr
4	Y	Cb	Y	Cr	Y	Cb	Y	Cr
5	Y	Cb	Y	Cr	Y	Cb	Y	Cr
6	Y	Cb	Y	Cr	Y	Cb	Y	Cr
7	Y	Cb	Y	Cr	Y	Cb	Y	Cr

Column Sample Length
CSML [4:0] = 0x01
Column Sample
CSM [1:0] = 01
C[1]C[0]

Row Sample Length
RSML [4:0] = 0x00
Row Sample
RSM [0] = 1
R[0]

Figure 166. Row and Column Sub-sampling Example

PDMA Data Transmission – Trigger PDMA by Rx

The CSIF contains dual FIFOs where each FIFO has an 8 word capacity, i.e., 8×32 bits. When one FIFO is full, the CSIF will send a request to the PDMA to request servicing. The CSIF always sends 8 data words each time through the PDMA to the SRAM to decrease the PDMA latency time. If the available data in the FIFO is less than 8 words, the CSIF will automatically fill the rest of the FIFO words with 0x0000.

Interrupts and Status

The device includes several interrupts and relevant status registers which are used to identify the present CSIF status and to subsequently allow decision making and actions to be taken. The CSIF interrupts include the Start of Frame interrupt, End of Frame interrupt, Capture Start interrupt, Capture Status interrupt, Bad Frame interrupt, FIFO overrun interrupt, FIFO Empty interrupt and the FIFO Full interrupt. The Start of Frame interrupt, if enabled, will be generated when the available CSIF_VSYNC signal determined by the VSYNCPOL and VSYNCTYP bits is received. The End of Frame interrupt will be generated when the total active image data bits determined by the IMG_WID, IMG_HGH and IMG_FMT setting are received by the CSIF if the corresponding interrupt is enabled. The Capture Start interrupt is generated when the relevant interrupt is enabled and the first active image data is received. The Capture Status interrupt is generated when the total pixel data to be captured has been received and transferred to the SRAM by the PDMA or CPU interface. The Bad Frame interrupt is generated when the CSIF detects abnormal VSYNC and HSYNC signals. The FIFO Overrun interrupt request will occur when the two FIFOs are both full and additional data continues to be written into the FIFO. The FIFO Empty interrupt request status is set to 1 when the dual FIFOs are empty and is cleared to 0 when one FIFO is full. The FIFO Full interrupt request flag is asserted when one FIFO is filled with the image data and is cleared to 0 when the data is read from the full FIFO.

Table 69. Interrupts and Status

Interrupt Status	Register	Description
SOF_FLG	CSIFSR [0]	Start of frame
EOF_FLG	CSIFSR [1]	End of frame
CAP_STA	CSIFSR [2]	Capture Start
CAP_STS	CSIFSR [3]	Capture Status: End or not End
BAD_FRM	CSIFSR [4]	Bad Frame
FIFO_OVR	CSIFSR [8]	FIFO Overrun
FIFO_EMP	CSIFSR [9]	FIFO Empty
FIFO_FUL	CSIFSR [10]	FIFO Full

Table 70. Interrupts Status

Interrupt Status	Description	Setting Criteria	Clearing Criteria
SOF_FLG	Start of frame	CSIF_EN=1, EOF_FLG=0, CAP_STS=0 and an available VSYNC signal starts	write 1 to clear
EOF_FLG	End of frame	CSIF_EN=1 and all the active image data has been received	write 1 to clear
CAP_STA	Capture Start	CSIF_EN=1, EOF_FLG=0, CAP_STS=0 and the first data at the start point of the active Image (after discarding IMG_SLD and IMG_SFD) is being captured	write 1 to clear
CAP_STS	Capture Status	CSIF_EN=1, all captured data has been received and been transferred by the PDMA	write 1 to clear
BAD_FRM	Bad Frame	Bad frame acceptance	write 1 to clear
FIFO_OVR	FIFO Overrun	CSIF_EN=1, dual FIFOs are full and New data word is written into the FIFO	CSIF_EN bit falling edge
FIFO_EMP	FIFO Empty	CSIF_EN=1 and dual FIFOs are empty	One FIFO is full
FIFO_FUL	FIFO Full	CSIF_EN=1 and one FIFO is full	Read one word of data from the full FIFO

Register Map

The following table shows the CSIF registers and their reset values.

Table 71. CSIF Register Map

Register	Offset	Description	Reset Value
CSIF Base Address=0x400C_C000			
CSIFENR	0x000	CSIF Enable Register	0x0000_0000
CSIFCR	0x004	CSIF Control Register	0x0000_0004
CSIFIMGWH	0x008	CSIF Image Width and Height Register	0x0000_0000
CSIFWCR0	0x00C	CSIF Window Capture Register 0	0x0000_0000
CSIFWCR1	0x010	CSIF Window Capture Register 1	0x0000_0000
CSIFSMP	0x014	CSIF Sub-Sample Register	0x0000_0000
CSIFSMPCOL	0x018	CSIF Column Sub-Sample Register	0x0000_0000
CSIFSMPROW	0x01C	CSIF Row Sub-Sample Register	0x0000_0000
CSIFFIFO0	0x020	CSIF FIFO Register 0	0x0000_0000
CSIFFIFO1	0x024	CSIF FIFO Register 1	0x0000_0000
CSIFFIFO2	0x028	CSIF FIFO Register 2	0x0000_0000
CSIFFIFO3	0x02C	CSIF FIFO Register 3	0x0000_0000
CSIFFIFO4	0x030	CSIF FIFO Register 4	0x0000_0000
CSIFFIFO5	0x034	CSIF FIFO Register 5	0x0000_0000
CSIFFIFO6	0x038	CSIF FIFO Register 6	0x0000_0000
CSIFFIFO7	0x03C	CSIF FIFO Register 7	0x0000_0000
CSIFIER	0x040	CSIF Interrupt Enable Register	0x0000_0000
CSIFSR	0x044	CSIF Status Register	0x0000_0000

Register Descriptions

CSIF Enable Register – CSIFENR

This register specifies the CSIF enable control.

Offset: 0x000

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	CSIF_EN	Reserved						
Type/Reset	RW 0							
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved							
Type/Reset								

Bits	Field	Descriptions
[31]	CSIF_EN	CSIF Enable Control 0: CSIF is disabled (default) 1: CSIF is enabled

CSIF Control Register – CSIFCR

This register contains various types of the CSIF control bits including the image format, image frame and line delay, sampling clock edge selection, synchronisation polarity and types, etc.

Offset: 0x004

Reset value: 0x0000_0004

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	IMG_SFD							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	IMG_SLD							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	HSYNCPOL	VSYNCPOL	PDMA_DIS	IMG_FMT	CLKEDGE	HSYNCTYP	VSYNCTYP	Reserved
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 1	RW 0	

Bits	Field	Descriptions
[23:16]	IMG_SFD	Image Frame Delay Frame Delay=0x00~0xFF The IMG_SFD field defines the number of lines to be skipped to specify the active image start point.
[15:8]	IMG_SLD	Image Line Delay Line Delay=0x00~0xFF The IMG_SLD field defines the number of pixels to be skipped to specify the active image start point.
[7]	HSYNCPOL	HSYNC Polarity 0: HSYNC polarity high (default) 1: HSYNC polarity low
[6]	VSYNCPOL	VSYNC Polarity 0: VSYNC polarity high (default) 1: VSYNC polarity low
[5]	PDMA_DIS	PDMA Disable 0: PDMA mode (default) 1: CPU mode
[4]	IMG_FMT	Image Format 0: Raw RGB (default) 1: YUV422
[3]	CLKEDGE	Pixel Clock Sample Edge 0: Falling edge to sample data (default) 1: Rising edge to sample data
[2]	HSYNCTYP	HSYNC Type 0: Continuous 1: Active during frame valid (default)
[1]	VSYNCTYP	VSYNC Type 0: Pulse (no overlap with HSYNC) (default) 1: Active during frame valid (overlap with HSYNC)

CSIF Image Width and Height Register – CSIFIMGWH

This register specifies the active image width and height settings.

Offset: 0x008

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved					IMG_HGH		
Type/Reset						RW 0	RW 0	RW 0
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	IMG_HGH							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	Reserved					IMG_WID		
Type/Reset						RW 0	RW 0	RW 0
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	IMG_WID							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[26:16]	IMG_HGH	Image Height The active image height field contents can be in the range from 0x0000 to 0x07FF and the relevant specified image height will be actually in the range from 0x0001 to 0x0800.
[10:0]	IMG_WID	Image Width The active image width field contents can be in the range from 0x0000 to 0x07FF and the relevant specified image width will be actually in the range from 0x0001 to 0x0800.

CSIF Window Capture Register 0 – CSIFWCR0

The register contains the window capture function enable control and specifies the window capture start point.

Offset: 0x00C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	WIN_EN	Reserved				WIN_VSTR		
Type/Reset	RW 0					RW 0	RW 0	RW 0
	23	22	21	20	19	18	17	16
	WIN_VSTR							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
	Reserved					WIN_HSTR		
Type/Reset						RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	WIN_HSTR							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[31]	WIN_EN	Window Capture Enable Control 0: Window capture is disabled (default) 1: Window capture is enabled
[26:16]	WIN_VSTR	Capture Window Vertical Start Point The WIN_VSTR field contents can be from 0x0000 to 0x07FF based on the active image start point within the specified image dimension.
[10:0]	WIN_HSTR	Capture Window Horizontal Start Point The WIN_HSTR field contents can be from 0x0000 to 0x07FF based on the active image start point within the specified image dimension.

CSIF Window Capture Register 1 – CSIFWCR1

The register specifies the window capture height and width settings.

Offset: 0x010

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved					WIN_HGH		
Type/Reset						RW 0	RW 0	RW 0
	23	22	21	20	19	18	17	16
	WIN_HGH							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
	Reserved					WIN_WID		
Type/Reset						RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	WIN_WID							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[26:16]	WIN_HGH	Window Height The WIN_HGH field contents can be in the range from 0x0000 to 0x07FF and the relevant window height will be from 0x0001 to 0x0800. The actual window height should be within the active image dimension.
[10:0]	WIN_WID	Window Width The WIN_WID field contents can be in the range from 0x0000 to 0x07FF and the relevant window width will be from 0x0001 to 0x0800. The actual window width should be within the active image dimension.

CSIF Sub-Sample Register – CSIFSMP

The register specifies the row and column sub-sampled length together with the sub-sampling function enable control.

Offset: 0x014

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	SMP_EN	Reserved						
Type/Reset	RW 0							
	23	22	21	20	19	18	17	16
	Reserved			RSML				
Type/Reset				RW 0	RW 0	RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
	Reserved			CSML				
Type/Reset				RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	Reserved							
Type/Reset								

Bits	Field	Descriptions
[31]	SMP_EN	CSIF Row & Column Sub-Sample Enable control 0: Sub-sample function is disabled (default) 1: Sub-sample function is enabled
[20:16]	RSML	Row Sub-sampled Length 0: 1 bit 1: 2 bits … 31: 32 bits
[12:8]	CSML	Column Sub-sampled Length 0: 1 bit 1: 2 bits … 31: 32 bits

CSIF Column Sub-Sample Register – CSIFSMPCOL

The register specifies the column sample enable control.

Offset: 0x018

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	CSM							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	23	22	21	20	19	18	17	16
	CSM							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
	CSM							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	CSM							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[31:0]	CSM	Column Sample Enable Control 0: Disable sample 1: Enable sample The column n sample enable control bit, CSM[n], determines whether the corresponding column data is sampled or discarded.

CSIF Row Sub-Sample Register – CSIFSMPROW

The register specifies the row sample enable control.

Offset: 0x01C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	RSM							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	23	22	21	20	19	18	17	16
	RSM							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
	RSM							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	RSM							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[31:0]	RSM	Row Sample Enable Control 0: Disable sample 1: Enable sample The row n sample enable control bit, RSM[n], determines whether the corresponding row data is sampled or discarded.

CSIF FIFO Register n – CSIFFIFOn, n=0~7

The register stores the n[th] FIFO data word .

Offset: 0x020~0x03C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	FIFOData							
Type/Reset	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	FIFOData							
Type/Reset	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	FIFOData							
Type/Reset	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	FIFOData							
Type/Reset	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0

Bits	Field	Descriptions
[31:0]	FIFOData	FIFO Data The FIFO Data is read by the PDMA or the CPU interface.

CSIF Interrupt Enable Register – CSIFIER

The register specifies the CSIF interrupt enable control bits.

Offset: 0x040

Reset value: 0x0000_0200

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved					FIFOFULE	FIFOEMPE	FIFOOVRE
Type/Reset						RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	Reserved			BADFRME	CAPSTSE	CAPSTAE	EOFFLGE	SOFFLGE
Type/Reset				RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[10]	FIFOFULE	FIFO Full Interrupt Enable Bit 0: Interrupt is disabled (default) 1: Interrupt is enabled
[9]	FIFOEMPE	FIFO Empty Interrupt Enable Bit 0: Interrupt is disabled (default) 1: Interrupt is enabled
[8]	FIFOOVRE	FIFO Overrun Interrupt Enable Bit 0: Interrupt is disabled (default) 1: Interrupt is enabled
[4]	BADFRME	Bad Frame Interrupt Enable Bit 0: Interrupt is disabled (default) 1: Interrupt is enabled
[3]	CAPSTSE	Capture Status Interrupt Enable Bit 0: Interrupt is disabled (default) 1: Interrupt is enabled
[2]	CAPSTAE	Capture Start Interrupt Enable Bit 0: Interrupt is disabled (default) 1: Interrupt is enabled
[1]	EOFFLGE	End of Frame Interrupt Enable Bit 0: Interrupt is disabled (default) 1: Interrupt is enabled
[0]	SOFFLGE	Start of Frame Interrupt Enable Bit 0: Interrupt is disabled (default) 1: Interrupt is enabled

CSIF Status Register – CSIFSR

The register contains the CSIF status.

Offset: 0x044

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved					FIFO_FUL	FIFO_EMP	FIFO_OVR
Type/Reset						RO 0	RO 0	RO 0
	7	6	5	4	3	2	1	0
	Reserved			BAD_FRM	CAP_STS	CAP_STA	EOF_FLG	SOF_FLG
Type/Reset				WC 0	WC 0	WC 0	WC 0	WC 0

Bits	Field	Descriptions
[10]	FIFO_FUL	FIFO Full Flag 0: FIFO is not full 1: One FIFO is full Once the data word is read from the full FIFO, the FIFO Full flag will be cleared to 0.
[9]	FIFO_EMP	FIFO Empty Flag 0: FIFO is not empty 1: Dual FIFOs are empty When one FIFO is completely filled with data words, the FIFO Empty flag will be cleared to 0.
[8]	FIFO_OVR	FIFO Overrun Flag 0: FIFO has not overrun 1: FIFO has overrun If the two FIFOs are full and a new data word is written into the FIFO, the FIFO Overrun flag will be set to 1. The FIFO Overrun flag is cleared to 0 by clearing the CSIF_EN bit to 0.
[4]	BAD_FRM	Bad Frame Flag 0: The received frame size is correct 1: The received frame size is incorrect When the received frame size is smaller than the active image size as defined by the CSIF, the Bad Frame flag will be set to 1 and the corresponding image data should be discarded. This bit is cleared to 0 by writing 1 into it.
[3]	CAP_STS	Capture Status Flag 0: Capture operation in progress 1: Capture operation finished When all the image data to be captured has been received and transferred to the SRAM by the PDMA, the Capture Status flag will be set to 1. This bit is cleared to 0 by writing 1 into it.

Bits	Field	Descriptions
[2]	CAP_STA	Capture Start Flag 0: Capture does not start 1: Capture starts When the first active image data is received as the relevant CSIF VSYNC and HSYNC signals are active, the Capture Start flag will be set to 1. This bit is cleared to 0 by writing 1 into it.
[1]	EOF_FLG	End of Frame Flag 0: Frame has not ended 1: Frame ends When all the active image data has been received, the End of Frame flag will be set to 1. This bit is cleared to 0 by writing 1 into it.
[0]	SOF_FLG	Start of Frame Flag 0: Frame does not start 1: Frame starts When the CSIF receives an available VSYNC signal, the Start of Frame flag will be set to 1 which means that the frame data reception will start. This bit is cleared to 0 by writing 1 into it.

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