Holtek 32-Bit Microcontroller with Arm® Cortex®-M0+ Core

HT32F52220/HT32F52230
User Manual

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1 Introduction

Overview

This user manual provides detailed information including how to use the devices, system and bus architecture, memory organization and peripheral instructions. The target audiences for this document are software developers, application developers and hardware developers. For more information regarding pin assignment, package and electrical characteristics, please refer to the datasheet.

The devices are high performance and low power consumption 32-bit microcontrollers based around an Arm® Cortex®-M0+ processor core. The Cortex®-M0+ is a next-generation processor core which is tightly coupled with Nested Vectored Interrupt Controller (NVIC), SysTick timer, and including advanced debug support.

The devices operate at a frequency of up to 40 MHz for HT32F52220/52230 with a Flash accelerator to obtain maximum efficiency. It provides up to 32 KB of embedded Flash memory for code/data storage and 4 KB of embedded SRAM memory for system operation and application program usage. A variety of peripherals, such as ADC, I^2C, USART, UART, SPI, GPTM, SCTM, SW-DP (Serial Wire Debug Port), etc., are also implemented in the device series. Several power saving modes provide the flexibility for maximum optimization between wakeup latency and power consumption, an especially important consideration in low power applications.

The above features ensure that the devices are suitable for use in a wide range of applications, especially in areas such as white goods application control, power monitors, alarm systems, consumer products, handheld equipment, data logging applications, motor control and so on.

Features

- Core
  - 32-bit Arm® Cortex®-M0+ processor core
  - Up to 40MHz operating frequency for HT32F52220/52230
  - 0.93 DMIPS/MHz (Dhrystone v2.1)
  - Single-cycle multiplication
  - Integrated Nested Vectored Interrupt Controller (NVIC)
  - 24-bit SysTick timer
- On-chip Memory
  - Up to 32 KB on-chip Flash memory for instruction/data and options storage
  - Up to 4 KB on-chip SRAM
  - Supports multiple boot modes
- Flash Memory Controller – FMC
  - Flash accelerator for maximum efficiency
  - 32-bit word programming with In System Programming Interface (ISP) and In Application Programming (IAP)
  - Flash protection capability to prevent illegal access
- Reset Control Unit – RSTCU
  - Supply supervisor: Power On Reset / Power Down Reset (POR/PDR) and Programmable Low Voltage Detector (LVD)
- Clock Control Unit – CKCU
  - External 4 to 16 MHz crystal oscillator
  - Internal 8 MHz RC oscillator trimmed to ±2 % accuracy at 3.3 V operating voltage and 25 ºC operating temperature
  - Internal 32 kHz RC oscillator
  - Integrated system clock PLL
  - Independent clock divider and gating bits for peripheral clock sources
- Power management – PWRCU
  - Single V_{DD} power supply: 2.0 V to 3.6 V
  - Integrated 1.5 V LDO regulator for CPU core, peripherals and memories power supply
  - Two power domains: V_{DD} and 1.5 V
  - Four power saving modes: Sleep, Deep-Sleep1, Deep-Sleep2, Power-Down
- External Interrupt/Event Controller – EXTI
  - Up to 16 EXTI lines with configurable trigger source and type
  - All GPIO pins can be selected as EXTI trigger source
  - Source trigger type includes high level, low level, negative edge, positive edge, or both edge
  - Individual interrupt enable, wakeup enable and status bits for each EXTI line
  - Software interrupt trigger mode for each EXTI line
  - Integrated deglitch filter for short pulse blocking

- Analog to Digital Converter – ADC
  - 12-bit SAR ADC engine
  - Up to 1 MSPS conversion rate – 1 μs at 28 MHz, 1.4 μs at 40 MHz
  - Up to 8 external analog input channels
- IO ports – GPIO
  - Up to 23 GPIOs
  - Port A, B are mapped as 16 external interrupts – EXTI
  - Almost I/O pins are configurable output driving current
- PWM Generation and Capture Timer – GPTM
  - One 16-bit up, down, up/down auto-reload counter
  - Up to 4 independent channels for each GPTM
  - 16-bit programmable prescaler allowing dividing the counter clock frequency by any factor between 1 and 65536
  - Input Capture function
  - Compare Match Output
  - PWM waveform generation with Edge-aligned and Center-aligned Counting Modes
  - Single Pulse Mode Output
  - Encoder interface controller with two inputs using quadrature decoder
- Single Channel PWM Generation and Capture Timers – SCTM
  - One 16-bit up and auto-reload counter
  - One channels for each SCTM
  - 16-bit programmable prescaler allowing dividing the counter clock frequency by any factor between 1 and 65536
  - Input Capture function
  - Compare Match Output
  - PWM waveform generation with Edge-aligned
  - Single Pulse Mode Output
- Basic Function Timer – BFTM
  - 32-bit compare/match count-up counter – no I/O control features
  - One shot mode – counting stops after a match condition
  - Repetitive mode – restart counter after a match condition
- Watchdog Timer
  - 12-bit down counter with 3-bit prescaler
  - Reset event for the system
  - Programmable watchdog timer window function
  - Registers write protection function
- Inter-integrated Circuit – I^2C
  - Supports both master and slave modes with a frequency of up to 1 MHz
  - Provide an arbitration function and clock synchronization
  - Supports 7-bit and 10-bit addressing modes and general call addressing
  - Supports slave multi-addressing mode with maskable address

- Serial Peripheral Interface – SPI
  - Supports both master and slave mode
  - Frequency of up to (f_{PCLK}/2) MHz for master mode and (f_{PCLK}/3) MHz for slave mode
  - FIFO Depth: 8 levels
  - Multi-master and multi-slave operation
- Universal Synchronous Asynchronous Receiver Transmitter – USART
  - Supports both asynchronous and clocked synchronous serial communication modes
  - Asynchronous operating baud rate up to (f_{PCLK}/16) MHz and synchronous operating rate up to (f_{PCLK}/8) MHz
  - Capability of full duplex communication
  - Fully programmable characteristics of serial communication including: word length, parity bit, stop bit and bit order
  - Error detection: Parity, overrun, and frame error
  - Support Auto hardware flow control mode – RTS, CTS
  - IrDA SIR encoder and decoder
  - RS485 mode with output enable control
  - FIFO Depth: 8 × 9 bits for both receiver and transmitter
- Universal Asynchronous Receiver Transmitter – UART
  - Asynchronous serial communication operating baud-rate up to (f_{PCLK}/16) MHz
  - Capability of full duplex communication
  - Fully programmable characteristics of serial communication including: word length, parity bit, stop bit and bit order
  - Error detection: Parity, overrun, and frame error
- Debug Support
  - Serial Wire Debug Port – SW-DP
  - 4 comparators for hardware breakpoint or code / literal patch
  - 2 comparators for hardware watchpoints
- Package and Operation Temperature
  - 24/28-pin SSOP, 33-pin QFN package
  - Operation temperature range: -40 °C to +85 °C

Device Information

Table 1. Features and Peripheral List

Peripherals		HT32F52220	HT32F52230
Main Flash (KB)		16	31
Option Bytes Flash (KB)		1	1
SRAM (KB)		4	4
Timers	GPTM	1	
	SCTM	2	
	BFTM	1	
	WDT	1	
Communication	SPI	1	
	USART	1	
	UART	1	
	I^2C	1	
EXTI		16	
12-bit ADC Number of channels		1 8 Channels	
GPIO		Up to 23	
CPU frequency		Up to 40 MHz	
Operating voltage		2.0 V ~ 3.6 V	
Operating temperature		-40 °C ~ +85 °C	
Package		24/28-pin SSOP, 33-pin QFN	

Block Diagram

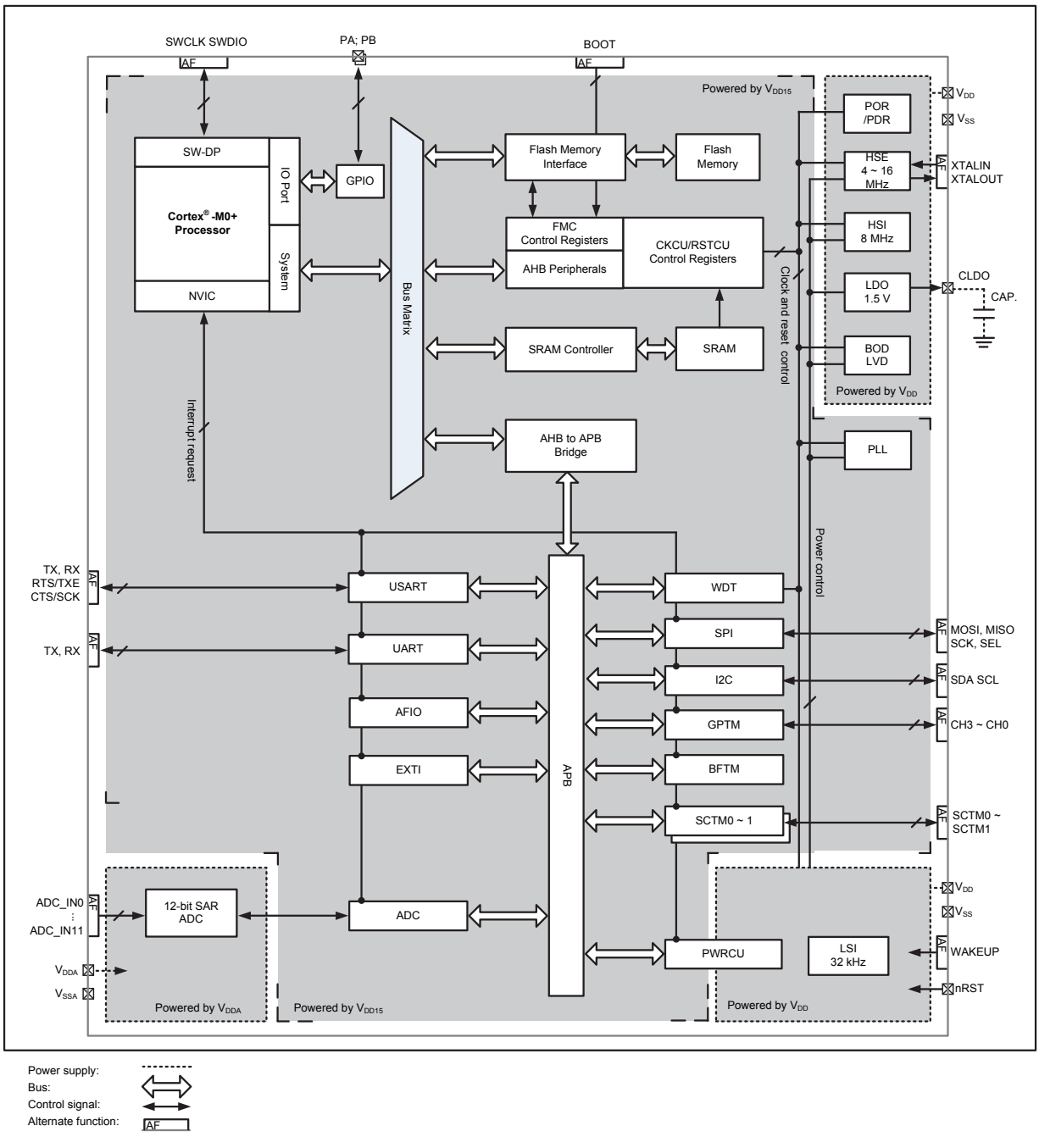
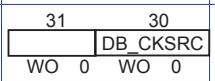
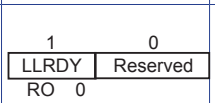


Figure 1. Block Diagram

2 Document Conventions

The conventions used in this document are shown in the following table.

Table 2. Document Conventions

Notation	Example	Description
0x	0x5a05	The number string with a 0x prefix indicates a hexadecimal number.
0xnnnn_nnnn	0x2000_0100	32-bit Hexadecimal address or data.
b	b0101	The number string with a lowercase b prefix indicates a binary number.
NAME [n]	ADDR [5]	Specific bit of NAME. NAME can be a register or field of register. For example, ADDR [5] means bit 5 of ADDR register (field).
NAME [m:n]	ADDR [11:5]	Specific bits of NAME. NAME can be a register or field of register. For example, ADDR [11:5] means bit 11 to 5 of ADDR register (field).
X	b10X1	Don't care notation which means any value is allowed.
RW		Software can read and write to this bit.
RO		Software can only read this bit. A write operation will have no effect.
RC		Software can only read this bit. Read operation will clear it to 0 automatically.
WC		Software can read this bit or clear it by writing 1. Writing a 0 will have no effect.
W0C		Software can read this bit or clear it by writing 0. Writing a 1 will have no effect.
WO		Software can only write to this bit. A read operation always returns 0.
Reserved		Reserved bit(s) for future use. Data read from these bits is not well defined and should be treated as random data. Normally these reserved bits should be set to a 0 value. Note that reserved bit must be kept at reset value.
Word		Data length of a word is 32-bit.
Half-word		Data length of a half-word is 16-bit.
Byte		Data length of a byte is 8-bit.

3 System Architecture

The system architecture of devices that includes the Arm® Cortex®-M0+ processor, bus architecture and memory organization will be described in the following sections. The Cortex®-M0+ is a next generation processor core which offers many new features. Integrated and advanced features make the Cortex®-M0+ processor suitable for market products that require microcontrollers with high performance and low power consumption. In brief, The Cortex®-M0+ processor includes AHB-Lite bus interface. All memory accesses of the Cortex®-M0+ processor are executed on the AHB-Lite bus according to the different purposes and the target memory spaces. The memory organization uses a Harvard architecture, pre-defined memory map and up to 4 GB of memory space, making the system flexible and extendable.

Arm® Cortex®-M0+ Processor

The Cortex®-M0+ processor is a very low gate count, highly energy efficient processor that is intended for microcontroller and deeply embedded applications that require an area optimized, low-power processor. The processor is based on the ARMv6-M architecture and supports Thumb® instruction sets; single-cycle I/O port; hardware multiplier and low latency interrupt respond time. Some system peripherals listed below are also provided by Cortex®-M0+:

- Internal Bus Matrix connected with AHB-Lite Interface, Single-cycle I/O port and Debug Accesses Port (DAP)
- Nested Vectored Interrupt Controller (NVIC)
- Optional Wakeup Interrupt Controller (WIC)
- Breakpoint and Watchpoint Unit
- Optional Memory Protection Unit (MPU)
- Serial Wire debug Port (SW-DP)
- Optional Micro Trace Buffer Interface (MTB)

The following figure shows the Cortex®-M0+ processor block diagram. For more information, refer to the Arm® Cortex®-M0+ Technical Reference Manual.

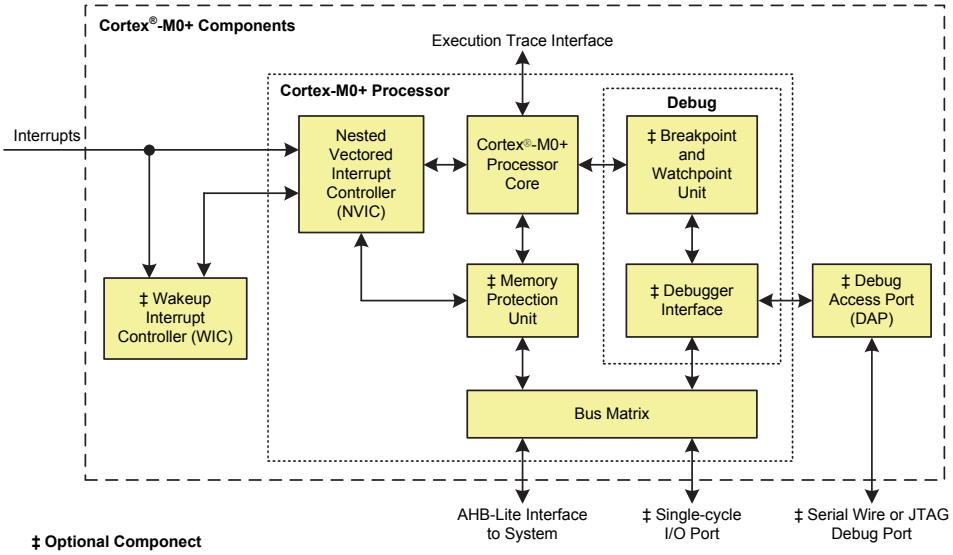


Figure 2. Cortex®-M0+ Block Diagram

Bus Architecture

The HT32F52220/HT32F52230 series consists of one master and four slaves in the bus architecture. The Cortex®-M0+ AHB-Lite bus is the master while the internal SRAM access bus, the internal Flash memory access bus, the AHB peripherals access bus and the AHB to APB bridges are the slaves. The single 32-bit AHB-Lite system interface provides simple integration to all system regions include the internal SRAM region and the peripheral region. All of the master buses are based on 32-bit Advanced High-performance Bus-Lite (AHB-Lite) protocol. The following figure shows the bus architecture of the HT32F52220/HT32F52230 series.

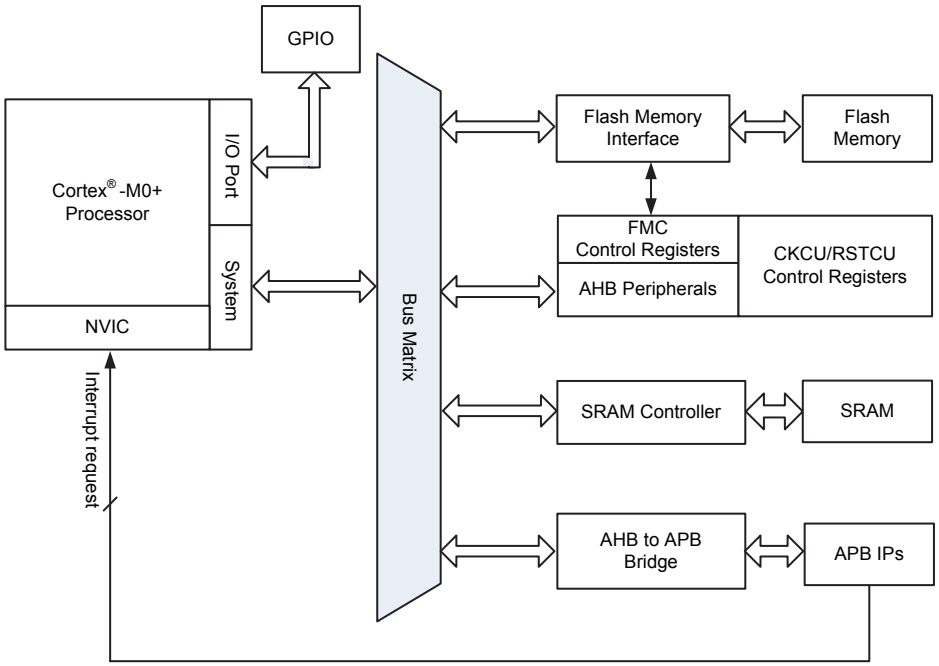


Figure 3. Bus Architecture

Memory Organization

The Arm® Cortex®-M0+ processor accesses and debug accesses share the single external interface to external AHB peripheral. The processor accesses take priority over debug accesses. The maximum address range of the Cortex®-M0+ is 4 GB since it has 32-bit bus address width. Additionally, a pre-defined memory map is provided by the Cortex®-M0+ processor to reduce the software complexity of repeated implementation of different device vendors. However, some regions are used by the Arm® Cortex®-M0+ system peripherals. Refer to the Arm® Cortex®-M0+ Technical Reference Manual for more information. The following figure shows the memory map of HT32F52220/HT32F52230 series of devices, including Code, SRAM, peripheral, and other pre-defined regions.

Memory Map

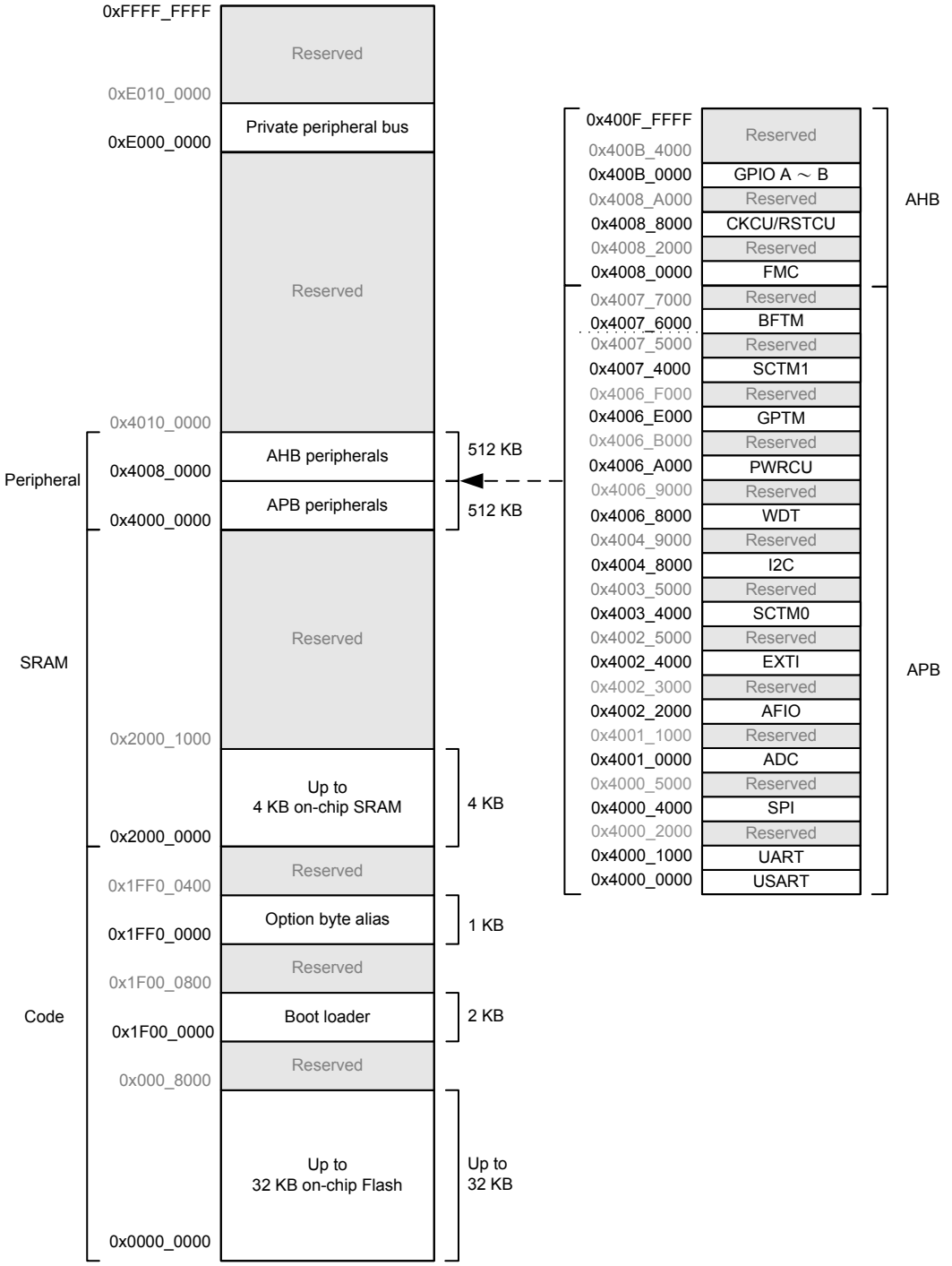


Figure 4. Memory Map

Table 3. Register Map

Start Address	End Address	Peripheral	Bus
0x4000_0000	0x4000_0FFF	USART	
0x4000_1000	0x4000_1FFF	UART	
0x4000_2000	0x4000_3FFF	Reserved	
0x4000_4000	0x4000_4FFF	SPI	
0x4000_5000	0x4001_9FFF	Reserved	
0x4001_0000	0x4001_0FFF	ADC	
0x4001_1000	0x4002_1FFF	Reserved	
0x4002_2000	0x4002_2FFF	AFIO	
0x4002_3000	0x4002_3FFF	Reserved	
0x4002_4000	0x4002_4FFF	EXTI	
0x4002_5000	0x4003_3FFF	Reserved	
0x4003_4000	0x4003_4FFF	SCTM0	
0x4003_5000	0x4004_7FFF	Reserved	APB
0x4004_8000	0x4004_8FFF	I^2C	
0x4004_9000	0x4006_7FFF	Reserved	
0x4006_8000	0x4006_8FFF	WDT	
0x4006_9000	0x4006_9FFF	Reserved	
0x4006_A000	0x4006_AFFF	PWRCU	
0x4006_B000	0x4006_DFFF	Reserved	
0x4006_E000	0x4006_EFFF	GPTM	
0x4006_F000	0x4007_3FFF	Reserved	
0x4007_4000	0x4007_4FFF	SCTM1	
0x4007_5000	0x4007_5FFF	Reserved	
0x4007_6000	0x4007_6FFF	BFTM	
0x4007_7000	0x4007_FFFF	Reserved	
0x4008_0000	0x4008_1FFF	FMC	
0x4008_2000	0x4008_7FFF	Reserved	
0x4008_8000	0x4008_9FFF	CKCU/RSTCU	
0x4008_A000	0x400A_FFFF	Reserved	AHB
0x400B_0000	0x400B_1FFF	GPIOA	
0x400B_2000	0x400B_3FFF	GPIOB	
0x400B_4000	0x400F_FFFF	Reserved	

Embedded Flash Memory

The HT32F52220/HT32F52230 series provides up to 32 KB on-chip Flash memory which is located at address 0x0000_0000. It supports byte, half-word, and word access operations. Note that the Flash memory only supports read operations for the bus access. Any write operations to the Flash memory will cause a bus fault exception. The Flash memory has up to capacity of 32 pages. Each page has a memory capacity of 1 KB and can be erased independently. A 32-bit programming interface provides the capability of changing bits from 1 to 0. A data storage or firmware upgrade can be implemented using several methods such as In System Programming (ISP), In Application Programming (IAP) or In Circuit Programming (ICP). For more information, refer to the Flash Memory Controller section.

Embedded SRAM Memory

The HT32F52220/HT32F52230 series contain up to 4 KB on-chip SRAM which is located at address 0x2000_0000. It support byte, half-word and word access operations.

AHB Peripherals

The address of the AHB peripherals ranges from 0x4008_0000 to 0x400F_FFFF. Some peripherals such as Clock Control Unit, Reset Control Unit and Flash Memory Controller are connected to the AHB bus directly. The AHB peripherals clocks are always enabled after a system reset. Access to registers for these peripherals can be achieved directly via the AHB bus. Note that all peripheral registers in the AHB bus support only word access.

APB Peripherals

The address of APB peripherals ranges from 0x4000_0000 to 0x4007_FFFF. An APB to AHB Bridge provides access capability between the CPU and the APB peripherals. Additionally, the APB peripheral clocks are disabled after a system reset. Software must enable the peripheral clock by setting the APBCCRn register in the Clock Control Unit before accessing the corresponding peripheral register. Note that the APB to AHB Bridge will duplicate the half-word or byte data to word width when a half-word or byte access is performed on the APB peripheral registers. In other words, the access result of a half-word or byte access on the APB peripheral register will vary depending on the data bit width of the access operation on the peripheral registers.

4 Flash Memory Controller (FMC)

Introduction

The Flash Memory Controller, FMC, provides all the necessary flash operation functions and pre-fetch buffer for the embedded on-chip Flash memory. Figure below shows the block diagram of the FMC which includes programming interface, control register, pre-fetch buffer and access interface. Since the Flash memory access speed is slower than the CPU, a wide access interface with the pre-fetch buffer is provided to the Flash memory in order to reduce the CPU waiting time which will cause the CPU instruction execution delays. The Flash memory word program and page erase functions are also provided for instruction/data storage.

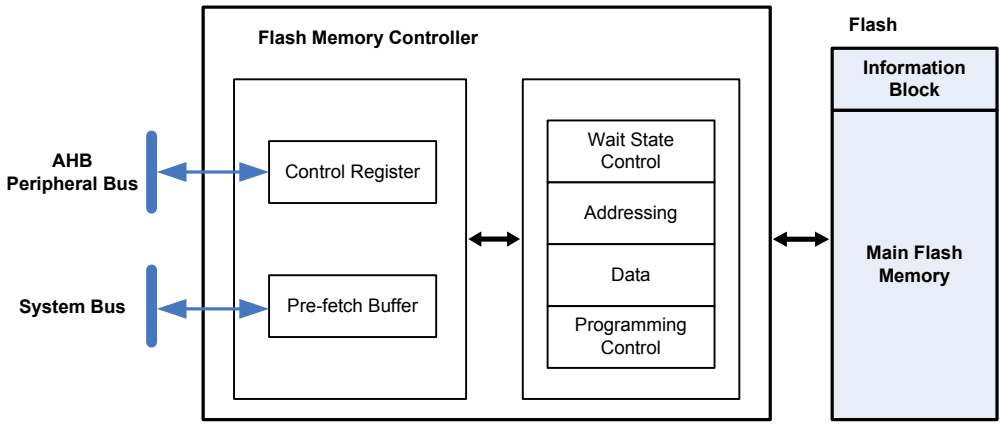


Figure 5. Flash Memory Controller Block Diagram

Features

- Up to 32 KB of on-chip Flash memory for storing instruction/data and options
  - 32 KB (instruction/data + Option Byte)
  - 16 KB (instruction/data + Option Byte)
- Page size of 1K Byte, totally up to 32 pages depending on the main Flash size
- Wide access interface with pre-fetch buffer to reduce instruction execution delay
- Page erase and mass erase capability
- 32-bit word programming
- Interrupt function to indicate the end of Flash memory operation or an error occurs
- Flash read protection to prevent illegal code/data access
- Page erase/program protection to prevent unexpected operation

Functional Descriptions

Flash Memory Map

The following figure is the Flash memory map of the system. The address ranges from 0x0000_0000 to 0x1FFF_FFFF (0.5 GB). The address from 0x1F00_0000 to 0x1F00_07FF is mapped to Boot Loader Block (2 KB). Additionally, the region addressed from 0x1FF0_0000 to 0x1FF0_03FF is the alias of Option Byte block (1 KB) which is located at the last page of the main Flash physically. The memory mapping on system view is shown as below.

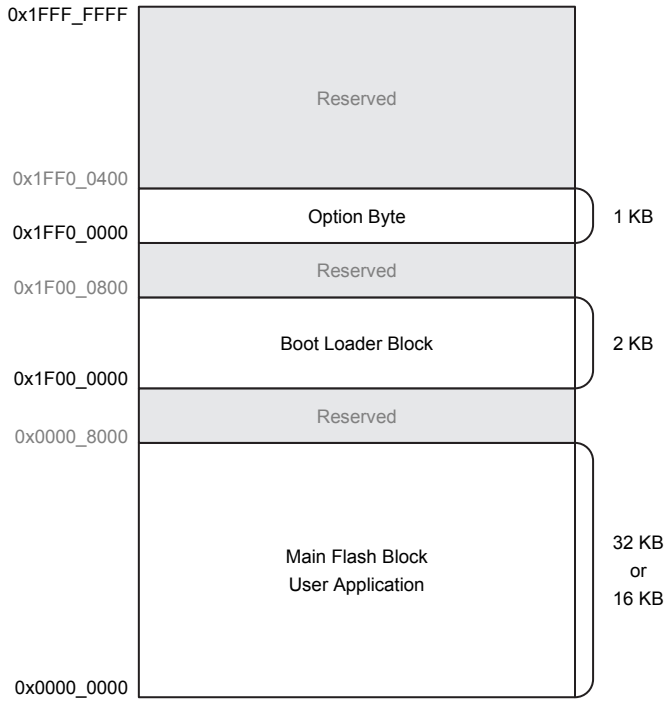


Figure 6. Flash Memory Map

Flash Memory Architecture

The Flash memory consists of up to 32 KB main Flash with 1 KB per page and 2 KB Information Block for Boot Loader. The main Flash memory contains a total of 32 pages (or 16 pages for 16 KB device) which can be erased individually. The following table shows the base address, size and protection setting bit of each page.

Table 4. Flash Memory and Option Byte

Block	Name	Address	Page Protection Bit	Size
Main Flash Block	Page 0	0x0000_0000 ~ 0x0000_03FF	OB_PP [0]	1 KB
	Page 1	0x0000_0400 ~ 0x0000_07FF	OB_PP [1]	1 KB
	Page 2	0x0000_0800 ~ 0x0000_0BFF	OB_PP [2]	1 KB
	Page 3	0x0000_0C00 ~ 0x0000_0FFF	OB_PP [3]	1 KB
	⋮	⋮	⋮	⋮
	Page 28	0x0000_7000 ~ 0x0000_73FF	OB_PP [28]	1 KB
	Page 29	0x0000_7400 ~ 0x0000_77FF	OB_PP [29]	1 KB
	Page 30	0x0000_7800 ~ 0x0000_7BFF	OB_PP [30]	1 KB
	Page 31 (Option Byte)	Physical:0x0000_7C00 ~ 0x0000_7FFF Alias: 0x1FF0_0000 ~ 0x1FF0_03FF	OB_CP [1]	1 KB
Information Block	Boot Loader	0x1F00_0000 ~ 0x1F00_07FF	NA	2 KB

Notes: 1. The Information Block stores boot loader – this block can not be programmed or erased by user.
2. The Option Byte is always located at last page of main Flash block.

Wait State Setting

When the CPU clock, HCLK, is greater than the access speed of the Flash memory, the wait state cycles must be inserted during the CPU fetch instructions or load data from Flash memory. The wait state can be changed by setting the WAIT [2:0] of the Flash Cache and Pre-fetch Control Register, CFCR. In order to match the wait state requirement, the following two rules should be considered.

- HCLK clock is switched from low speed to high speed frequency:
  Change the wait state setting first and then switch the HCLK clock.
- HCLK clock is switched from high speed to low speed frequency:
  Switch the HCLK clock first and then change the wait state setting.

The following table shows the relationship between the wait state cycle and HCLK. The default wait state is 0 since the High Speed Internal oscillator, HSI, which operates at a frequency of 8MHz is selected as the HCLK clock source after system reset.

Table 5. Relationship between Wait State Cycle and HCLK

Wait State Cycle	HCLK
0	0 MHz < HCLK ≤ 20 MHz
1	20 MHz < HCLK ≤ 40 MHz

Booting Configuration

The system provides two kinds of boot modes which can be selected using the BOOT pin. The BOOT pin is sampled during a power-on reset or system reset. Once the logic value is decided, the first 4 words of vector will be remapped to the corresponding source according to the boot modes. The boot mode is shown in the following table.

Table 6. Boot Modes

Boot modes selection pin	Mode	Descriptions
BOOT		
0	Boot Loader	The Vector source is Boot Loader
1	Main Flash	The Vector source is main Flash

The Vector Mapping Control Register, VMCR, is provided to change the vector remapping setting temporarily after the chip reset. The reset initial value of the VMCR register is determined by the BOOT pin status which will be sampled during the reset duration.

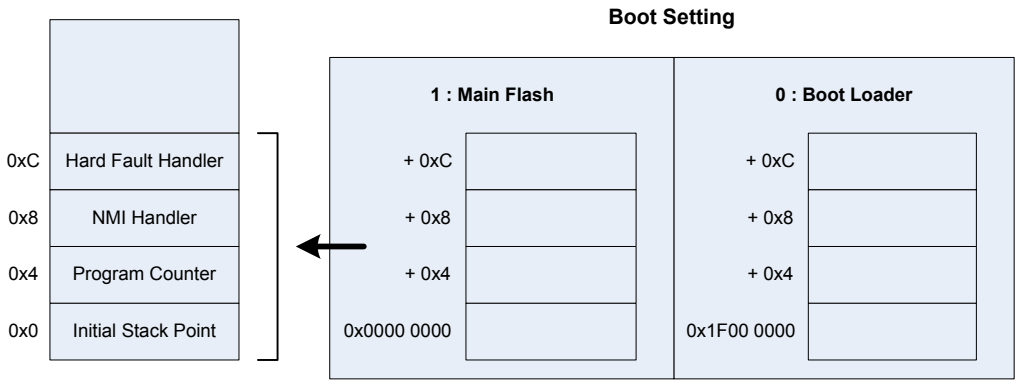


Figure 7. Vector Remapping

Page Erase

The FMC provides a page erase function which is used to initialize the contents of the specific Flash memory page. Each page can be erased independently without affecting the contents of other pages. The following steps show the access sequence of the register for a page erase operation.

- Check the OPCR register to confirm that no Flash memory operation is in progress (OPM [3:0] equal to 0xE or 0x6). Otherwise, wait until the previous operation has been finished.
- Write the page address to the TADR register.
- Write the page erase command to the OCMR register (CMD [3:0] = 0x8).
- Commit the page erase command to the FMC by setting the OPCR register (set OPM [3:0]=0xA).
- Wait until all the operations have been completed by checking the OPCR register value (OPM [3:0] equals to 0xE).
- Read and verify the page if required.

Note that a correct target page address must be confirmed. The software may run out of control if the target erase page is being used to fetch code or access data. The FMC will not provide any notification when this happens. Additionally, the page erase operation will be ignored on the protected pages. A Flash Operation Error interrupt will be triggered by the FMC if the OREIEN bit in the OIER register is set. The software can check the PPEF bit in the OISR register to detect this condition in the interrupt handler. The following figure shows the page erase operation flow.

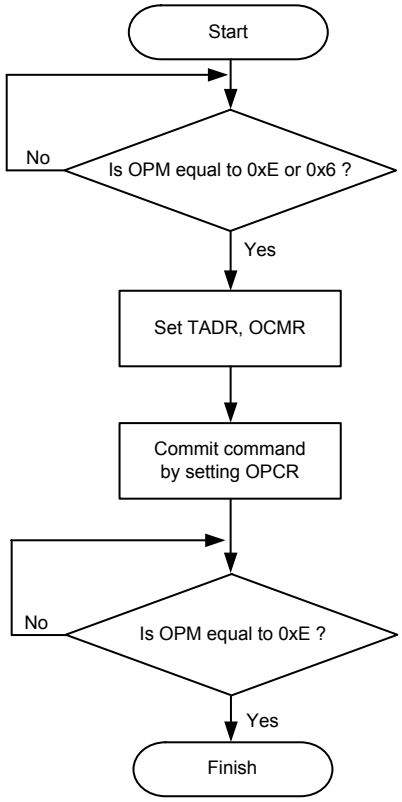


Figure 8. Page Erase Operation Flowchart

Mass Erase

The FMC provides a mass erase function which is used to initialize all the main Flash memory contents to a high state. The following steps show the mass erase operation register access sequence.

- Check the OPCR register to confirm that no Flash memory operation is in progress (OPM [3:0] equal to 0xE or 0x6). Otherwise, wait until the previous operation has been finished.
- Write the mass erase command to the OCMR register (CMD [3:0] = 0xA).
- Commit the mass erase command to the FMC by setting the OPCR register (set OPM [3:0]=0xA).
- Wait until all operations have been finished by checking the value of the OPCR register (OPM [3:0] equals to 0xE).
- Read and verify the Flash memory if required.

Since all Flash data will be reset as 0xFFFF_FFFF, the mass erase operation can be implemented by the program that runs in the SRAM or by the debugging tool that access the FMC register directly. The software function that is executed on the Flash memory should not trigger a mass erase operation. The following figure shows the mass erase operation flow.

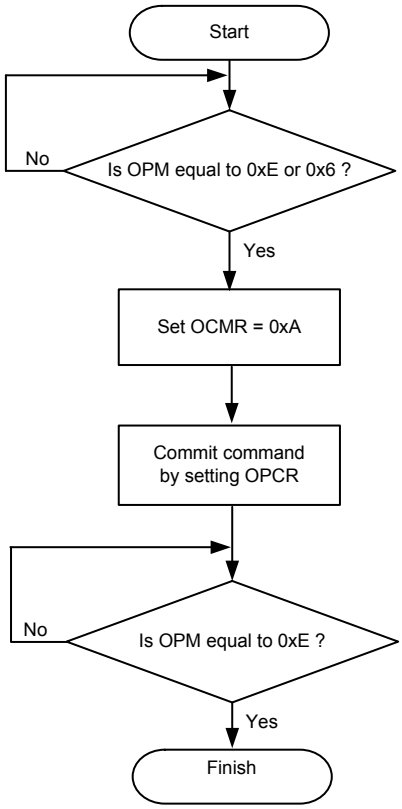


Figure 9. Mass Erase Operation Flowchart

Word Programming

The FMC provides a 32-bit word programming function which is used to modify the specific Flash memory word contents. The following steps show the word programming operation register access sequence.

- Check the OPCR register to confirm that no Flash memory operation is in progress (OPM [3:0] equal to 0xE, or 0x6). Otherwise, wait until the previous operation has been finished.
- Write the word address to the TADR register. Write the word data to the WRDR register.
- Write the word program command to the OCMR register (CMD [3:0] = 0x4).
- Commit the word program command to the FMC by setting the OPCR register (set OPM [3:0]=0xA).
- Wait until all operations have been finished by checking the value of the OPCR register (OPM [3:0] equals to 0xE).
- Read and verify the Flash memory if required.

Note that the word programming operation can not be applied to the same address twice. Successive word programming operations to the same address must be separated by a page erase operation. Additionally, the word programming operation will be ignored on protected pages. A Flash operation error interrupt will be triggered by the FMC if the OREIEN bit in the OIER register is set. The software can check the PPEF bit in the OISR register to detect this condition in the interrupt handler. The following figure shows the word programming operation flow.

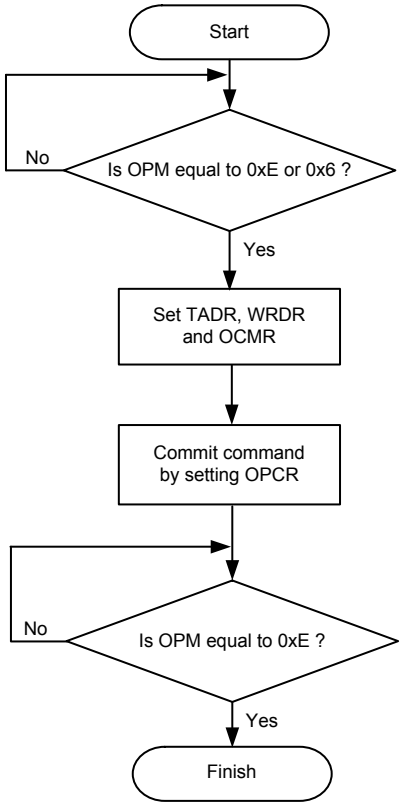


Figure 10. Word Programming Operation Flowchart

Option Byte Description

The Option Byte region can be treated as an independent Flash memory in which the base address is 0x1FF0_0000. The following table shows the functional description and the Option Byte memory map.

Table 7. Option Byte Memory Map

Option Byte	Offset	Description	Reset Value
Option Byte Base Address = 0x1FF0_0000			
OB_PP	0x000 0x004 0x008 0x00C	OB_PP [n]: Flash Page Erase/Program Protection (n = 0 ~ 127) OB_PP [n] (n = 0 ~ 30) 0: Flash Page n Erase / Program Protection is enabled 1: Flash Page n Erase / Program Protection is disabled OB_PP [n] (n = 31 ~ 127) Reserved	0xFFFF_FFFF 0xFFFF_FFFF 0xFFFF_FFFF 0xFFFF_FFFF
OB_CP	0x010	OB_CP [0]: Flash Security Protection 0: Flash Security protection is enabled 1: Flash Security protection is disabled OB_CP [1]: Option Byte Protection 0: Option Byte protection is enabled 1: Option Byte protection is disabled OB_CP [31:2]: Reserved	0xFFFF_FFFF
OB_CK	0x020	OB_CK [31:0]: Flash Option Byte Checksum OB_CK should be set as the sum of the 5 words Option Byte contents, of which the offset address is from 0x000 to 0x010 (0x000 + 0x004 + 0x008 + 0x00C + 0x010), when the OB_PP or OB_CP register content is not equal to 0xFFFF_FFFF. Otherwise, both page erase/program protection and security protection will be enabled.	0xFFFF_FFFF

Page Erase/Program Protection

The FMC provides the page erase/program protection function to prevent unexpected operation of the Flash memory. The page erase (CMD [3:0] = 0x8 in the OCMR register) or word program (CMD [3:0] = 0x4) command will not be accepted by the FMC on the protected pages. When the page erase or word programming command is sent to the FMC on a protected page, the PPEF bit in the OISR register will then be set by the FMC and the Flash operation error interrupt will be triggered to the CPU by the FMC if the OREIEN bit in the OIER register is set. The page protection function can be enabled for each page independently by setting the OB_PP registers in the Option Byte. The following table shows the access permission of the main Flash page when the page protection is enabled.

Table 8. Access Permission of Protected Main Flash Page

Mode / Operation	ISP/IAP	ICP/Debug mode
Read	O	O
Program	X	X
Page Erase	X	X
Mass Erase	O	O

Notes: 1. The write protection is based on specific pages. The above access permission only affects the pages of which the protection function has been enabled. Other pages are not affected.
2. The Main Flash page protection is configured by the OB_PP [126:0] field. The Option Byte is physically located at the last page of the main Flash. The Option Byte page protection is configured by the OB_CP [1] bit.
3. The page erase on the Option Byte area can be used to disable the page protection of the main Flash.
4. The page protection of the Option Byte can only be disabled by a mass erase operation.

The following steps show the page erase/program protection register access sequence.

- Check the OPCR register to confirm that no Flash memory operation is in progress (OPM [3:0] equal to 0xE or 0x6). Otherwise, wait until the previous operation has been finished.
- Write the OB_PP address to the TADR register (TADR = 0x1FF0_0000).
- Write the WRDR register, which indicates the protection function of corresponding page is enabled or disabled (0: Enabled, 1: Disabled).
- Write the word program command to the OCMR register (CMD [3:0] = 0x4).
- Commit the word program command to the FMC by setting the OPCR register (set OPM [3:0] = 0xA).
- Wait until all operations have been finished by checking the value of the OPCR register (OPM [3:0] equals to 0xE).
- Read and verify the Option Byte if required.
- The OB_CK field in the Option Byte must be updated according to the Option Byte checksum rule.
- Apply a system reset to activate the new OB_PP setting.

Security Protection

The FMC provides a Security protection function to prevent an illegal code/data access of the Flash memory. This function is useful for protecting the software / firmware from the illegal users. The function is activated by configuring the Option Byte OB_CP [0] bit. Once the function has been enabled, all the main Flash data access through ICP/Debug mode, programming and page erase operation will not be allowed except via the user's application. However, the mass erase operation will still be accepted by the FMC in order to disable this security protection function. The following table shows the access permission of the Flash memory when the security protection is enabled.

Table 9. Access Permission When Security Protection is Enabled

Mode / Operation	User application (Note 1)	ICP/Debug mode
Read	O	X (read as 0)
Program	O (Note 1)	X
Page Erase	O (Note 1)	X
Mass Erase	O	O

Notes: 1. User application means the software that is executed or booted from the main Flash memory with the JTAG/SW debugger being disconnected. However, the Option Byte block and page 0 are still in protection and the Program/Page Erase operation cannot be executed.

2. The Mass erase operation can erase the Option Byte block and disable the security protection.

The following steps show the security protection register access sequence:

- Check the OPCR register to confirm that no Flash memory operation is in progress (OPM [3:0] equal to 0xE or 0x6). Otherwise, wait until the pervious operation has been finished.
- Write the OB_CP address to the TADR register (TADR = 0x1FF0_0010).
- Write the data into the WRDR register to set the OB_CP [0] field to 0.
- Write the word program command to the OCMR register (CMD [3:0] = 0x4).
- Commit the word program command to the FMC by setting the OPCR register (set OPM = 0xA).
- Wait until all operations have been finished by checking the value of the OPCR register (OPM [3:0] equals to 0xE).
- Read and verify the Option Byte if required.
- The OB_CK field in the Option Byte must be updated according to the Option Byte checksum rule.
- Apply a system reset to active the new OB_CP setting.

Register Map

The following table shows the FMC registers and reset values.

Table 10. FMC Register Map

Register	Offset	Description	Reset Value
FMC Base Address = 0x4008_0000			
TADR	0x000	Flash Target Address Register	0x0000_0000
WRDR	0x004	Flash Write Data Register	0x0000_0000
OCMR	0x00C	Flash Operation Command Register	0x0000_0000
OPCR	0x010	Flash Operation Control Register	0x0000_000C
OIER	0x014	Flash Operation Interrupt Enable Register	0x0000_0000
OISR	0x018	Flash Operation Interrupt and Status Register	0x0001_0000
PPSR	0x020 0x024 0x028 0x02C	Flash Page Erase/Program Protection Status Register	0xXXXX_XXXX 0xXXXX_XXXX 0xXXXX_XXXX 0xXXXX_XXXX
CPSR	0x030	Flash Security Protection Status Register	0xXXXX_XXXX
VMCR	0x100	Flash Vector Mapping Control Register	0x0000_000X
MDID	0x180	Flash Manufacturer and Device ID Register	0x0376_XXXX
PNSR	0x184	Flash Page Number Status Register	0x0000_00X0
PSSR	0x188	Flash Page Size Status Register	0x0000_0400
CFCR	0x200	Flash Pre-fetch Control Register	0x0000_0011
CIDR0	0x310	Custom ID Register 0	0xXXXX_XXXX
CIDR1	0x314	Custom ID Register 1	0xXXXX_XXXX
CIDR2	0x318	Custom ID Register 2	0xXXXX_XXXX
CIDR3	0x31C	Custom ID Register 3	0xXXXX_XXXX

Note: "X" means various reset values which depend on the Device, Flash value, Option Byte value, or power on reset setting.

Register Descriptions

Flash Target Address Register – TADR

This register specifies the target address of the page erase and word programming operations.

Offset: 0x000

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	TADB							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	TADB							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	TADB							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	TADB							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[31:0]	TADB	Flash Target Address Bits For programming operations, the TADR register specifies the address where the data is written. Since the programming length is 32-bit, the TADR should be set as word-aligned (4 bytes). The TADB [1:0] bits will be ignored during programming operations. For page erase operations, the TADR register contains the page address which is going to be erased. Since the page size is 1 KB, the TADB [9:0] bits will be ignored in order to limit the target address as 1 Kbyte-aligned. For 32 KB main Flash addressing, the TADB [31:16] bits should be zero while the TADB [31:15] bits should be zero for 16 KB main Flash addressing. The region of which the address ranges from 0x1FF0_0000 to 0x1FF0_03FF is the 1KB Option Byte. This field for the available Flash address must be under 0x1FFF_FFFF. Otherwise, the Invalid Target Address interrupt will occur if the corresponding interrupt enable bit is set.

Flash Write Data Register – WRDR

This register specifies the data to be written for programming operation.

Offset: 0x004

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	WRDB							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	23	22	21	20	19	18	17	16
	WRDB							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
	WRDB							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	WRDB							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[31:0]	WRDB	Flash Write Data Bits The data value for programming operation.

Flash Operation Command Register – OCMR

This register is used to specify the Flash operation commands that include word program, page erase and mass erase.

Offset: 0x00C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved				CMD			
Type/Reset					RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[3:0]	CMD	Flash Operation Command The following table shows the definitions of the operation command bits, CMD [3:0], which specify the Flash memory operation. If an invalid command is set and the IOCMIEN bit is set to 1, an Invalid Operation Command interrupt will occur.

CMD [3:0]	Description
0x0	Idle (default)
0x4	Word program
0x8	Page erase
0xA	Mass erase
Others	Reserved

Flash Operation Control Register – OPCR

This register is used for controlling the command commitment and checking the status of the FMC operations.

Offset: 0x010

Reset value: 0x0000_000C

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved			OPM				Reserved
Type/Reset				RW 0	RW 1	RW 1	RW 0	

Bits	Field	Descriptions
[4:1]	OPM	Operation Mode The following table shows the operation modes of the FMC. User can commit the command which is set by the OCMR register to the FMC according to the address alias setting in the TADR register. The contents of the TADR, WRDR, and OCMR registers should be prepared before setting this register. After all the operations have been finished, the OPM field will be set as 0xE by the FMC hardware. The Idle mode can be set when all the operations have been finished for power saving purpose. Note that the operation status should be checked before the next operation is executed to the FMC. The contents of the TADR, WRDR, OCMR, and OPCR registers should not be changed until the previous operation has been finished.

OPM [3:0]	Description
0x6	Idle (default)
0xA	Commit command to main Flash
0xE	All operation finished on main Flash
Others	Reserved

Flash Operation Interrupt Enable Register – OIER

This register is used to enable or disable the FMC interrupt function. The FMC generates interrupts to the controller when corresponding interrupt enable bits are set.

Offset: 0x014

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								

	7	6	5	4	3	2	1	0
	Reserved			OREIEN	IOCMIEN	OBEIEN	ITADIEN	ORFIEN
Type/Reset				RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[4]	OREIEN	Operation Error Interrupt Enable 0: Operation error interrupt is disabled 1: Operation error interrupt is enabled
[3]	IOCMIEN	Invalid Operation Command Interrupt Enable 0: Invalid Operation Command interrupt is disabled 1: Invalid Operation Command interrupt is enabled
[2]	OBEIEN	Option Byte Check Sum Error Interrupt Enable 0: Option Byte Check Sum Error interrupt is disabled 1: Option Byte Check Sum Error interrupt is enabled
[1]	ITADIEN	Invalid Target Address Interrupt Enable 0: Invalid Target Address interrupt is disabled 1: Invalid Target Address interrupt is enabled
[0]	ORFIEN	Operation Finished Interrupt Enable 0: Operation Finish interrupt is disabled 1: Operation Finish interrupt is enabled

Flash Operation Interrupt and Status Register – OISR

This register indicates the FMC interrupt status which is used to check if a Flash operation has been finished or an error occurs. The status bits, bit [4:0], are available when the corresponding bits in the OIER register are set.

Offset: 0x018

Reset value: 0x0001_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved						PPEF	RORFF
Type/Reset							RO 0	RO 1
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved			OREF	IOCMF	OBEF	ITADF	ORFF
Type/Reset				WC 0	WC 0	WC 0	WC 0	WC 0

Bits	Field	Descriptions
[17]	PPEF	Page Erase/Program Protected Error Flag 0: Page Erase/Program Protected Error does not occur 1: Operation error occurs due to an invalid erase/program operation applied to a protected page This bit is reset by hardware once a new flash operation command is committed.
[16]	RORFF	Raw Operation Finished Flag 0: The last flash operation command is not finished 1: The last flash operation command is finished The RORFF bit is directly connected to the Flash memory for debugging purpose.
[4]	OREF	Operation Error Flag 0: No Flash operation error occurred 1: The last flash operation is failed This bit will be set when any Flash operation error occurs such as an invalid command, program error and erase error, etc. The ORE interrupt occurs if the OREIEN bit in the OIER register is set. Reset this bit by writing 1.
[3]	IOCMF	Invalid Operation Command Flag 0: No invalid flash operation command was set 1: An invalid flash operation command has been written into the OCMR register The IOCM interrupt will occur if the IOCMIEN bit in the OIER register is set. Reset this bit by writing 1.
[2]	OBEF	Option Byte Checksum Error Flag 0: Option Byte checksum is correct 1: Option Byte checksum is incorrect The OBE interrupt will occur if the OBEIEN bit in the OIER register is set. This bit is cleared to 0 by software writing 1 into it. However, the Option Byte Checksum Error Flag can not be cleared by software until the interrupt condition is cleared, which means that the Option Byte check sum value has to be correctly modified or the corresponding interrupt control is disabled. Otherwise, the interrupt will be continually generated.

Bits	Field	Descriptions
[1]	ITADF	Invalid Target Address Flag 0: The target address is valid 1: The target address is invalid The data in the TADR field must be in the range from 0x0000_0000 to 0x1FFF_FFFF. Otherwise, an ITAD interrupt will occur if the ITADIEN bit in the OIER register is set. Reset this bit by writing 1.
[0]	ORFF	Operation Finished Flag 0: No flash operation is finished 1: Last Flash operation is finished The ORF interrupt will occur if the ORFIEN bit in the OIER register is set. Reset this bit by writing 1.

Flash Page Erase/Program Protection Status Register – PPSR

This register indicates the page protection status of the Flash page erase/program protection functions.

Offset: 0x020 (0) ~ 0x02C (3)

Reset value: 0xXXXX_XXXX

	31	30	29	28	27	26	25	24
	PPSBn							
Type/Reset	RO X	RO X	RO X	RO X	RO X	RO X	RO X	RO X
	23	22	21	20	19	18	17	16
	PPSBn							
Type/Reset	RO X	RO X	RO X	RO X	RO X	RO X	RO X	RO X
	15	14	13	12	11	10	9	8
	PPSBn							
Type/Reset	RO X	RO X	RO X	RO X	RO X	RO X	RO X	RO X
	7	6	5	4	3	2	1	0
	PPSBn							
Type/Reset	RO X	RO X	RO X	RO X	RO X	RO X	RO X	RO X

Bits	Field	Descriptions
[127:0]	PPSBn	Page Erase/Program Protection Status Bits (n = 0 ~ 127) PPSB[n] = OB_PP[n] 0: The corresponding page n is protected 1: The corresponding page n is not protected The content of this register is not dynamically updated and will only be reloaded from the Option Byte when any kind of reset occurs. The erase or program function of the specific page is not allowed when the corresponding bits of the PPSR registers are reset. The reset value of PPSR [127:0] is determined by the Option Byte OB_PP [127:0] bits. Each page erase/program protection status bit protects one page. The other remained bits of the OB_PP field and PPSR registers are reserved.

Flash Security Protection Status Register – CPSR

This register indicates the Flash Memory Security protection status. The content of this register is not dynamically updated and will only be reloaded by the Option Byte loader which is active when any kind of reset occurs.

Offset: 0x030

Reset value: 0xXXXX_XXXX

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved						OBPSB	CPSB
Type/Reset							RO X	RO X

Bits	Field	Descriptions
[1]	OBPSB	Option Byte Page Erase/Program Protection Status Bit 0: The Option Byte page is protected 1: The Option Byte page is not protected The reset value of the OPBSB bit is determined by the Option Byte OB_CP [1] bit.
[0]	CPSB	Flash Memory Security Protection Status Bit 0: Flash Memory Security protection is enabled 1: Flash Memory Security protection is not enabled The reset value of the CPSB bit is determined by the Option Byte OB_CP [0] bit.

Flash Vector Mapping Control Register – VMCR

This register is used to control the vector mapping. The reset value of the VMCR register is determined by the external BOOT pin during the power-on reset period.

Offset: 0x100

Reset value: 0x0000_000X

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved						VMCB	Reserved
Type/Reset							RW	X

Bits	Field	Descriptions
[1]	VMCB	Vector Mapping Control Bit The VMCB bit is used to control the mapping source of the first 4-word vectors addressed from 0x0 to 0xC. The following table shows the vector mapping setting.

BOOT	VMCB [1]	Descriptions
Low	0	Boot Loader mode The vector mapping source is the boot loader area.
High	1	Main Flash mode The vector mapping source is the main Flash area.

The reset value of the VMCB bit is determined by the BOOT pin status during the power-on reset and system reset. The vector mapping setting can be changed temporarily by configuring the VMCB bit when the application program is executed.

Flash Manufacturer and Device ID Register – MDID

This register is used to store the manufacture ID and device part number information which can be used as the product identity.

Offset: 0x180

Reset value: 0x0376_xxxx

	31	30	29	28	27	26	25	24
	MFID							
Type/Reset	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 1	RO 1
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	MFID							
Type/Reset	RO 0	RO 1	RO 1	RO 1	RO 0	RO 1	RO 1	RO 0
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	ChipID							
Type/Reset	RO X	RO X	RO X	RO X	RO X	RO X	RO X	RO X
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	ChipID							
Type/Reset	RO X	RO X	RO X	RO X	RO X	RO X	RO X	RO X

Bits	Field	Descriptions
[31:16]	MFID	Manufacturer ID Read as 0x0376
[15:0]	ChipID	Chip ID Read the last 4 digital codes of the MCU device part number.

Flash Page Number Status Register – PNSR

This register is used to indicate the Flash memory page number.

Offset: 0x184

Reset value: 0x0000_00XX

	31	30	29	28	27	26	25	24
	PNSB							
Type/Reset	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	PNSB							
Type/Reset	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PNSB							
Type/Reset	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	PNSB							
Type/Reset	RO X	RO X	RO X	RO X	RO X	RO X	RO X	RO X

Bits	Field	Descriptions
[31:0]	PNSB	Flash Page Number Status Bits 0x0000_0010: Totally 16 pages for the on-chip Flash memory device 0x0000_0020: Totally 32 pages for the on-chip Flash memory device 0x0000_0040: Totally 64 pages for the on-chip Flash memory device 0x0000_0080: Totally 128 pages for the on-chip Flash memory device 0x0000_00FF: Totally 255 pages for the on-chip Flash memory device

Flash Page Size Status Register – PSSR

This register is used to indicate the page size in bytes.

Offset: 0x188

Reset value: 0x0000_0400

	31	30	29	28	27	26	25	24
	PSSB							
Type/Reset	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	PSSB							
Type/Reset	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PSSB							
Type/Reset	RO 0	RO 0	RO 0	RO 0	RO 0	RO 1	RO 0	RO 0
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	PSSB							
Type/Reset	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0

Bits	Field	Descriptions
[31:0]	PSSB	Flash Page Size Status Bits 0x200: The page size is 512 Bytes per page 0x400: The page size is 1 KB per page 0x800: The page size is 2 KB per page

Device ID Register – DID

This register is used to store the device part number information which can be used as the product identity.

Offset: 0x18C

Reset value: 0x000X_XXXX

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved				ChipID			
Type/Reset					RO X	RO X	RO X	RO X
	15	14	13	12	11	10	9	8
	ChipID							
Type/Reset	RO X	RO X	RO X	RO X	RO X	RO X	RO X	RO X
	7	6	5	4	3	2	1	0
	ChipID							
Type/Reset	RO X	RO X	RO X	RO X	RO X	RO X	RO X	RO X

Bits	Field	Descriptions
[19:0]	ChipID	Chip ID Read the complete 5 digital codes of the MCU device part number.

Flash Pre-fetch Control Register – CFCR

This register is used to control the FMC pre-fetch module.

Offset: 0x200

Reset value: 0x0000_0011

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved			PFBE	Reserved	WAIT		
Type/Reset				RW 1		RW 0	RW 0	RW 1

Bits	Field	Descriptions
[4]	PFBE	Pre-fetch Buffer Enable Bit 0: Pre-fetch buffer is disabled 1: Pre-fetch buffer is enabled (default) The pre-fetch buffer is enabled in default. When the pre-fetch buffer is disabled, the instruction and data are directly provided by the Flash memory.
[2:0]	WAIT	Flash Wait State Setting The WAIT[2:0] field is used to set the HCLK wait clock during a non-sequential address Flash access. The actual wait clock is given by (WAIT[2:0] - 1). Since a wide access interface with a pre-fetch buffer is provided, the wait state of sequential Flash access is very close to zero.

WAIT [2:0]	Wait Status	Allowed HCLK Range
001	0	0 MHz < HCLK ≤ 20 MHz
010	1	20 MHz < HCLK ≤ 40 MHz
Others	Reserved	Reserved

Custom ID Register n – CIDRn (n = 0 ~3)

This register is used to store the custom ID information which can be used as the custom identity.

Offset: 0x310 (0) ~ 0x31C (3)

Reset value: Various depending on Flash Manufacture Privilege Information Block.

	31	30	29	28	27	26	25	24
	CID							
Type/Reset	RO X	RO X	RO X	RO X	RO X	RO X	RO X	RO X
	23	22	21	20	19	18	17	16
	CID							
Type/Reset	RO X	RO X	RO X	RO X	RO X	RO X	RO X	RO X
	15	14	13	12	11	10	9	8
	CID							
Type/Reset	RO X	RO X	RO X	RO X	RO X	RO X	RO X	RO X
	7	6	5	4	3	2	1	0
	CID							
Type/Reset	RO X	RO X	RO X	RO X	RO X	RO X	RO X	RO X

Bits	Field	Descriptions
[31:0]	CIDn	Custom ID Read as the CIDn[31:0] (n=0 ~ 3) field in the Custom ID registers in Flash Manufacture Privilege Block.

5 Power Control Unit (PWRCU)

Introduction

The power consumption can be regarded as one of the most important issues for many embedded system applications. Accordingly the Power Control Unit, PWRCU, provides many types of power saving modes such as Sleep, Deep-Sleep1, Deep-Sleep2, and Power-Down modes. These modes reduce the power consumption and allow the application to achieve the best trade-off between the conflicting demands of CPU operating time, speed and power consumption. The dash line in the Figure 11 indicates the power supply source of two digital power domains.

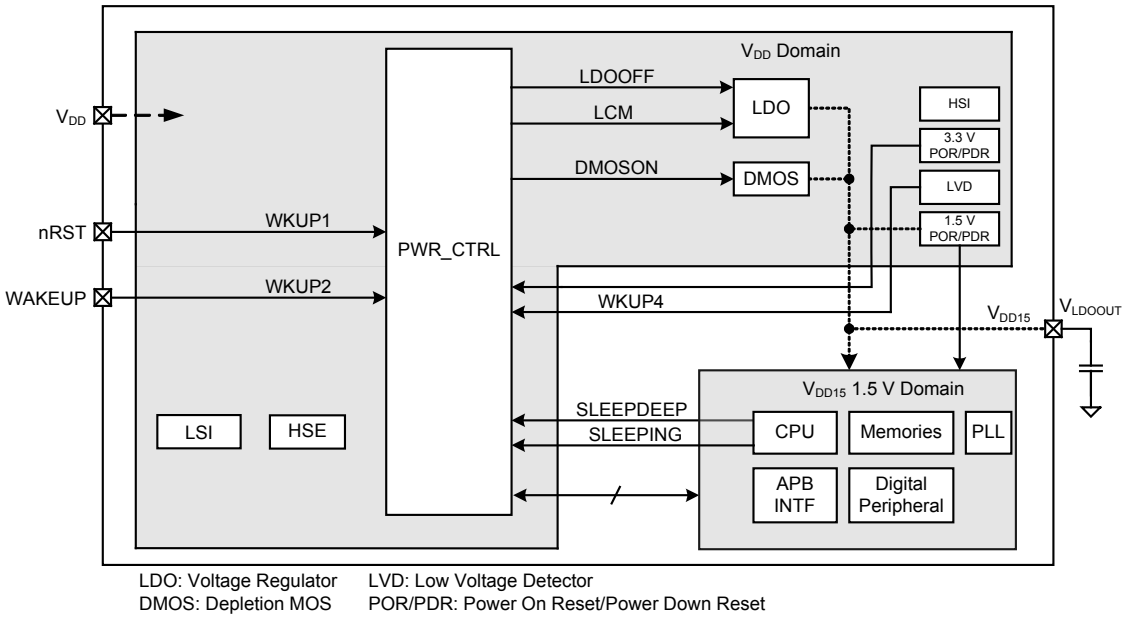


Figure 11. PWRCU Block Diagram

Features

- Two power domains: V_{DD} 3.3 V and V_{DD15} 1.5 V power domains.
- Four power saving modes: Sleep, Deep-Sleep1, Deep-Sleep2 and Power-Down modes.
- Internal Voltage regulator supplies 1.5 V voltage source.
- Additional Depletion MOS supplies 1.5 V voltage source with low leakage and low operating current.
- A power reset is generated when one of the following events occurs:
  - Power-on / Power-down reset (POR / PDR reset).
  - When exiting Power-Down mode.
  - The control bits BODEN = 1, BODRIS=0 and the supply power $V_{DD} \leq V_{BOD}$.
- BOD Brown Out Detector can issue a system reset or an interrupt when V_{DD} power source is lower than the Brown Out Detector voltage V_{BOD}.
- LVD Low Voltage Detector can issue an interrupt or wakeup event when V_{DD} is lower than a programmable threshold voltage V_{LVD}.

Functional Descriptions

V_{DD} Power Domain

LDO Power Control

The LDO will be automatically switched off when one of the following conditions occurs:

- The Power-Down or Deep-Sleep 2 mode is entered.
- The control bits BODEN = 1, BODRIS = 0 and the supply power $V_{DD} \leq V_{BOD}$.
- The supply power $V_{DD} \leq V_{PDR}$

The LDO will be automatically switched on by hardware when the supply power $V_{DD} > V_{POR}$ if any of the following conditions occurs:

- Resume operation from the power saving mode – LVD wakeup and WAKEUP pin rising edge.
- Detect a falling edge on the external reset pin (nRST).
- The control bit BODEN = 1 and the supply power $V_{DD} > V_{BOD}$.

To enter the Deep-Sleep1 mode, the PWRCU will request the LDO to operate in a low current mode, LCM. To enter the Deep-Sleep 2 mode, the PWRCU will turn off the LDO and turn on the DMOS to supply an alternative 1.5 V power.

Voltage Regulator

The voltage regulator, LDO, Depletion MOS, DMOS, Low voltage Detector, LVD, High Speed Internal oscillator, HSI, and Low Speed Internal RC oscillator, LSI, are operated under the V_{DD} power domain. The LDO can be configured to operate in either normal mode (LDOOFF = 0, LDOLCM = 0, I_{OUT} = High current mode) or low current mode (LDOOFF = 0, LDOLCM =1, I_{OUT} = Low current mode) to supply the 1.5 V power. An alternative 1.5 V power source is the output of the DMOS which has low static and driving current characteristics. It is controlled using the DMOSON bit in the PWRCR register. The DMOS output has weak output current and regulation capability and only operate in the Deep-Sleep 2 mode for data retention purposes in the V_{DD15} power domain.

Power On Reset (POR) / Power Down Reset (PDR)

The device has an integrated POR/PDR circuitry that allows proper operation starting from/down to 2.0 V. The device remains in Power-Down mode when V_{DD} is below a specified threshold V_{PDR}, without the need for an external reset circuit. For more details the power on / power down reset threshold voltage, refer to the electrical characteristics of the corresponding datasheet.

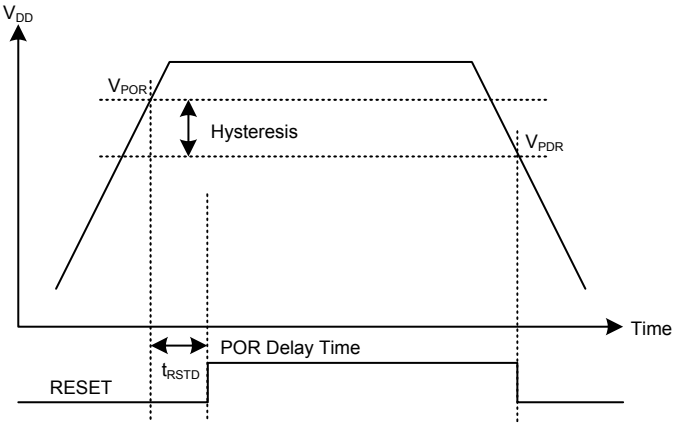


Figure 12. Power On Reset / Power Down Reset Waveform

Low Voltage Detector / Brown Out Detector

The Low Voltage Detector, LVD, can detect whether the supply voltage V_{DD} is lower than a programmable threshold voltage V_{LVD}. It is selected by the LVDS bits in the LVDCSR register. When a low voltage on the V_{DD} power pin is detected, the LVDF flag will be active and an interrupt will be generated and sent to the MCU core if the LVDEN and LVDIWEN bits in the LVDCSR register are set. For more details concerning the LVD programmable threshold voltage V_{LVD}, refer to the electrical characteristics of the corresponding datasheet.

The Brown Out Detector, BOD, is used to detect if the V_{DD} supply voltage is equal to or lower than V_{BOD}. When the BODEN bit in the LVDCSR register is set to 1 and the V_{DD} supply voltage is lower than V_{BOD} then the BODF flag is active. The PWRCU will regard this as a power down reset situation and then immediately disable the internal LDO regulator when the BODRIS bit is cleared to 0 or issue an interrupt to notify the CPU to execute a power down procedure when the BODRIS bit is set to 1. For more details concerning the Brown Out Detector voltage V_{BOD}, refer to the electrical characteristics of the corresponding datasheet.

High Speed Internal Oscillator

The High Speed Internal Oscillator, HSI, is located in the V_{DD} power domain. When exiting from the Deep-Sleep mode, the HSI clock will be configured as the system clock for a certain period by setting the PSRCEN bit to 1 This bit is located in the Global Clock Control Register, GCCR, in the Clock Control Unit, CKCU. The system clock will not be switched back to the original clock source used before entering the Deep-Sleep mode until the original clock source, which may be either sourced from the PLL or HSE stabilizes. Also the system will force the HSI oscillator to be the system clock after a wake up from Power-Down mode since a 1.5 V power on reset will occur.

High Speed External Oscillator

The High Speed External Oscillator, HSE, is located in the V_{DD} power domain. The HSE crystal oscillator can be switched on or off using the HSEEN bit in the Global Clock Control Register, GCCR. The HSE clock can then be used directly as the system clock source or be used as the PLL input clock.

Isolation Cells

When the device resumes operation from the 1.5 V power, either by Hardware or Software, access to the PWRCU registers in the V_{DD} power domain are disabled by the isolation cells which protect these registers against possible parasitic write accesses. To resume access operations, users must disable these isolation cells by setting the VDDISO bit to 1 in the LPCR register of the Clock Control Unit.

1.5 V Power Domain

The main functions that include the APB interface for the V_{DD} domain, CPU core logic, AHB/APB peripherals and memories and so on are located in this power domain. Once the 1.5 V is powered up, the POR will generate a reset sequence on 1.5 V power domain. Subsequently, to enter the expected power saving mode, the associated control bits including the LDOOFF, DMOSON and LDOLCM bits must be configured. Then, once a WFI or WFE instruction is executed, the device will enter an expected power saving mode which will be discussed in the following section.

Operation Modes

Run Mode

In the Run mode, the system operates with full functions and all power domains are active. There are two ways to reduce the power consumption in this mode. The first is to slow down the system clock by setting the AHBPRE field in the CKCU AHBCFGR register, and the second is to turn off the unused peripherals clock by setting the APBCCR0 and APBCCR1 registers or slow down peripherals clock by setting the APBPCSR0 and APBPCSR1 registers to meet the application requirement. Reducing the system clock speed before entering the sleep mode will also help to minimize power consumption.

Additionally, there are several power saving modes to provide maximum optimization between device performance and power consumption.

Table 11. Operation Mode Definitions

Mode name	Hardware Action
Run	After system reset, CPU fetches instructions to execute.
Sleep	1. CPU clock will be stopped. 2. Peripherals, Flash and SRAM clocks can be stopped by setting.
Deep-Sleep1~2	1. Stop all clocks in the 1.5 V power domain. 2. Disable HSI, HSE, and PLL. 3. Turning on the LDO low current mode or DMOS to reduce the 1.5 V power domain current.
Power-Down	Shut down the 1.5 V power domain

Sleep Mode

By default, only the CPU clock will be stopped in the Sleep mode. Clearing the FMCEN or SRAMEN bit in the CKCU AHBCCR register to 0 will have the effect of stopping the Flash clock or SRAM clock after the system enters the Sleep mode. If it is not necessary for the CPU to access the Flash memory and SRAM in the Sleep mode, it is recommended to clear the FMCEN and SRAMEN bits in the AHBCCR register to minimize power consumption. To enter the Sleep mode, it is only CPU executes a WFI or WFE instruction and lets the SLEEPDEEP signal to 0. The system will exit from the Sleep mode via any interrupt or event trigger. The accompanying table provides more information about the power saving modes.

Table 12. Enter/Exit Power Saving Modes

Mode	Mode Entry				Mode Exit
	CPU Instruction	CPU SLEEPDEEP	LDOOFF	DMOSON	
Sleep	WFI or WFE (Takes effect)	0	X	X	WFI: Any interrupt WFE: Any wakeup event (1) or Any interrupt (NVIC on) or Any interrupt with SEVONPEND = 1 (NVIC off)
Deep-Sleep1		1	0	0	Any EXTI in event mode or LVD wakeup (2) or WAKEUP pin rising edge
Deep-Sleep2		1	X	1	LVD wakeup (2) or WAKEUP pin rising edge
Power-Down		1	1	0	LVD wakeup (2) or WAKEUP pin rising edge or External reset (nRST)

Notes: 1. Wakeup event means EXTI line in event mode, LVD, and WAKEUP pin rising edge.

2. If the system allows the LVD activity to wake it up after the system has entered the power saving mode, the LVDEWEN and LVDEN bits in the LVDCSR register must be set to 1 to make sure that the system can be waked up by a LVD event and then the LDO regulator can be turned on when system is woken up from the Deep-Sleep2 and Power-Down modes.

Deep-Sleep Mode

To enter Deep-Sleep mode, configure the registers as shown in the preceding table and execute the WFI or WFE instruction. In the Deep-Sleep mode, all clocks including PLL and high speed oscillator, known as HSI and HSE, will be stopped. In addition, Deep-Sleep1 turns the LDO into low current mode while Deep-Sleep2 turns off the LDO and uses a DMOS to keep 1.5 V power. Once the PWRCU receives a wakeup event or an interrupt as shown in the preceding Mode-Exiting table, the LDO will then operate in normal mode and the high speed oscillator will be enabled. Finally, the CPU will return to Run mode to handle the wakeup interrupt if required. A Low Voltage Detection also can be regarded as a wakeup event if the corresponding wakeup control bit LVDEWEN in the LVDCSR register is enabled. The last wakeup event is a transition from low to high on the external WAKEUP pin sent to the PWRCU to resume from Deep-Sleep mode. During the Deep-Sleep mode, retaining the register and memory contents will shorten the wakeup latency.

Power-Down Mode

The Power-Down mode is derived from the Deep-Sleep mode of the CPU together with the additional control bits LDOOFF and DMOSON. To enter the Power-Down mode, users can configure the registers shown in the preceding Mode-Entering table and execute the WFI or WFE instruction. A LVD wakeup, a low to high transition on the external WAKEUP pin or an external reset (nRST) signal will force the MCU out of the Power-Down mode. In the Power-Down mode, the 1.5 V power supply will be turned off. The remaining active power supplies are the 3.3 V power (V_{DD}/V_{DDA}).

After a system reset, the PORSTF bit in the GRSR register in the Reset Control Unit, RSTCU, the PDF and PORF bits in the PWRSR register should be checked by software to confirm if the device is being resumed from the Power-Down mode, an power on reset or other reset events (nRST, WDT, …). If the device has entered the Power-Down mode under the correct firmware procedure, then the PDF bit will be set. The system information could be saved in the V_{DD} power domain registers and be retrieved when the 1.5 V power domain is powered on again. More information about the PDF and PORF bits in the PWRSR register and PORSTF bit in the RSTCU GRSR register is shown in the following table.

Table 13. Power Status After System Reset

PORF	PDF	PORSTF	Description
1	0	1	Power-up for the first time after the V_{DD} power domain is reset: Power on reset when V_{DD} is applied for the first time or executing software reset command on the V_{DD} domain.
0	0	1	Restart from unexpected loss of the 1.5 V power or other reset (nRST, WDT, …)
0	1	1	Restart from the Power-Down mode.
1	1	x	Reserved

Register Map

The following table shows the PWRCU registers and reset values. Note all the registers in this unit are located in the V_{DD} power domain.

Table 14. PWRCU Register Map

Register	Offset	Description	Reset Value
PWRSR	0x100	Power Control Status Register	0x0000_0001
PWRCR	0x104	Power Control Register	0x0000_0000
PWRTEST	0x108	V_{DD} Power Domain Test Register	0x0000_0027
LVDCSR	0x110	Low Voltage/Brown Out Detect Control and Status Register	0x0000_0000

Register Descriptions

Power Control Status Register – PWRSR

This register indicates the power control status.

Offset: 0x100

Reset value: 0x0000_0001 (Reset only by V_{DD} domain power on reset)

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							WUPF
Type/Reset								RC 0
	7	6	5	4	3	2	1	0
	Reserved						PDF	PORF
Type/Reset							RC 0	RC 1

Bits	Field	Descriptions
[8]	WUPF	External WAKEUP Pin Flag 0: The Wakeup pin is not asserted 1: The Wakeup pin is asserted This bit is set by hardware when the WAKEUP pin asserts and is cleared by software read. Software should read this bit to clear it after a system wake up from the power saving mode.
[1]	PDF	Power Down Flag 0: Wakeup from abnormal V_{DD15} shutdown (Loss of V_{DD15} is unexpected) 1: Wakeup from Power-Down mode. The loss of V_{DD15} is under expectation. This bit is set by hardware when the system has successfully entered the Power-Down mode. This bit is cleared by software read.
[0]	PORF	Power On Reset Flag 0: V_{DD} Power Domain reset does not occur 1: V_{DD} Power Domain reset occurs This bit is set by hardware when V_{DD} power on reset occurs, either a hardware power on reset or software reset. The bit is cleared by software read. This bit must be cleared after the system is first powered on, otherwise it will be impossible to detect when a V_{DD} Power Domain reset has been triggered. When this bit is read as 1, a read software loop must be implemented until the bit returns again to 0. This software loop is necessary to confirm that the V_{DD} Power Domain is ready for access.

Power Control Register – PWRCR

This register provides power control bits for the different kinds of power saving modes.

Offset: 0x104

Reset value: 0x0000_0000 (Reset only by V_{DD} domain power on reset)

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	DMOSSTS	Reserved		V15RDYSC	Reserved		WUPIEN	WUPEN
Type/Reset	RO 0			RW 0			RW 0	RW 0
	7	6	5	4	3	2	1	0
	DMOSON	Reserved			LDOOFF	LDOLCM	Reserved	PWRST
Type/Reset	RW 0				RW 0	RW 0		WO 0

Bits	Field	Descriptions
[15]	DMOSSTS	Depletion MOS Status This bit is set to 1 if the DMOSON bit in this register has been set to 1. This bit is cleared to 0 if the DMOSON bit has been set to 0 or if a POR/PDR reset occurred.
[12]	V15RDYSC	V_{DD15} Ready Source Selection. 0: VDDISO bit in the LPCR register located in the CKCU 1: V_{DD15} POR Setting this bit to determine what control signal of isolation cells is used to disable the isolation function of the V_{DD15} to V_{DD} power domain level shifter.
[9]	WUPIEN	External WAKEUP Pin Interrupt Enable 0: Disable WAKEUP pin interrupt function 1: Enable WAKEUP pin interrupt function The software can set the WUPIEN bit to 1 to assert the LPWUP interrupt in the NVIC unit when both the WUPEN and WUPF bits are set to1.

Bits	Field	Descriptions
[8]	WUPEN	External WAKEUP Pin Enable 0: Disable WAKEUP pin function. 1: Enable WAKEUP pin function. The Software can set the WUPEN bit as 1 to enable the WAKEUP pin function before entering the power saving mode. When WUPEN = 1, a rising edge on the WAKEUP pin wakes up the system from the power saving mode. As the WAKEUP pin is active high, this bit will set an input pull down mode when the bit is high. The WAKEUP pin alternate function should first be selected by configuring the PBCFG12 bit field in the GPBCFGHR register to 0x0F before the WAKEUP pin is used. The corresponding pull-up function on the WAKEUP pin should also be disabled by clearing the PBPU[12] bit in the PBPUR register to 0 while the pull-down function should be enabled by setting the PBPD[12] bit in the PBPDR register to 1. Note: This bit is reset by a V_{DD} Power Domain reset. Because this bit is located in the V_{DD} Power Domain, after reset activity there will be a delay until the bit is active. The bit will not be active until the system reset finished and the V_{DD} Power Domain ISO signal has been disabled. This means that the bit cannot be immediately set by software after a system reset finished and the V_{DD} Power Domain ISO signal disabled. The necessary delay time is a minimum of three 32kHz clock periods until the bit reset activity has finished.
[7]	DMOSON	DMOS Control 0: DMOS is OFF 1: DMOS is ON A DMOS is implemented to provide an alternative voltage source for the 1.5 V power domain when the CPU enters the Deep-Sleep mode (SLEEPDEEP = 1). The control bit DMOSON is set by software and cleared by software or V_{DD} power domain reset. If the DMOSON bit is set to 1, the LDO will automatically be turned off when the CPU enters the Deep-Sleep mode.
[3]	LDOOFF	LDO Operating Mode Control 0: The LDO operates in a low current mode when CPU enters the Deep-Sleep mode (SLEEPDEEP = 1). The V_{DD15} power is available. 1: The LDO is turned off when the CPU enters the Deep-Sleep mode (SLEEPDEEP=1). The V_{DD15} power is not available. Note: This bit is only available when the DMOSON bit is cleared to 0.
[2]	LDOLCM	LDO Low Current Mode 0: The LDO is operated in normal current mode 1: The LDO is operated in low current mode Note: This bit is only available when CPU is in the run mode. The LDO output current capability will be limited at 10mA below and lower static current when the LDOLCM bit is set. It is suitable for CPU is operated at lower speed system clock to get a lower current consumption. This bit will be clear to 0 when the LDO is power down or V_{DD} power domain reset.
[0]	PWRST	V_{DD} Power Domain Software Reset 0: No action 1: V_{DD} Power Domain Software Reset is activated It will reset the PWRCU registers.

V_{DD} Power Domain Test Register – PWRTEST

This register specifies a read-only value for the software to recognize whether V_{DD} Power Domain is ready for access.

Offset: 0x108

Reset value: 0x0000_0027

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	PWRTEST							
Type/Reset	RO 0	RO 0	RO 1	RO 0	RO 0	RO 1	RO 1	RO 1

Bits	Field	Descriptions
[7:0]	PWRTEST	V_{DD} Power Domain Test Bits A constant 0x27 will be read when the V_{DD} Power Domain is ready for CPU access.

Low Voltage / Brown Out Detect Control and Status Register – LVDCSR

This register specifies flags, enable bits and option bits for low voltage detector.

Offset: 0x110

Reset value: 0x0000_0000 (Reset only by V_{DD} domain power on reset)

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved	LVDS [2]	LVDEWEN	LVDIWEN	LVDF		LVDS [1:0]	LVDEN
Type/Reset		RW 0	RW 0	RW 0	RO 0	RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved				BODF	Reserved	BODRIS	BODEN
Type/Reset					RO 0		RW 0	RW 0

Bits	Field	Descriptions
[21]	LVDEWEN	LVD Event Wakeup Enable 0: LVD event wakeup is disabled 1: LVD event wakeup is enabled Setting this bit to 1 will enable the LVD event wakeup function to wake up the system when a LVD condition occurs which result in the LVDF bit being asserted. If the system requires to be waked up from the Deep-Sleep or Power-Down mode by a LVD condition, this bit must be set to 1.
[20]	LVDIWEN	LVD Interrupt Wakeup Enable 0: LVD interrupt wakeup is disabled 1: LVD interrupt wakeup is enabled Setting this bit to 1 will enable the LVD interrupt function. When a LVD condition occurs and the LVDIWEN bit is set to 1, a LVD interrupt will be generated and sent to the CPU NVIC unit.
[19]	LVDF	Low Voltage Detect Status Flag 0: V_{DD} is higher than the specific voltage level 1: V_{DD} is equal to or lower than the specific voltage level When the LVD condition occurs, the LVDF flag will be asserted. When the LVDF flag is asserted, a LVD interrupt will be generated for CPU if the LVDIWEN bit is set to 1. However, if the LVDEWEN bit is set to 1 and the LVDIWEN bit is cleared to 0, only a LVD event will be generated rather than a LVD interrupt when the LVDF flag is asserted.
[22], [18:17]	LVDS [2:0]	Low Voltage Detect Level Selection For more details concerning the LVD programmable threshold voltage, refer to the electrical characteristics of the corresponding datasheet.

Bits	Field	Descriptions
[16]	LVDEN	Low Voltage Detect Enable 0: Disable Low Voltage Detect 1: Enable Low Voltage Detect Setting this bit to 1 will generate a LVD event when the V_{DD} power is lower than the voltage set by LVDS bits. Therefore when the LVD function is enabled before the system is into the Deep-Sleep2 (DMOS is turn on and LDO is power down) or Power-Down mode (DMOS and LDO is power down), the LVDEWEN bit has to be enabled to avoid the LDO does not activate in the meantime when the CPU is woken up by the low voltage detection activity.
[3]	BODF	Brow Out Detect Flag 0: $V_{DD} > V_{BOD}$ 1: $V_{DD} \leq V_{BOD}$
[1]	BODRIS	BOD Reset or Interrupt Selection 0: Reset the whole chip 1: Generate Interrupt
[0]	BODEN	Brown Out Detector Enable 0: Disable Brown Out Detector 1: Enable Brown Out Detector

6 Clock Control Unit (CKCU)

Introduction

The Clock Control unit (CKCU) provides functions of high speed internal RC oscillator (HSI), High speed external crystal oscillator (HSE), Low speed internal RC oscillator (LSI), Phase Lock Loop (PLL), HSE clock monitor, clock prescaler, clock multiplexer and clock gating. The clock of AHB, APB, and CPU are derived from system clock (CK_SYS) which can come from HSI, HSE, LSI or PLL. The Watchdog Timer uses the LSI as the clock source.

A variety of internal clocks can also be wired out through the CKOUT pin for debugging purpose. The clock monitor can be used to detect the HSE clock failure. Once the HSE clock does not normally function, which could be broken down or removed, etc., the CKCU will force to switch the system clock source to the HSI clock to prevent system halt.

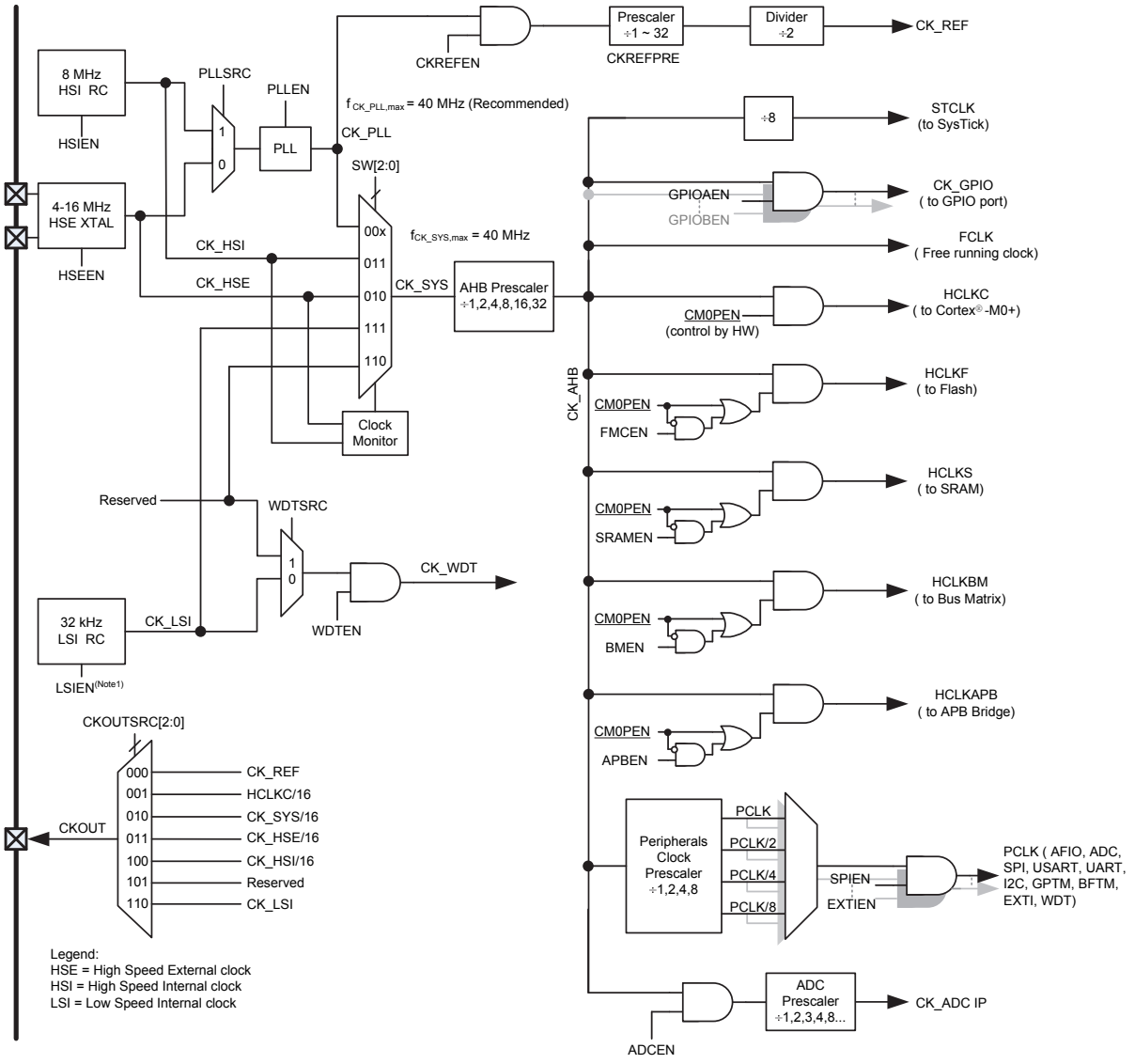


Figure 13. CKCU Block Diagram

Features

- 4 ~ 16 MHz external crystal oscillator (HSE)
- Internal 8 MHz RC oscillator (HSI) with configuration option calibration and custom trimming capability.
- PLL with selectable clock source (from HSE or HSI) for system clock.
- Internal 32 kHz RC oscillator (LSI) for Watchdog Timer or system clock.
- HSE clock monitor

Function Descriptions

High Speed External Crystal Oscillator – HSE

The high speed external crystal oscillator (HSE) with a frequency range from 4MHz to 16MHz produces a highly accurate clock source to the system clock. The related hardware configuration is shown in the following figure. The crystal with specific frequency must be placed across the two HSE pins (XTALIN / XTALOUT) and the external components such as resistors and capacitors are necessary to make it oscillate properly.

The following guidelines are provided to improve the stability of the crystal circuit PCB layout.

- The crystal oscillator should be located as close as possible to the MCU so that the trace lengths are kept as short as possible to reduce any parasitic capacitances.
- Shield any lines in the vicinity of the crystal by using a ground plane to isolate signals and reduce noise.
- Keep frequently switching signal lines away from the crystal area to prevent crosstalk.

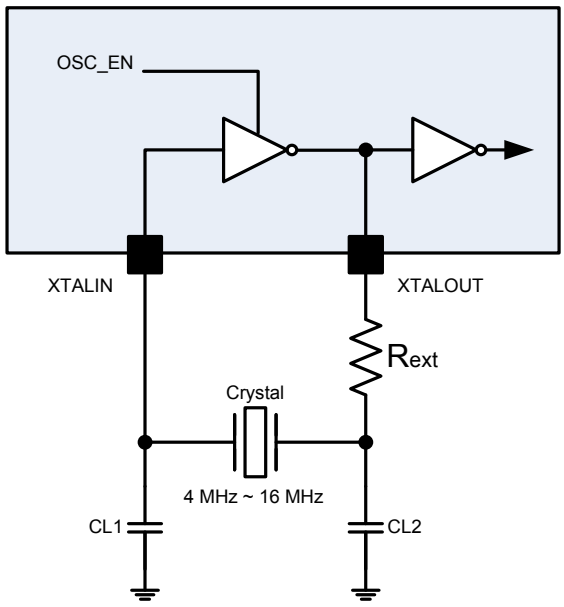


Figure 14. External Crystal, Ceramic, and Resonators for HSE

The HSE crystal oscillator can be switched on or off using the HSEEN bit in the Global Clock Control Register (GCCR). The HSERDY flag in the Global Clock Status Register (GCSR) will indicate if the high-speed external crystal oscillator is stable. When switching on the HSE oscillator, the HSE clock will still not be released until this HSERDY bit is set by the hardware. The specific delay period is well-known as "Start-up time". As the HSE becomes stable, an interrupt will be generated if the related interrupt enable bit, HSERDYIE, in the Global Clock Interrupt Register (GCIR) is set. The HSE clock can then be used directly as the system clock source or be used as the PLL input clock.

High Speed Internal RC Oscillator – HSI

The high speed internal 8 MHz RC oscillator (HSI) is the default selection of the clock source for the CPU when the device is powered up. The HSI RC oscillator provides a clock source in a lower cost because no external components are required. The HSI RC oscillator can be switched on or off using the HSIEN bit in the Global Clock Control Register (GCCR). The HSIRDY flag in the Global Clock Status Register (GCSR) will indicate if the internal RC oscillator is stable. The start-up time of the HSI oscillator is shorter than the HSE crystal oscillator. An interrupt can be generated if the related interrupt enable bit, HSIRDYIE, in the Global Clock Interrupt Register (GCIR) is set as the HSI becomes stable. The HSI clock can also be used as the PLL input clock.

The frequency accuracy of the high speed internal RC oscillator, HSI, can be calibrated via the trimming operations. However, it is still less accurate than the HSE crystal oscillator. The considerations of the applications, environments and cost will determine the selection of the oscillators.

The software program could configure the PSRCEN bit (Power Saving Wakeup RC Clock Enable) to 1 to force the HSI clock to be the system clock when wake-up from the Deep-Sleep or Power-Down mode. Subsequently, the system clock is switched back to the original clock source (HSE or PLL) if the original clock source ready flag is asserted. This function can reduce the wakeup time when using the HSE or PLL output clock as the system clock.

Phase Locked Loop – PLL

This PLL can provide 4 ~ 48 MHz clock output which is 1~12 multiples of a fundamental reference frequency of 4 ~ 16 MHz. The rationale of the clock synthesizer relies on the digital Phase Locked Loop (PLL) which includes a reference divider, a feedback divider, a digital phase frequency detector (PFD), a current-controlled charge pump, a built-in loop filter and a voltage-controlled oscillator (VCO) to achieve a stable phase-locked state.

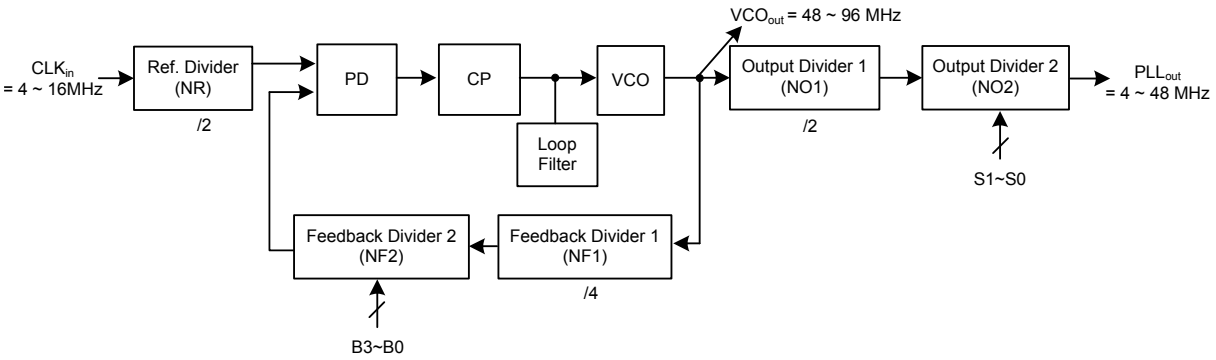


Figure 15. PLL Block Diagram

The frequency of the PLL output clock can be determined by the following formula:

$$PLL_{OUT} = CLK_{in} \times \frac{NF1 \times NF2}{NR \times NO1 \times NO2} = CLK_{in} \times \frac{4 \times NF2}{2 \times 2 \times NO2} = CLK_{in} \times \frac{NF2}{NO2}$$

where NR = Ref divider = 2, NF1 = Feedback Divider 1 = 4, NF2 = Feedback Divider 2 = 1 ~ 16,
NO1 = Output Divider 1 = 2, NO2 = Output Divider 2 = 1, 2, 4, or 8

Considering the duty cycle of 50%, both input and output frequencies are divided by 2. If a given CLK_{in} frequency used as the PLL input generates a specific PLL output frequency, it is recommended to load a larger value into the NF2 field to increase the PLL stability and reduce the jitter with expense of the settling time. The output and feedback divider 2 setup values are described in Table 15 and Table 16. All the configuration bits (S1 ~ S0, B3 ~ B0) in Table 15 and Table 16 are defined in the PLL Configuration Register (PLLCFGR) and PLL Control Register (PLLCR) in the section of Register Definition. Note that the VCO_{OUT} frequency should be in the range from 48 MHz to 96 MHz. If the selected configuration exceeds this range, the PLL output frequency will not be guaranteed to match the above PLL_{OUT} formula.

The PLL can be switched on or off using the PLLEN bit in the Global Clock Control Register (GCCR). The PLLRDY flag in the Global Clock Status Register (GCSR) will indicate if the PLL clock is stable. An interrupt can be generated if the related interrupt enable bit PLLRDYIE in the Global Clock Interrupt Register (GCIR) is set as the PLL becomes stable.

Table 15. Output Divider2 Value Mapping

Output divider 2 setup bits S[1:0] (POTD bits in the PLLCFGR register)	NO2 (Output divider 2 value)
00	1
01	2
10	4
11	8

Table 16. Feedback Divider2 Value Mapping

Feedback divider2 setup bits B[3:0] (PFBD bits in the PLLCFGR register)	NF2 (Feedback divider 2 value)
0000	16
0001	1
0010	2
0011	3
0100	4
0101	5
0110	6
0111	7
1000	8
1001	9
1010	10
1011	11
1100	12
:	:
:	:
1111	15

Low Speed Internal RC Oscillator – LSI

The low speed internal RC oscillator with a frequency of about 32 kHz produces a low power clock source for the Watchdog Timer or system clock. The LSI oscillator offers a low cost clock source because no external component is required to make it oscillates. The LSI RC oscillator is always enable. The LSI frequency accuracy is shown in the datasheet. The LSIRDY flag in the Global Clock Status Register (GCSR) will indicate if the LSI clock is stable. An interrupt can be generated if the related interrupt enable bit LSIRDYIE in the Global Clock Interrupt Register (GCIR) is set as the LSI becomes stable.

Clock Ready Flag

The CKCU provides the corresponding clock ready flags for the HSI, HSE, PLL and LSI oscillators to indicate whether these clocks are stable. Before using them as the system clock source or other purpose, it is necessary to confirm the specific clock ready flag is set. Software can check the specific clock is ready or not by polling the corresponding clock ready status bits in the GCSR register. Additionally, the CKCU can trigger an interrupt to notify that the specific clock is ready if the corresponding interrupt enable bit in the GCIR register is set. Software should clear the interrupt status bit in the GCIR register in the interrupt service routine.

System Clock (CK_SYS) Selection

After the system reset occurs, the default system clock source, CK_SYS, will be the high speed internal RC oscillator, HSI. The CK_SYS may come from the HSI, HSE, LSI or PLL output clock and it can be switched from one clock source to another by configuring the System Clock Switch bits SW in the Global Clock Control Register, GCCR. The system will still run under the original clock until the destination clock gets ready when the SW value is changed. The corresponding clock ready status bits in the Global Clock Status Register GCSR will indicate whether the selected clock is ready to use or not. The CKCU also contains the clock source status bits in the Clock Source Status Register CKST to indicate which clock is currently used as the system clock. If a clock source or the PLL output clock is used as the system clock source, it is not possible to stop it. More details about the clock enable function are described in the following .

If any event in the following occurs, the HSI will be enabled .

- Enable PLL and configure its source clock to HSI. (PLLEN, PLLSRC)
- Enable Clock monitor. (CKMEN)
- Configure clock switch register to HSI. (SW)
- Configure HSI enable register to 1. (HSIEN)

If any event in the following occurs, the HSE will be enabled.

- Enable PLL and configure its source clock to HSE. (PLLEN, PLLSRC)
- Configure clock switch register to HSE. (SW)
- Configure HSE enable register to 1. (HSEEN)

If any event in the following occurs, the PLL will be enabled.

- Enable USB Enable register. (USBEN)
- Configure clock switch register to PLL (SW)
- Configure PLL enable register to 1. (PLLEN)

The system clock selection programming guide is listed in the following.

1. Enable any clock source which will become the system clock or PLL input clock.
2. Configuring the PLLSRC register will has no operation until the ready flags of both HSI and HSE are asserted.
3. Configuring the SW register to change the system clock source will take effect after the corresponding ready flag of the clock source is asserted. Note that the system clock will be forced to HSI if the clock monitor is enabled and the PLL output clock or HSE clock configured as the system clock is stuck at 0 or 1.

HSE Clock Monitor

The HSE Clock Monitor main function is enabled by the HSE Clock Monitor Enable bit CKMEN in the Global Clock Control Register, GCCR. The HSE clock monitor function should be enabled after the HSE oscillator start-up delay and disabled when the HSE oscillator is stopped. Once the HSE oscillator failure is detected, the HSE oscillator will automatically be disabled. The HSE clock stuck flag CKSF in the Global Clock Interrupt Register GCIR will be set and the HSE oscillator failure interrupt will be generated if the clock failure interrupt enable bit CKSIE in the GCIR is set. This failure interrupt is connected to the CPU Non-Maskable Interrupt, NMI. When the HSE oscillator failure occurs, the HSE will be turned off and the system clock will be switched to the HSI automatically by the hardware. If the HSE is used as the clock input of the PLL circuit and the PLL output clock is used as the system clock, the PLL circuit will also be turned off as well as the HSE when the failure happens.

Clock Output Capability

The device has the clock output capability to allow the clocks to be output on the specific external output pin CKOUT. The configuration registers of the corresponding GPIO port must be well configured in the Alternate Function I/O, AFIO, section to output the selected clock signal. There are six output clock signals to be selected via the device clock output source selection bits CKOUTSRC in the Global Clock Configuration Register, GCFGR.

Table 17. CKOUT Clock Source

CKOUTSRC[2:0]	Clock Source
000	CK_REF = CK_PLL / (CKREFPRE + 1) / 2
001	CK_AHB / 16
010	CK_SYS / 16
011	CK_HSE / 16
100	CK_HSI / 16
101	Reserved
110	CK_LSI

Register Map

The following table shows the CKCU register and reset value.

Table 18. CKCU Register Map

Register	Offset	Description	Reset Value
GCFGR	0x000	Global Clock Configuration Register	0x0000_0102
GCCR	0x004	Global Clock Control Register	0x0000_0803
GCSR	0x008	Global Clock Status Register	0x0000_0028
GCIR	0x00C	Global Clock Interrupt Register	0x0000_0000
PLLCFGR	0x018	PLL Configuration Register	0x0000_0000
PLLCR	0x01C	PLL Control Register	0x0000_0000
AHBCFGR	0x020	AHB Configuration Register	0x0000_0000
AHBCCR	0x024	AHB Clock Control Register	0x0000_0065
APBCFGR	0x028	APB Configuration Register	0x0000_0000
APBCCR0	0x02C	APB Clock Control Register 0	0x0000_0000
APBCCR1	0x030	APB Clock Control Register 1	0x0000_0000
CKST	0x034	Clock Source Status Register	0x0100_0003
APBPCSR0	0x038	APB Peripheral Clock Selection Register 0	0x0000_0000
APBPCSR1	0x03C	APB Peripheral Clock Selection Register 1	0x0000_0000
LPCR	0x300	Low Power Control Register	0x0000_0000
MCUDBGCR	0x304	MCU Debug Control Register	0x0000_0000

Register Descriptions

Global Clock Configuration Register – GCFGR

This register specifies the clock source for the PLL/USART/Watchdog Timer/CKOUT.

Offset: 0x000

Reset value: 0x0000_0102

	31	30	29	28	27	26	25	24
	LPMOD			Reserved				
Type/Reset	RO 0	RO 0	RO 0					
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	CKREFPRE					Reserved		PLLSRC
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0			RW 1
	7	6	5	4	3	2	1	0
	Reserved					CKOUTSRC		
Type/Reset						RW 0	RW 1	RW 0

Bits	Field	Descriptions
[31:29]	LPMOD	Lower Power Mode Status 000: When Chip is in running mode 001: When Chip wants to enter Sleep mode 010: When Chip wants to enter Deep Sleep mode1 011: When Chip wants to enter Deep Sleep mode2 100: When Chip wants to enter Power Down mode Others: Reserved Set and reset by hardware.
[15:11]	CKREFPRE	CK_REF Clock Prescaler Selection CK_REF = CK_PLL / (CKREFPRE + 1) / 2 00000: CK_REF = CK_PLL / 2 00001: CK_REF = CK_PLL / 4 ... 11111: CK_REF = CK_PLL / 64 Set and reset by software to control the CK_REF clock prescaler setting.
[8]	PLLSRC	PLL Clock Source Selection 0: External 4 ~ 16 MHz crystal oscillator clock is selected (HSE) 1: Internal 8 MHz RC oscillator clock is selected (HSI) Set and reset by software to control the PLL clock source.

Bits	Field	Descriptions
[2:0]	CKOUTSRC	CKOUT Clock Source Selection 000: CK_REF is selected where CK_REF = CK_PLL / (CKREFPRE+1) / 2 001: (HCLKC / 16) is selected 010: (CK_SYS / 16) is selected 011: (CK_HSE / 16) is selected 100: (CK_HSI / 16) is selected 101: Reserved 110: CK_LSI is selected 111: Reserved Set and reset by software.

Global Clock Control Register – GCCR

This register specifies the clock enable bits.

Offset: 0x004

Reset value: 0x0000_0803

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved						PSRCEN	CKMEN
Type/Reset							RW 0	RW 0
	15	14	13	12	11	10	9	8
	Reserved				HSIEN	HSEEN	PLLEN	HSEGAIN
Type/Reset					RW 1	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	Reserved					SW		
Type/Reset						RW 0	RW 1	RW 1

Bits	Field	Descriptions
[17]	PSRCEN	Power Saving Wakeup RC Clock Enable 0: No action 1: Use Internal 8 MHz RC clock (HSI) as system clock after power down wakeup. The software can set the PSRCEN bit high before entering the power saving mode in order to reduce the waiting time after a wakeup. When the PSRCEN bit is set to 1, the HSI will be used as the CK_SYS clock source after waking up from the power saving mode. This means that the instruction can be executed early before the original clock CK_SYS source is stable since the HSI clock is provided to CPU. After the original CK_SYS clock source is ready, the CK_SYS clock will automatically be switched back to the original selected clock source from the HSI clock.
[16]	CKMEN	HSE Clock Monitor Enable 0: Disable External 4 ~ 16 MHz crystal oscillator clock monitor 1: Enable External 4 ~ 16 MHz crystal oscillator clock monitor When the hardware detects that the HSE clock is stuck at a low or high state, the internal hardware will switch the system clock to the internal high speed RC clock, HSI.
[11]	HSIEN	Internal High Speed Oscillator Enable 0: Internal 8 MHz RC oscillator is disabled 1: Internal 8 MHz RC oscillator is enabled Set and reset by software. This bit can not be reset if the HSI clock is used as system clock.
[10]	HSEEN	External High Speed Oscillator Enable 0: External 4 ~ 16 MHz crystal oscillator is disabled 1: External 4 ~ 16 MHz crystal oscillator is enabled Set and reset by software. This bit can not be reset if the HSE clock is used as the system clock or the PLL input clock.

Bits	Field	Descriptions
[9]	PLLEN	PLL Enable 0: PLL is disabled 1: PLL is enabled Set and reset by software. This bit cannot be reset if the PLL clock is used as the system clock.
[8]	HSEGAIN	External High Speed Oscillator Gain Selection 0: HSE is in low gain mode 1: HSE is in high gain mode
[2:0]	SW	System Clock Switch 00x: CK_PLL clock out as system clock 010: CK_HSE as system clock 011: CK_HSI as system clock 110: Reserved 111: CK_LSI as system clock Other: CK_HSI as system clock These bits are set and reset by software and used to select the CK_SYS source. When switching the system clock using the SW bits, the system clock will not be immediately switched and a certain delay is necessary. The system clock source selected by the SW bits can be indicated in the CKSWST bits in the clock source status register CKST to make sure which clock is currently used as the system clock. Note that the HSI oscillator will be forced as the system clock when the HSE clock failure is detected as the HSE clock monitor function is enabled.

Global Clock Status Register – GCSR

This register indicates the clock ready status.

Offset: 0x008

Reset value: 0x0000_0028

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
		Reserved	LSIRDY	Reserved	HSIRDY	HSERDY	PLLRDY	Reserved
Type/Reset			RO 1		RO 1	RO 0	RO 0	

Bits	Field	Descriptions
[5]	LSIRDY	Internal Low Speed Oscillator Ready Flag 0: Internal 32 kHz RC oscillator is not ready 1: Internal 32 kHz RC oscillator is ready Set by hardware to indicate whether the LSI oscillator is stable to be used.
[3]	HSIRDY	Internal High Speed Oscillator Ready Flag 0: Internal 8 MHz RC oscillator is not ready 1: Internal 8 MHz RC oscillator is ready Set by hardware to indicate whether the HSI oscillator is stable to be used.
[2]	HSERDY	External High Speed Oscillator Ready Flag 0: External 4 ~ 16 MHz crystal oscillator is not ready 1: External 4 ~ 16 MHz crystal oscillator is ready Set by hardware to indicate whether the HSE oscillator is stable to be used.
[1]	PLLRDY	PLL Clock Ready Flag 0: PLL is not ready 1: PLL is ready Set by hardware to indicate whether the PLL output clock is stable to be used.

Global Clock Interrupt Register – GCIR

This register specifies the interrupt enable and flag bits.

Offset: 0x00C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							CKSIE
Type/Reset								RW 0
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved							CKSF
Type/Reset								WC 0

Bits	Field	Descriptions
[16]	CKSIE	Clock Stuck Interrupt Enable 0: Disable clock failure interrupt 1: Enable clock failure interrupt Set and reset by software to enable or disable the clock failure interrupt caused by the clock monitor function.
[0]	CKSF	Clock Stuck Interrupt Flag 0: Clock works normally 1: HSE clock is stuck Reset by software (Write 1 clear). Set by hardware when the HSE clock is stuck and the CKMEN bit is set.

PLL Configuration Register – PLLCFGR

This register specifies the PLL configurations.

Offset: 0x018

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved					PFBD		
Type/Reset						RW 0	RW 0	RW 0
	23	22	21	20	19	18	17	16
	PFBD			POTD		Reserved		
Type/Reset	RW 0	RW 0	RW 0					
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved							
Type/Reset								

Bits	Field	Descriptions
[26:23]	PFBD	PLL VCO Output Clock Feedback Divider (Figure 15 B3 ~ B0) The PLL Feedback Divider divides the output clock from the PLL VCO.
[22:21]	POTD	PLL Output Clock Divider (Figure 15 S1 ~ S0)

PLL Control Register – PLLCR

This register specifies the PLL Bypass mode.

Offset: 0x01C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	PLLBPS	Reserved						
Type/Reset	RW 0							
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved							
Type/Reset								

Bits	Field	Descriptions
[31]	PLLBPS	PLL Bypass Mode Enable 0: Disable PLL Bypass mode 1: Enable PLL Bypass mode which acts as FOUT = FIN

AHB Configuration Register – AHBCFGR

This register specifies the system clock frequency.

Offset: 0x020

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved					AHBPRE		
Type/Reset						RW 0	RW 0	RW 0

Bits	Field	Descriptions
[2:0]	AHBPRE	AHB Pre-scaler 000: CK_AHB = CK_SYS 001: CK_AHB = CK_SYS / 2 010: CK_AHB = CK_SYS / 4 011: CK_AHB = CK_SYS / 8 100: CK_AHB = CK_SYS / 16 101: CK_AHB = CK_SYS / 32 110: CK_AHB = CK_SYS / 32 111: CK_AHB = CK_SYS / 32 Set and reset by software to control the division factor of the AHB clock.

AHB Clock Control Register – AHBCCR

This register specifies the AHB clock enable control bits.

Offset: 0x024

Reset value: 0x0000_0065

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved						PBEN	PAEN
Type/Reset							RW 0	RW 0
	15	14	13	12	11	10	9	8
	Reserved				CKREFEN	Reserved		
Type/Reset					RW 0			
	7	6	5	4	3	2	1	0
	Reserved	APBEN	BMEN		Reserved	SRAMEN	Reserved	FMCEN
Type/Reset		RW 1	RW 1			RW 1		RW 1

Bits	Field	Descriptions
[17]	PBEN	GPIO Port B Clock Enable 0: Port B clock is disabled 1: Port B clock is enabled Set and reset by software
[16]	PAEN	GPIO Port A Clock Enable 0: Port A clock is disabled 1: Port A clock is enabled Set and reset by software
[11]	CKREFEN	CK_REF Clock Enable 0: CK_REF clock is disabled 1: CK_REF clock is enabled Set and reset by software
[6]	APBEN	APB bridge Clock Enable 0: APB bridge clock is automatically disabled by hardware during Sleep mode 1: APB bridge clock is always enabled during Sleep mode Set and reset by software. User can set the APBEN bit to 0 to reduce the power consumption if the APB bridge is unused during the Sleep mode.
[5]	BMEN	Bus Matrix Clock Enable 0: Bus Matrix clock is automatically disabled by hardware during Sleep mode 1: Bus Matrix clock is always enabled during Sleep mode Set and reset by software. User can set the BMEN bit to 0 to reduce the power consumption if the bus matrix is unused during the Sleep mode.
[2]	SRAMEN	SRAM Clock Enable 0: SRAM clock is automatically disabled by hardware during Sleep mode 1: SRAM clock is always enabled during Sleep mode Set and reset by software. User can set the SRAMEN bit to 0 to reduce the power consumption if the SRAM is unused during the Sleep mode.

Bits	Field	Descriptions
[0]	FMCEN	Flash Memory Controller Clock Enable 0: FMC clock is automatically disabled by hardware during Sleep mode 1: FMC clock is always enabled during Sleep mode Set and reset by software. User can set the FMCEN bit to 0 to reduce the power consumption if the Flash Memory is unused during the Sleep mode.

APB Configuration Register – APBCFGR

This register specifies the ADC conversion clock frequency.

Offset: 0x028

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved					ADCDIV		
Type/Reset						RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved							
Type/Reset								

Bits	Field	Descriptions
[18:16]	ADCDIV	ADC Clock Frequency Division Selection 000: CK_ADC = (CK_AHB / 1) 001: CK_ADC = (CK_AHB / 2) 010: CK_ADC = (CK_AHB / 4) 011: CK_ADC = (CK_AHB / 8) 100: CK_ADC = (CK_AHB / 16) 101: CK_ADC = (CK_AHB / 32) 110: CK_ADC = (CK_AHB / 64) 111: CK_ADC = (CK_AHB / 3) Set and reset by software to control the ADC conversion clock division factor.

APB Clock Control Register 0 – APBCCR0

This register specifies the APB peripherals clock enable control bits.

Offset: 0x02C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	EXTIEN	AFIOEN	Reserved			UREN	Reserved	USREN
Type/Reset	RW 0	RW 0				RW 0		RW 0
	7	6	5	4	3	2	1	0
	Reserved			SPIEN	Reserved			I2CEN
Type/Reset				RW 0				RW 0

Bits	Field	Descriptions
[15]	EXTIEN	External Interrupt Clock Enable 0: EXTI clock is disabled 1: EXTI clock is enabled Set and reset by software.
[14]	AFIOEN	Alternate Function I/O Clock Enable 0: AFIO clock is disabled 1: AFIO clock is enabled Set and reset by software.
[10]	UREN	UART Clock Enable 0: UART clock is disabled 1: UART clock is enabled Set and reset by software.
[8]	USREN	USART Clock Enable 0: USART clock is disabled 1: USART clock is enabled Set and reset by software.
[4]	SPIEN	SPI Clock Enable 0: SPI clock is disabled 1: SPI clock is enabled Set and reset by software.
[0]	I2CEN	I^2C Clock Enable 0: I^2C clock is disabled 1: I^2C clock is enabled Set and reset by software.

APB Clock Control Register 1 – APBCCR1

This register specifies the APB peripherals clock enable control bits.

Offset: 0x030

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
		Reserved	SCTM1EN	SCTM0EN	Reserved			ADCCEN
Type/Reset			RW 0	RW 0				RW 0
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	Reserved							BFTMEN
Type/Reset								RW 0
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	Reserved							GPTMEN
Type/Reset								RW 0
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	Reserved	VDDREN	Reserved	WDTREN	Reserved			
Type/Reset		RW 0		RW 0				

Bits	Field	Descriptions
[29]	SCTM1EN	SCTM1 Clock Enable 0: SCTM1 clock is disabled 1: SCTM1 clock is enabled Set and reset by software.
[28]	SCTM0EN	SCTM0 Clock Enable 0: SCTM0 clock is disabled 1: SCTM0 clock is enabled Set and reset by software.
[24]	ADCCEN	ADC Controller Clock Enable 0: ADC clock is disabled 1: ADC clock is enabled Set and reset by software.
[16]	BFTMEN	BFTM Clock Enable 0: BFTM clock is disabled 1: BFTM clock is enabled Set and reset by software.
[8]	GPTMEN	GPTM Clock Enable 0: GPTM clock is disabled 1: GPTM clock is enabled Set and reset by software.
[6]	VDDREN	V_{DD} Domain Clock Enable for Registers Access 0: V_{DD} Domain Register access clock is disabled 1: V_{DD} Domain Register access clock is enabled Set and reset by software.
[4]	WDTREN	Watchdog Timer Clock Enable for Registers Access 0: Register access clock is disabled 1: Register access clock is enabled Set and reset by software.

Clock Source Status Register – CKST

This register specifies the clock source status.

Offset: 0x034

Reset value: 0x0100_0003

	31	30	29	28	27	26	25	24
	Reserved					HSIST		
Type/Reset						RO 0	RO 0	RO 1
	23	22	21	20	19	18	17	16
	Reserved						HSEST	
Type/Reset							RO 0	RO 0
	15	14	13	12	11	10	9	8
	Reserved				PLLST			
Type/Reset					RO 0	RO 0	RO 0	RO 0
	7	6	5	4	3	2	1	0
	Reserved					CKSWST		
Type/Reset						RO 0	RO 1	RO 1

Bits	Field	Descriptions
[26:24]	HSIST	Internal High Speed Clock Occupation Status (CK_HSI) xx1: HSI is used by System Clock (CK_SYS) (SW = 0x03) x1x: HSI is used by PLL 1xx: HSI is used by Clock Monitor
[17:16]	HSEST	External High Speed Clock Occupation Status (CK_HSE) x1: HSE is used by System Clock (CK_SYS) (SW = 0x02) 1x: HSE is used by PLL
[11:8]	PLLST	PLL Clock Occupation Status xxx1: PLL is used by System Clock (CK_SYS) xx1x: Reserved x1xx: Reserved 1xxx: PLL is used by CK_REF
[2:0]	CKSWST	Clock Switch Status 00x: CK_PLL clock out as system clock 010: CK_HSE as system clock 011: CK_HSI as system clock 110: Reserved 111: CK_LSI as system clock The fields are status to indicate which clock source is using as system clock currently.

APB Peripheral Clock Selection Register 0 – APBPCSR0

This register specifies the APB peripheral clock prescaler selection.

Offset: 0x038

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
		Reserved		URPCLK		Reserved		USRPCLK
Type/Reset			RW	0 RW 0			RW	0 RW 0
	23	22	21	20	19	18	17	16
		Reserved		GPTMPCLK		Reserved		
Type/Reset			RW	0 RW 0				
	15	14	13	12	11	10	9	8
		Reserved		BFTMPCLK		Reserved		
Type/Reset			RW	0 RW 0				
	7	6	5	4	3	2	1	0
		Reserved		SPIPCLK		Reserved		I2CPCLK
Type/Reset			RW	0 RW 0			RW	0 RW 0

Bits	Field	Descriptions
[29:28]	URPCLK	UART Peripheral Clock Selection 00: PCLK = CK_AHB 01: PCLK = CK_AHB / 2 10: PCLK = CK_AHB / 4 11: PCLK = CK_AHB / 8 PCLK = Peripheral Clock; CK_AHB = AHB and CPU clock
[25:24]	USRPCLK	USART Peripheral Clock Selection 00: PCLK = CK_AHB 01: PCLK = CK_AHB / 2 10: PCLK = CK_AHB / 4 11: PCLK = CK_AHB / 8 PCLK = Peripheral Clock; CK_AHB = AHB and CPU clock
[21:20]	GPTMPCLK	GPTM Peripheral Clock Selection 00: PCLK = CK_AHB 01: PCLK = CK_AHB / 2 10: PCLK = CK_AHB / 4 11: PCLK = CK_AHB / 8 PCLK = Peripheral Clock; CK_AHB = AHB and CPU clock
[13:12]	BFTMPCLK	BFTM Peripheral Clock Selection 00: PCLK = CK_AHB 01: PCLK = CK_AHB / 2 10: PCLK = CK_AHB / 4 11: PCLK = CK_AHB / 8 PCLK = Peripheral Clock; CK_AHB = AHB and CPU clock
[5:4]	SPIPCLK	SPI Peripheral Clock Selection 00: PCLK = CK_AHB 01: PCLK = CK_AHB / 2 10: PCLK = CK_AHB / 4 11: PCLK = CK_AHB / 8 PCLK = Peripheral Clock; CK_AHB = AHB and CPU clock

Bits	Field	Descriptions
[1:0]	I2CPCLK	I2C Peripheral Clock Selection 00: PCLK = CK_AHB 01: PCLK = CK_AHB / 2 10: PCLK = CK_AHB / 4 11: PCLK = CK_AHB / 8 PCLK = Peripheral Clock; CK_AHB = AHB and CPU clock

APB Peripheral Clock Selection Register 1 – APBPCSR1

This register specifies the APB peripheral clock prescaler selection.

Offset: 0x03C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved					SCTM1PCLK		SCTM0PCLK
Type/Reset					RW 0	RW 0	RW 0	RW 0
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
		VDDRPCLK		WDTRPCLK	Reserved			
Type/Reset	RW 0	RW 0	RW 0	RW 0				
	7	6	5	4	3	2	1	0
		Reserved		ADCCPCLK		EXTIPCLK		AFIOPCLK
Type/Reset			RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[27:26]	SCTM1PCLK	SCTM1 Peripheral Clock Selection 00: PCLK = CK_AHB 01: PCLK = CK_AHB / 2 10: PCLK = CK_AHB / 4 11: PCLK = CK_AHB / 8 PCLK = Peripheral Clock; CK_AHB = AHB and CPU clock
[25:24]	SCTM0PCLK	SCTM0 Peripheral Clock Selection 00: PCLK = CK_AHB 01: PCLK = CK_AHB / 2 10: PCLK = CK_AHB / 4 11: PCLK = CK_AHB / 8 PCLK = Peripheral Clock; CK_AHB = AHB and CPU clock
[15:14]	VDDRPCLK	V_{DD} Domain Register Access Clock Selection 00: PCLK = CK_AHB / 4 01: PCLK = CK_AHB / 8 10: PCLK = CK_AHB / 16 11: PCLK = CK_AHB / 32 PCLK = Peripheral Clock; CK_AHB = AHB and CPU clock
[13:12]	WDTRPCLK	WDT Register Access Clock Selection 00: PCLK = CK_AHB 01: PCLK = CK_AHB / 2 10: PCLK = CK_AHB / 4 11: PCLK = CK_AHB / 8 PCLK = Peripheral Clock; CK_AHB = AHB and CPU clock
[5:4]	ADCCPCLK	ADC Controller Peripheral Clock Selection 00: PCLK = CK_AHB 01: PCLK = CK_AHB / 2 10: PCLK = CK_AHB / 4 11: PCLK = CK_AHB / 8 PCLK = Peripheral Clock; CK_AHB = AHB and CPU clock

Bits	Field	Descriptions
[3:2]	EXTIPCLK	EXTI Peripheral Clock Selection 00: PCLK = CK_AHB 01: PCLK = CK_AHB / 2 10: PCLK = CK_AHB / 4 11: PCLK = CK_AHB / 8 PCLK = Peripheral Clock; CK_AHB = AHB and CPU clock
[1:0]	AFIOPCLK	AFIO Peripheral Clock Selection 00: PCLK = CK_AHB 01: PCLK = CK_AHB / 2 10: PCLK = CK_AHB / 4 11: PCLK = CK_AHB / 8 PCLK = Peripheral Clock; CK_AHB = AHB and CPU clock

Low Power Control Register – LPCR

This register specifies the low power control.

Offset: 0x300

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved							VDDISO
Type/Reset								RW 0

Bits	Field	Descriptions
[0]	VDDISO	V_{DD} Domain Isolation Control 0: V_{DD} domain is isolated from other power domain 1: V_{DD} domain is accessible by other power domain Set and reset by software. Please refer to the Power Control Unit chapter for more information.

MCU Debug Control Register – MCUDBGCR

This register specifies the MCU debug control.

Offset: 0x304

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	DBSCTM1	DBSCTM0	Reserved			DBUR	Reserved	DBBFTM
Type/Reset	RW 0	RW 0				RW 0		RW 0
	15	14	13	12	11	10	9	8
	Reserved	DBDSLP2	Reserved	DBI2C	Reserved	DBSPI	Reserved	DBUSR
Type/Reset		RW 0		RW 0		RW 0		RW 0
	7	6	5	4	3	2	1	0
	Reserved	DBGPTM	Reserved		DBWDT	DBPD	DBDSLP1	DBSLP
Type/Reset		RW 0			RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[23]	DBSCTM1	SCTM1 Debug Mode Enable 0: SCTM1 counter continues to count even if the core is halted 1: SCTM1 counter stops counting when the core is halted Set and reset by software.
[22]	DBSCTM0	SCTM0 Debug Mode Enable 0: SCTM0 counter continues to count even if the core is halted 1: SCTM0 counter stops counting when the core is halted Set and reset by software.
[18]	DBUR	UART Debug Mode Enable 0: Same behavior as in normal mode 1: UART FIFO timeout is frozen when the core is halted Set and reset by software.
[16]	DBBFTM	BFTM Debug Mode Enable 0: BFTM counter continues to count even if the core is halted 1: BFTM counter stops counting when the core is halted Set and reset by software.
[14]	DBDSLP2	Debug Deep-Sleep2 0: LDO = Off (but turn on DMOS), FCLK = Off, and HCLK = Off in Deep-Sleep2 1: LDO = On, FCLK = On, and HCLK = On in Deep-Sleep2 Set and reset by software.
[12]	DBI2C	I^2C Debug Mode Enable 0: Same behavior as in normal mode 1: I^2C timeout is frozen when the core is halted Set and reset by software.
[10]	DBSPI	SPI Debug Mode Enable 0: Same behavior as in normal mode 1: SPI FIFO timeout is frozen when the core is halted Set and reset by software.

Bits	Field	Descriptions
[8]	DBUSR	USART Debug Mode Enable 0: Same behavior as in normal mode 1: USART FIFO timeout is frozen when the core is halted Set and reset by software.
[6]	DBGPTM	GPTM Debug Mode Enable 0: GPTM counter continues to count even if the core is halted 1: GPTM counter stops counting when the core is halted Set and reset by software.
[3]	DBWDT	Watchdog Timer Debug Mode Enable 0: Watchdog Timer counter continues to count even if the core is halted 1: Watchdog Timer counter stops counting when the core is halted Set and reset by software.
[2]	DBPD	Debug Power-Down Mode 0: LDO = Off, FCLK = Off, and HCLK = Off in Power-Down mode 1: LDO = On, FCLK = On, and HCLK = On in Power-Down mode Set and reset by software.
[1]	DBDSLP1	Debug Deep-Sleep1 0: LDO = Low power mode, FCLK = Off, and HCLK = Off in Deep-Sleep1 1: LDO = On, FCLK = On, and HCLK = On in Deep-Sleep1 Set and reset by software.
[0]	DBSLP	Debug Sleep Mode 0: LDO = On, FCLK = On, and HCLK = Off in Sleep mode 1: LDO = On, FCLK = On, and HCLK = On in Sleep mode Set and reset by software.

7 Reset Control Unit (RSTCU)

Introduction

The Reset Control Unit, RSTCU, has three kinds of reset, the power on reset, system reset and APB unit reset. The power on reset, known as a cold reset, resets the full system during a power up. A system reset resets the processor core and peripheral IP components with the exception of the debug port controller. The resets can be triggered by an external signal, internal events and the reset generators. More information about these resets will be described in the following section.

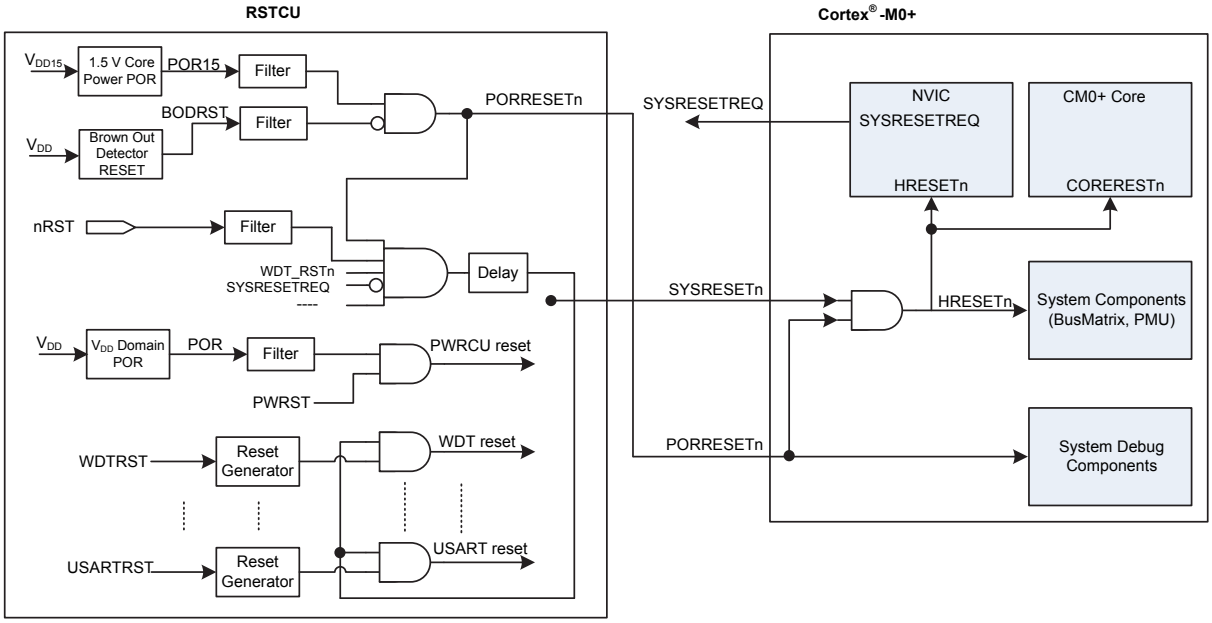


Figure 16. RSTCU Block Diagram

Functional Descriptions

Power On Reset

The Power on reset, POR, is generated by either an external reset or the internal reset generator. Both types have an internal filter to prevent glitches from causing erroneous reset operations. By referring to Figure 17, the POR15 active low signal will be de-asserted when the internal LDO voltage regulator is ready to provide 1.5 V power. In addition to the POR15 signal, the Power Control Unit, PWRCU, will assert the BODF signal as a Power Down Reset, PDR, when the BODEN bit in the LVDCSR register is set and the brown-out event occurs. For more details about the PWRCU function, refer to the PWRCU chapter.

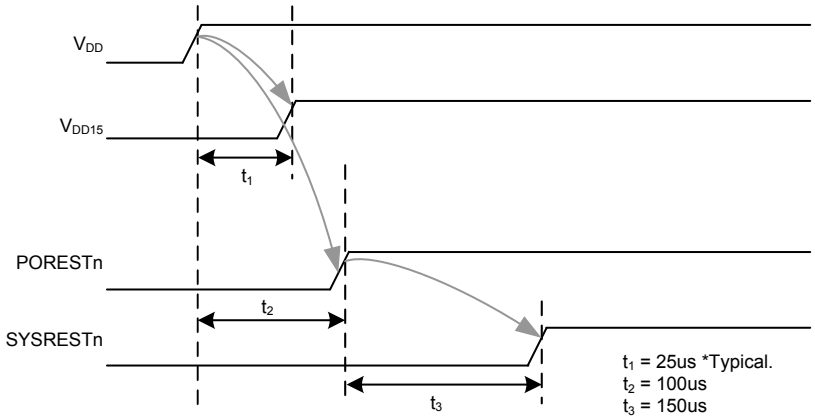


Figure 17. Power On Reset Sequence

System Reset

A system reset is generated by a power on reset (PORRESETn), a Watchdog Timer reset (WDT_RSTn), nRST pin or a software reset (SYSRESETREQ) event. For more information about SYSRESETREQ event, refer to the related chapter in the Cortex®-M0+ reference manual.

AHB and APB Unit Reset

The AHB and APB unit reset can be divided into hardware and software resets. A hardware reset can be generated by either power on reset or system reset for all AHB and APB units. Each functional IP connected to the AHB and APB buses can be reset individually through the associated software reset bits in the RSTCU. For example, the application software can generate a USART reset via the USRRST bit in the APBPRSTR0 register.

Register Map

The following table shows the RSTCU registers and reset values.

Table 19. RSTCU Register Map

Register	Offset	Description	Reset Value
RSTCU Base Address = 0x4008_8000			
GRSR	0x100	Global Reset Status Register	0x0000_0008
AHBPRSTR	0x104	AHB Peripheral Reset Register	0x0000_0000
APBPRSTR0	0x108	APB Peripheral Reset Register 0	0x0000_0000
APBPRSTR1	0x10C	APB Peripheral Reset Register 1	0x0000_0000

Register Descriptions

Global Reset Status Register – GRSR

This register specifies a variety of reset status conditions.

Offset: 0x100
Reset value: 0x0000_0008

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved				PORSTF	WDTRSTF	EXTRSTF	NVICRSTF
Type/Reset					WC 1	WC 0	WC 0	WC 0

Bits	Field	Descriptions
[3]	PORSTF	Core 1.5 V Power On Reset Flag 0: No POR occurred 1: POR occurred This bit is set by hardware when a power on reset occurs and reset by writing 1 into it.
[2]	WDTRSTF	Watchdog Timer Reset Flag 0: No Watchdog Timer reset occurred 1: Watchdog Timer occurred This bit is set by hardware when a watchdog timer reset occurs and reset by writing 1 into it or by hardware when a power on reset occurs.
[1]	EXTRSTF	External Pin Reset Flag 0: No pin reset occurred 1: Pin reset occurred This bit is set by hardware when an external pin reset occurs and reset by writing 1 into it or by hardware when a power on reset occurs.

Bits	Field	Descriptions
[0]	NVICRSTF	NVIC Reset Flag 0: No NVIC asserting system reset occurred 1: NVIC asserting system reset occurred This bit is set by hardware when a system reset occurs and reset by writing 1 into it or by hardware when a power on reset occurs.

AHB Peripheral Reset Register – AHBPRSTR

This register specifies several AHB peripherals software reset control bits.

Offset: 0x104
Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved						PBRST	PARST
Type/Reset							RW 0	RW 0
	7	6	5	4	3	2	1	0
	Reserved							
Type/Reset								

Bits	Field	Descriptions
[9]	PBRST	GPIO Port B Reset Control 0: No reset 1: Reset Port B This bit is set by software and cleared to 0 by hardware automatically.
[8]	PARST	GPIO Port A Reset Control 0: No reset 1: Reset Port A This bit is set by software and cleared to 0 by hardware automatically.

APB Peripheral Reset Register 0 – APBPRSTR0

This register specifies several APB peripherals software reset control bits.

Offset: 0x108

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	EXTIRST	AFIORST	Reserved			URRST	Reserved	USRRST
Type/Reset	RW 0	RW 0				RW 0		RW 0
	7	6	5	4	3	2	1	0
	Reserved			SPIRST	Reserved			I2CRST
Type/Reset				RW 0				RW 0

Bits	Field	Descriptions
[15]	EXTIRST	External Interrupt Controller Reset Control 0: No reset 1: Reset EXTI This bit is set by software and cleared to 0 by hardware automatically.
[14]	AFIORST	Alternate Function I/O Reset Control 0: No reset 1: Reset Alternate Function I/O This bit is set by software and cleared to 0 by hardware automatically.
[10]	URRST	UART Reset Control 0: No reset 1: Reset UART This bit is set by software and cleared to 0 by hardware automatically.
[8]	USRRST	USART Reset Control 0: No reset 1: Reset USART This bit is set by software and cleared to 0 by hardware automatically.
[4]	SPIRST	SPI Reset Control 0: No reset 1: Reset SPI This bit is set by software and cleared to 0 by hardware automatically.
[0]	I2CRST	I^2C Reset Control 0: No reset 1: Reset I^2C This bit is set by software and cleared to 0 by hardware automatically.

APB Peripheral Reset Register 1 – APBPRSTR1

This register specifies several APB peripherals software reset control bits.

Offset: 0x10C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved		SCTM1RST	SCTM0RST	Reserved			ADCRST
Type/Reset			RW 0	RW 0				RW 0
	23	22	21	20	19	18	17	16
	Reserved							BFTMRST
Type/Reset								RW 0
	15	14	13	12	11	10	9	8
	Reserved							GPTMRST
Type/Reset								RW 0
	7	6	5	4	3	2	1	0
	Reserved			WDTRST	Reserved			
Type/Reset				RW 0				

Bits	Field	Descriptions
[29]	SCTM1RST	SCTM1 Reset Control 0: No reset 1: Reset SCTM1 This bit is set by software and cleared to 0 by hardware automatically.
[28]	SCTM0RST	SCTM0 Reset Control 0: No reset 1: Reset SCTM0 This bit is set by software and cleared to 0 by hardware automatically.
[24]	ADCRST	A/D Converter Reset Control 0: No reset 1: Reset A/D Converter This bit is set by software and cleared to 0 by hardware automatically.
[16]	BFTMRST	BFTM Reset Control 0: No reset 1: Reset BFTM This bit is set by software and cleared to 0 by hardware automatically.
[8]	GPTMRST	GPTM Reset Control 0: No reset 1: Reset GPTM This bit is set by software and cleared to 0 by hardware automatically.
[4]	WDTRST	Watchdog Timer Reset Control 0: No reset 1: Reset Watchdog Timer This bit is set by software and cleared to 0 by hardware automatically.

8 General Purpose I/O (GPIO)

Introduction

There are up to 23 General Purpose I/O port, GPIO, named PA0~PA7, PA9, PA12~PA15, PB0~PB4, PB7~PB8 and PB12~PB14 for the device to implement the logic input/output functions. Each of the GPIO ports has related control and configuration registers to satisfy the requirement of specific applications. The actual available General Purpose I/O port numbers are dependent on the device specification and package type. Refer to the device datasheet for detailed information.

The GPIO ports are pin-shared with other alternative functions (AFs) to obtain maximum flexibility on the package pins. The GPIO pins can be used as alternative functional pins by configuring the corresponding registers regardless of the AF input or output pins.

The external interrupts on the GPIO pins of the device have related control and configuration registers in the External Interrupt Control Unit (EXTI).

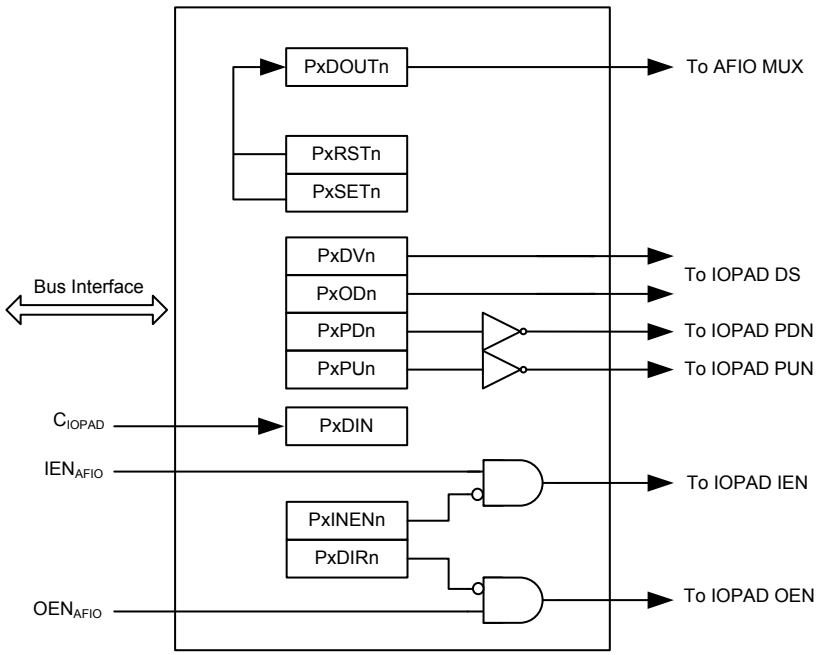


Figure 18. GPIO Block Diagram

Features

- Input/output direction control
- Schmitt Trigger Input function enable control
- Input weak pull-up/pull-down control
- Output push-pull/open drain enable control
- Output set/reset control
- Output drive current selection
- External interrupt with programmable trigger edge – using EXTI configuration registers
- Analog input/output configurations – using AFIO configuration registers
- Alternate function input/output configurations – using AFIO configuration registers
- Port configuration lock

Functional Descriptions

Default GPIO Pin Configuration

During or just after the reset period, the alternative functions are all inactive and the GPIO ports are configured into the input disable floating mode, i.e. input disabled without pull-up/pull-down resistors. Only the boot and Serial-Wired Debug pins which are pin-shared with the I/O pins are active after a device reset.

- PA9_BOOT: Input enable with internal pull-up
- SWCLK: Input enable with internal pull-up
- SWDIO: Input enable with internal pull-up

General Purpose I/O – GPIO

The GPIO pins can be configured as inputs or outputs via the data direction control registers PxDIRCR (where x = A ~ B). When the GPIO pins are configured as input pins, the data on the external pads can be read if the enable bits in the input enable function register PxINER are set. The GPIO pull-up/pull-down registers PxPUR/PxPDR can be configured to fit specific applications. When the pull-up and pull-down functions are both enabled, the pull-up function has the higher priority while the pull-down function will be blocked until the pull-up function is released.

The GPIO pins can be configured as output pins where the output data is latched into the data register PxDOUTR. The output type can be setup to be either push-pull or open-drain by the open drain selection register PxODR. Only one or several specific bits of the output data will be set or reset by configuring the port output set and reset control register PxSRR or the port output reset control register PxRR without affecting the unselected bits. As the port output set and reset functions are both enabled, the port output set function has the higher priority and the port output reset function will be blocked. The output driving current of the GPIO pins can be selected by configuring the drive current selection register PxDRVR.

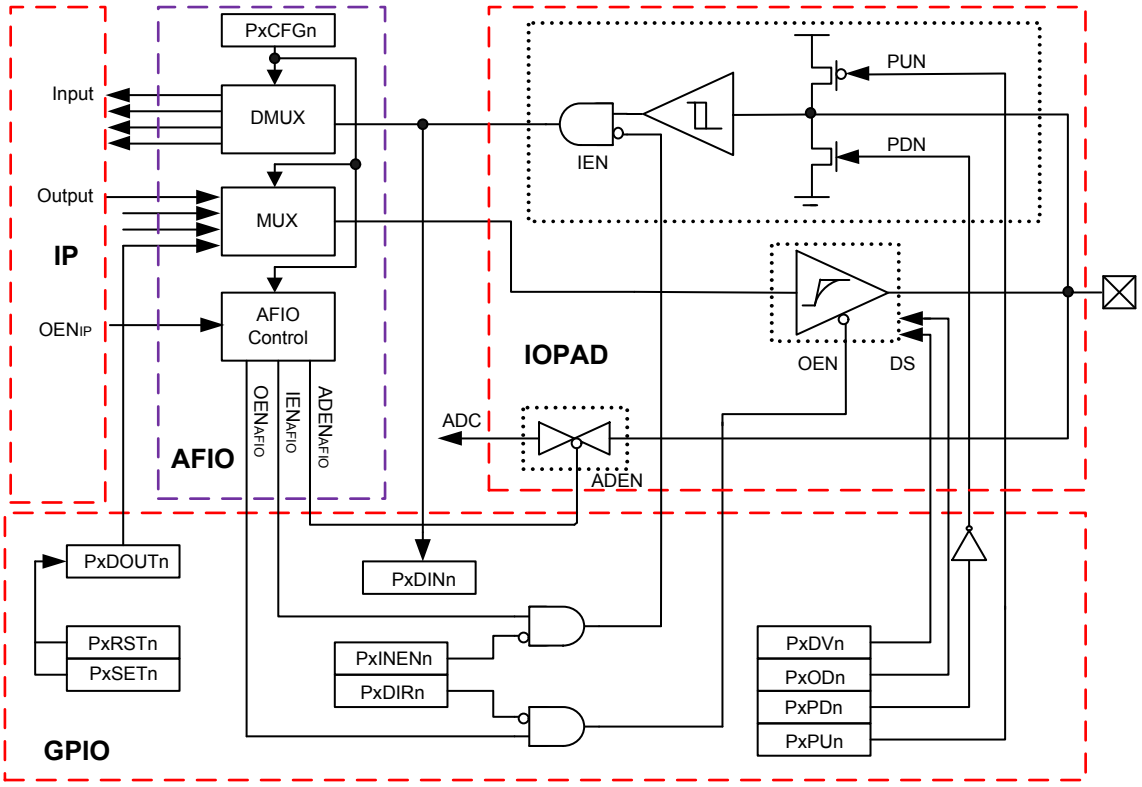


Figure 19. AFIO/GPIO Control Signal

PxDINn/PxDOUTn (x=A ~ B): Data Input/Data Output

PxRSTn/PxSETn (x=A ~ B): Reset/Set

PxDIRn (x=A ~ B): Direction

PxINENn (x=A ~ B): Input Enable

PxDVn (x=A ~ B): Output Drive

PxODn (x=A ~ B): Open Drain

PxPDn/PxPUn (x=A ~ B): Pull Down/Up

PxCFGn (x=A ~ B): AFIO Configuration

Table 20. AFIO, GPIO and IO Pad Control Signal True Table

Type	AFIO			GPIO		PAD		
	$ADEN_{AFIO}$	OEN_{AFIO}	IEN_{AFIO}	PxDIRn	PxINENn	ADEN	OEN	IEN
GPIO Input (Note)	1	1	1	0	1	1	1	0
GPIO Output (Note)	1	1	1	1	0 (1 if need)	1	0	1 (0)
AFIO Input	1	1	0	0	X	1	1	0
AFIO Output	1	0	1	X	0 (1 if need)	1	0	1 (0)
ADC Input	0	1	1	0	0 (1 if need)	0	1	1 (0)
OSC Output	0	1	1	0	0 (1 if need)	0	1	1 (0)

Note: The signals, IEN and OEN, for I/O pads are derived from the GPIO register bits PxINENn and PxDIRn respectively when the associated pin is configured in the GPIO input/output mode.

GPIO Locking Mechanism

The GPIO also offers a lock function to lock the port until a reset event occurs. The PxLOCKR (x = A ~ B) registers are used to lock the port x and lock control options. The value 0x5FA0 is written into the PxLKEY field in the PxLOCKR registers to freeze the PxDIRCR, PxINER, PxPUR, PxPDR, PxODR, PxDRVR control and AFIO mode configuration (GPxCFGHR or GPxCFGLR, where x = A ~ B). If the value in the PxLOCKR register is 0x5FA0_0001, it means that the Port x Lock function is enabled and the Port x pin 0 is frozen

Register Map

The following table shows the GPIO registers and reset values of the Port A ~ B.

Table 21. GPIO Register Map

Register	Offset	Description	Reset Value
GPIO A Base Address = 0x400B_0000			
PADIRCR	0x000	Port A Data Direction Control Register	0x0000_0000
PAINER	0x004	Port A Input Function Enable Control Register	0x0000_0200
PAPUR	0x008	Port A Pull-Up Selection Register	0x0000_3200
PAPDR	0x00C	Port A Pull-Down Selection Register	0x0000_0000
PAODR	0x010	Port A Open Drain Selection Register	0x0000_0000
PADRVR	0x014	Port A Drive Current Selection Register	0x0000_0000
PALOCKR	0x018	Port A Lock Register	0x0000_0000
PADINR	0x01C	Port A Data Input Register	0x0000_3200
PADOUTR	0x020	Port A Data Output Register	0x0000_0000
PASRR	0x024	Port A Output Set and Reset Control Register	0x0000_0000
PARR	0x028	Port A Output Reset Control Register	0x0000_0000
GPIO B Base Address = 0x400B_2000			
PBDIRCR	0x000	Port B Data Direction Control Register	0x0000_0000
PBINER	0x004	Port B Input Function Enable Control Register	0x0000_0000
PBPUR	0x008	Port B Pull-Up Selection Register	0x0000_0000
PBPDR	0x00C	Port B Pull-Down Selection Register	0x0000_0000
PBODR	0x010	Port B Open Drain Selection Register	0x0000_0000
PBDRVR	0x014	Port B Drive Current Selection Register	0x0000_0000
PBLOCKR	0x018	Port B Lock Register	0x0000_0000
PBDINR	0x01C	Port B Data Input Register	0x0000_0000
PBDOUTR	0x020	Port B Data Output Register	0x0000_0000
PBSRR	0x024	Port B Output Set and Reset Control Register	0x0000_0000
PBRR	0x028	Port B Output Reset Control Register	0x0000_0000

Register Descriptions

Port A Data Direction Control Register – PADIRCR

This register is used to control the direction of the GPIO Port A pin as input or output.

Offset: 0x000
Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	PADIR				Reserved		PADIR	Reserved
Type/Reset	RW 0	RW 0	RW 0	RW 0			RW 0	
	7	6	5	4	3	2	1	0
	PADIR							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:12], [9], [7:0]	PADIRn	GPIO Port A pin n Direction Control Bits (n = 0 ~ 7, 9, 12 ~ 15) 0: Pin n is input mode 1: Pin n is output mode

Port A Input Function Enable Control Register – PAINER

This register is used to enable or disable the GPIO Port A input function.

Offset: 0x004

Reset value: 0x0000_0200

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	PAINEN				Reserved		PAINEN	Reserved
Type/Reset	RW 0	RW 0	RW 0	RW 0			RW 1	
	7	6	5	4	3	2	1	0
	PAINEN							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:12], [9], [7:0]	PAINENn	GPIO Port A pin n Input Enable Control Bits (n = 0 ~ 7, 9, 12 ~ 15) 0: Pin n input function is disabled 1: Pin n input function is enabled When the pin n input function is disabled, the input Schmitt trigger will be turned off and the Schmitt trigger output will remain at a zero state.

Port A Pull-Up Selection Register – PAPUR

This register is used to enable or disable the GPIO Port A pull-up function.

Offset: 0x008

Reset value: 0x0000_3200

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	PAPU				Reserved		PAPU	Reserved
Type/Reset	RW 0	RW 0	RW 1	RW 1			RW 1	
	7	6	5	4	3	2	1	0
	PAPU							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:12], [9], [7:0]	PAPUn	GPIO Port A pin n Pull-Up Selection Control Bits (n = 0 ~ 7, 9, 12 ~ 15) 0: Pin n pull-up function is disabled 1: Pin n pull-up function is enabled Note: When the pull-up and pull-down functions are both enabled, the pull-up function will have the higher priority and therefore the pull-down function will be blocked and disabled.

Port A Pull-Down Selection Register – PAPDR

This register is used to enable or disable the GPIO Port A pull-down function.

Offset: 0x00C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	PAPD				Reserved		PAPD	Reserved
Type/Reset	RW 0	RW 0	RW 0	RW 0			RW 0	
	7	6	5	4	3	2	1	0
	PAPD							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:12], [9], [7:0]	PAPDn	GPIO Port A pin n Pull-Down Selection Control Bits (n = 0 ~ 7, 9, 12 ~ 15) 0: Pin n pull-down function is disabled 1: Pin n pull-down function is enabled Note: When the pull-up and pull-down functions are both enabled, the pull-up function will have the higher priority and therefore the pull-down function will be blocked and disabled.

Port A Open Drain Selection Register – PAODR

This register is used to enable or disable the GPIO Port A open drain function.

Offset: 0x010

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	PAOD				Reserved		PAOD	Reserved
Type/Reset	RW 0	RW 0	RW 0	RW 0			RW 0	
	7	6	5	4	3	2	1	0
	PAOD							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:12], [9], [7:0]	PAODn	GPIO Port A pin n Open Drain Selection Control Bits (n = 0 ~ 7, 9, 12 ~ 15) 0: Pin n Open Drain output is disabled. (The output type is CMOS output) 1: Pin n Open Drain output is enabled. (The output type is open-drain output)

Port A Output Current Drive Selection Register – PADRVR

This register specifies the GPIO Port A output driving current.

Offset: 0x014

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	PADV15		PADV14		PADV13		PADV12	
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	23	22	21	20	19	18	17	16
	Reserved				PADV9		Reserved	
Type/Reset					RW 0	RW 0		
	15	14	13	12	11	10	9	8
	PADV7		PADV6		PADV5		PADV4	
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	PADV3		PADV2		PADV1		PADV0	
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[31:24], [19:18], [15:0]	PADVn[1:0]	GPIO Port A pin n Output Current Drive Selection Control Bits (n = 0 ~ 7, 9, 12 ~ 15) 00: 4 mA source/sink current 01: 8 mA source/sink current 10: 12 mA source/sink current 11: 16 mA source/sink current

Port A Lock Register – PALOCKR

This register specifies the GPIO Port A lock configuration.

Offset: 0x018

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	PALKEY							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	PALKEY							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PALOCK				Reserved		PALOCK	Reserved
Type/Reset	RW 0	RW 0	RW 0	RW 0			RW 0	
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	PALOCK							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[31:16]	PALKEY	GPIO Port A Lock Key 0x5FA0: Port A Lock function is enable Others: Port A Lock function is disable To lock the Port A function, a value 0x5FA0 should be written into the PALKEY field in this register. To execute a successful write operation on this lock register, the value written into the PALKEY field must be 0x5FA0. If the value written into this field is not equal to 0x5FA0, any write operations on the PALOCKR register will be aborted. The result of a read operation on the PALKEY field returns the GPIO Port A Lock Status which indicates whether the GPIO Port A is locked or not. If the read value of the PALKEY field is 0, this indicates that the GPIO Port A Lock function is disabled. Otherwise, it indicates that the GPIO Port A Lock function is enabled as the read value is equal to 1.
[15:12], [9], [7:0]	PALOCKn	GPIO Port A Pin n Lock Control Bits (n = 0 ~ 7, 9, 12 ~ 15) 0: Port A Pin n is not locked 1: Port A Pin n is locked The PALOCKn bits are used to lock the configurations of corresponding GPIO Pins when the correct Lock Key is applied to the PALKEY field. The locked configurations including PADIRn, PAINENn, PAPUn, PAPDn, PAODn and PADVn setting in the related GPIO registers. Additionally, the GPACFGHR or GPACFGLR field which is used to configure the alternative function of the associated GPIO pin will also be locked. Note that the PALOCKR can only be written once which means that PALKEY and PALOCKn (lock control bit) should be written together and can not be changed until a system reset or GPIO Port A reset occurs.

Port A Data Input Register – PADINR

This register specifies the GPIO Port A input data.

Offset: 0x01C

Reset value: 0x0000_3200

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	PADIN				Reserved		PADIN	Reserved
Type/Reset	RO	RO	RO	RO			RO	
	0	0	1	1			1	
	7	6	5	4	3	2	1	0
	PADIN							
Type/Reset	RO	RO	RO	RO	RO	RO	RO	RO
	0	0	0	0	0	0	0	0

Bits	Field	Descriptions
[15:12], [9], [7:0]	PADINn	GPIO Port A pin n Data Input Bits (n = 0 ~ 7, 9, 12 ~ 15) 0: The input data of pin n is 0 1: The input data of pin n is 1

Port A Output Data Register – PADOUTR

This register specifies the GPIO Port A output data.

Offset: 0x020

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	PADOUT				Reserved		PADOUT	Reserved
Type/Reset	RW 0	RW 0	RW 0	RW 0			RW 0	
	7	6	5	4	3	2	1	0
	PADOUT							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:12], [9], [7:0]	PADOUTn	GPIO Port A pin n Data Output Bits (n = 0 ~ 7, 9, 12 ~ 15) 0: Data to be output on pin n is 0 1: Data to be output on pin n is 1

Port A Output Set/Reset Control Register – PASRR

This register is used to set or reset the corresponding bit of the GPIO Port A output data.

Offset: 0x024

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	PARST				Reserved		PARST	Reserved
Type/Reset	WO 0	WO 0	WO 0	WO 0			WO 0	
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	PARST							
Type/Reset	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	PASET				Reserved		PASET	Reserved
Type/Reset	WO 0	WO 0	WO 0	WO 0			WO 0	
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	PASET							
Type/Reset	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0

Bits	Field	Descriptions
[31:28], [25], [23:16]	PARSTn	GPIO Port A pin n Output Reset Control Bits (n = 0 ~ 7, 9, 12 ~ 15) 0: No effect on the PADOUTn bit 1: Reset the PADOUTn bit
[15:12], [9], [7:0]	PASETn	GPIO Port A pin n Output Set Control Bits (n = 0 ~ 7, 9, 12 ~ 15) 0: No effect on the PADOUTn bit 1: Set the PADOUTn bit Note that the function enabled by the PASETn bit has the higher priority if both the PASETn and PARSTn bits are set at the same time.

Port A Output Reset Register – PARR

This register is used to reset the corresponding bit of the GPIO Port A output data.

Offset: 0x028

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	PARST				Reserved		PARST	Reserved
Type/Reset	WO 0	WO 0	WO 0	WO 0			WO 0	
	7	6	5	4	3	2	1	0
	PARST							
Type/Reset	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0

Bits	Field	Descriptions
[15:12], [9], [7:0]	PARSTn	GPIO Port A pin n Output Reset Bits (n = 0 ~ 7, 9, 12 ~ 15) 0: No effect on the PADOUTn bit 1: Reset the PADOUTn bit

Port B Data Direction Control Register – PBDIRCR

This register is used to control the direction of GPIO Port B pin as input or output.

Offset: 0x000

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved	PBDIR			Reserved			PBDIR
Type/Reset		RW 0	RW 0	RW 0				RW 0
	7	6	5	4	3	2	1	0
	PBDIR	Reserved		PBDIR				
Type/Reset	RW 0			RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[14:12], [8:7] [4:0]	PBDIRn	GPIO Port B pin n Direction Control Bits (n = 0 ~ 4, 7 ~ 8, 12 ~ 14) 0: Pin n is input mode 1: Pin n is output mode

Port B Input Function Enable Control Register – PBINER

This register is used to enable or disable the GPIO Port B input function.

Offset: 0x004

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved	PBINEN			Reserved			PBINEN
Type/Reset		RW 0	RW 0	RW 0				RW 0
	7	6	5	4	3	2	1	0
	PBINEN	Reserved		PBINEN				
Type/Reset	RW 0			RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[14:12], [8:7] [4:0]	PBINENn	GPIO Port B pin n Input Enable Control Bits (n = 0 ~ 4, 7 ~ 8, 12 ~ 14) 0: Pin n input function is disabled 1: Pin n input function is enabled When the pin n input function is disabled, the input Schmitt trigger will be turned off and the Schmitt trigger output will remain at a zero state.

Port B Pull-Up Selection Register – PBPUR

This register is used to enable or disable the GPIO Port B pull-up function.

Offset: 0x008

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved	PBPU			Reserved			PBPU
Type/Reset		RW 0	RW 0	RW 0				RW 0
	7	6	5	4	3	2	1	0
	PBPU	Reserved		PBPU				
Type/Reset	RW 0			RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[14:12], [8:7] [4:0]	PBPUn	GPIO Port B pin n Pull-Up Selection Control Bits (n = 0 ~ 4, 7 ~ 8, 12 ~ 14) 0: Pin n pull-up function is disabled 1: Pin n pull-up function is enabled Note: When the pull-up and pull-down functions are both enabled, the pull-up function will have the higher priority and therefore the pull-down function will be blocked and disabled.

Port B Pull-Down Selection Register – PBPDR

This register is used to enable or disable the GPIO Port B pull-down function.

Offset: 0x00C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved	PBPD			Reserved			PBPD
Type/Reset		RW 0	RW 0	RW 0				RW 0
	7	6	5	4	3	2	1	0
	PBPD	Reserved		PBPD				
Type/Reset	RW 0			RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[14:12], [8:7] [4:0]	PBPDn	GPIO Port B pin n Pull-Down Selection Control Bits (n = 0 ~ 4, 7 ~ 8, 12 ~ 14) 0: Pin n pull-down function is disabled 1: Pin n pull-down function is enabled Note: When the pull-up and pull-down functions are both enabled, the pull-up function will have the higher priority and therefore the pull-down function will be blocked and disabled.

Port B Open Drain Selection Register – PBODR

This register is used to enable or disable the GPIO Port B open drain function.

Offset: 0x010

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved	PBOD			Reserved			PBOD
Type/Reset		RW 0	RW 0	RW 0				RW 0
	7	6	5	4	3	2	1	0
	PBOD	Reserved		PBOD				
Type/Reset	RW 0			RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[14:12], [8:7] [4:0]	PBODn	GPIO Port B pin n Open Drain Selection Control Bits (n = 0 ~ 4, 7 ~ 8, 12 ~ 14) 0: Pin n Open Drain output is disabled. (The output type is CMOS output) 1: Pin n Open Drain output is enabled. (The output type is open-drain output)

Port B Output Current Drive Selection Register – PBDRVR

This register specifies the GPIO Port B output driving current.

Offset: 0x014

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved		PBDV14		PBDV13		PBDV12	
Type/Reset			RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	23	22	21	20	19	18	17	16
	Reserved						PBDV8	
Type/Reset							RW 0	RW 0
	15	14	13	12	11	10	9	8
	PBDV7		Reserved				PBDV4	
Type/Reset	RW 0	RW 0					RW 0	RW 0
	7	6	5	4	3	2	1	0
	PBDV3		PBDV2		PBDV1		PBDV0	
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[29:24], [17:14], [9:0]	PBDVn[1:0]	GPIO Port B pin n Output Current Drive Selection Control Bits (n = 0 ~ 4, 7 ~ 8, 12 ~ 14) 00: 4 mA source/sink current 01: 8 mA source/sink current 10: 12 mA source/sink current 11: 16 mA source/sink current

Port B Lock Register – PBLOCKR

This register specifies the GPIO Port B lock configuration.

Offset: 0x018

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	PBLKEY							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	PBLKEY							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	Reserved	PBLOCK			Reserved			PBLOCK
Type/Reset		RW 0	RW 0	RW 0				RW 0
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	PBLOCK	Reserved		PBLOCK				
Type/Reset	RW 0			RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[31:16]	PBLKEY	GPIO Port Block Key 0x5FA0: Port Block function is enable Others: Port B Lock function is disable To lock the Port B function, a value 0x5FA0 should be written into the PBLKEY field in this register. To execute a successful write operation on this lock register, the value written into the PBLKEY field must be 0x5FA0. If the value written into this field is not equal to 0x5FA0, any write operations on the PBLOCKR register will be aborted. The result of a read operation on the PBLKEY field returns the GPIO Port B Lock Status which indicates whether the GPIO Port B is locked or not. If the read value of the PBLKEY field is 0, this indicates that the GPIO Port B Lock function is disabled. Otherwise, it indicates that the GPIO Port B Lock function is enabled as the read value is equal to 1.
[14:12], [8:7] [4:0]	PBLOCKn	GPIO Port B pin n Lock Control Bits (n = 0 ~ 4, 7 ~ 8, 12 ~ 14) 0: Port B pin n is not locked 1: Port B pin n is locked The PBLOCKn bits are used to lock the configurations of corresponding GPIO Pins when the correct Lock Key is applied to the PBLKEY field. The locked configurations including PBDIRn, PBINENn, PBPUn, PBPDn and PBODn setting in the related GPIO registers. Additionally, the GPBCFGHR or GPBCFGLR field which is used to configure the alternative function of the associated GPIO pin will also be locked. Note that the PBLOCKR can only be written once which means that PBLKEY and PBLOCKn (lock control bit) should be written together and can not be changed until a system reset or GPIO Port B reset occurs.

Port B Data Input Register – PBDINR

This register specifies the GPIO Port B input data.

Offset: 0x01C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved	PBDIN			Reserved			PBDIN
Type/Reset		RO	0 RO	0 RO	0			RO 0
	7	6	5	4	3	2	1	0
	PBDIN	Reserved		PBDIN				
Type/Reset	RO 0			RO	0 RO	0 RO	0 RO	0 RO 0

Bits	Field	Descriptions
[14:12], [8:7] [4:0]	PBDINn	GPIO Port B pin n Data Input Bits (n = 0 ~ 4, 7 ~ 8, 12 ~ 14) 0: The input data of pin n is 0 1: The input data of pin n is 1

Port B Output Data Register – PBDOUTR

This register specifies the GPIO Port B output data.

Offset: 0x020

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved	PBDOUT			Reserved			PBDOUT
Type/Reset		RW 0	RW 0	RW 0				RW 0
	7	6	5	4	3	2	1	0
	PBDOUT	Reserved		PBDOUT				
Type/Reset	RW 0			RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[14:12], [8:7] [4:0]	PBDOUTn	GPIO Port B pin n Data Output Bits (n = 0 ~ 4, 7 ~ 8, 12 ~ 14) 0: Data to be output on pin n is 0 1: Data to be output on pin n is 1

Port B Output Set/Reset Control Register – PBSRR

This register is used to set or reset the corresponding bit of the GPIO Port B output data.

Offset: 0x024

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved	PBRST			Reserved			PBRST
Type/Reset		WO 0	WO 0	WO 0				WO 0
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	PBRST	Reserved		PBRST				
Type/Reset	WO 0			WO 0	WO 0	WO 0	WO 0	WO 0
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	Reserved	PBSET			Reserved			PBSET
Type/Reset		WO 0	WO 0	WO 0				WO 0
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	PBSET	Reserved		PBSET				
Type/Reset	WO 0			WO 0	WO 0	WO 0	WO 0	WO 0

Bits	Field	Descriptions
[30:28], [24:23] [20:16]	PBRSTn	GPIO Port B pin n Output Reset Control Bits (n = 0 ~ 4, 7 ~ 8, 12 ~ 14) 0: No effect on the PBDOUTn bit 1: Reset the PBDOUTn bit
[14:12], [8:7] [4:0]	PBSETn	GPIO Port B pin n Output Set Control Bits (n = 0 ~ 4, 7 ~ 8, 12 ~ 14) 0: No effect on the PBDOUTn bit 1: Set the PBDOUTn bit Note that the function enabled by the PBSETn bit has the higher priority if both the PBSETn and PBRSTn bits are set at the same time.

Port B Output Reset Register – PBRR

This register is used to reset the corresponding bit of the GPIO Port B output data.

Offset: 0x028

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved	PBRST			Reserved			PBRST
Type/Reset		WO 0	WO 0	WO 0				WO 0
	7	6	5	4	3	2	1	0
	PBRST	Reserved		PBRST				
Type/Reset	WO 0			WO 0	WO 0	WO 0	WO 0	WO 0

Bits	Field	Descriptions
[14:12], [8:7] [4:0]	PBRSTn	GPIO Port B pin n Output Reset Bits (n = 0 ~ 4, 7 ~ 8, 12 ~ 14) 0: No effect on the PBDOUTn bit 1: Reset the PBDOUTn bit

9 Alternate Function Input/Output Control Unit (AFIO)

Introduction

In order to expand the flexibility of the GPIO or the usage of peripheral functions, each IO pin can be configured to have up to sixteen different functions such as GPIO or IP functions by setting the GPxCFGLR or GPxCFGHR register where x is the different port name. According to the usage of the IP resource and application requirements, suitable pin-out locations can be selected by using the peripheral IO remapping mechanism. Additionally, various GPIO pins can be selected to be the EXTI interrupt line by setting the EXTInPIN [3:0] field in the ESSRn register to trigger an interrupt or event. Please refer to the EXTI section for more details.

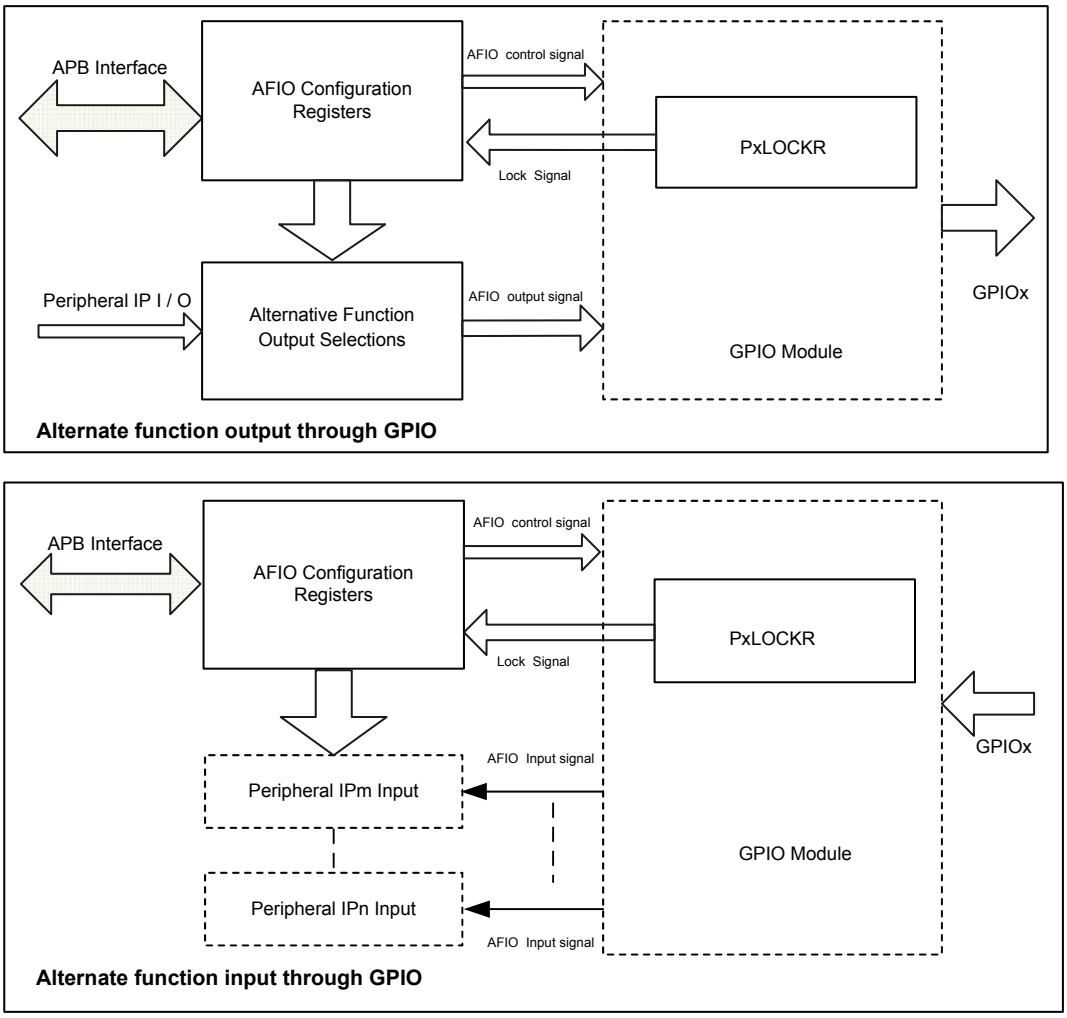


Figure 20. AFIO Block Diagram

Features

- APB slave interface for register access
- EXTI source selection
- Configurable pin function for each GPIO, up to sixteen alternative functions on each pin
- AFIO lock mechanism

Functional Descriptions

External Interrupt Pin Selection

The GPIO pins are connected to the 16 EXTI lines as shown in the accompanying figure. For example, the user can set the EXTI0PIN [3:0] field in the ESSR0 register to b0000 to select the GPIO PA0 pin as EXTI line 0 input. Since not all the pins of the Port A ~ B pins are available in all package types, please refer to the pin assignment section for detailed pin information. The setting of the EXTInPIN [3:0] field is invalid when the corresponding pin is not available.

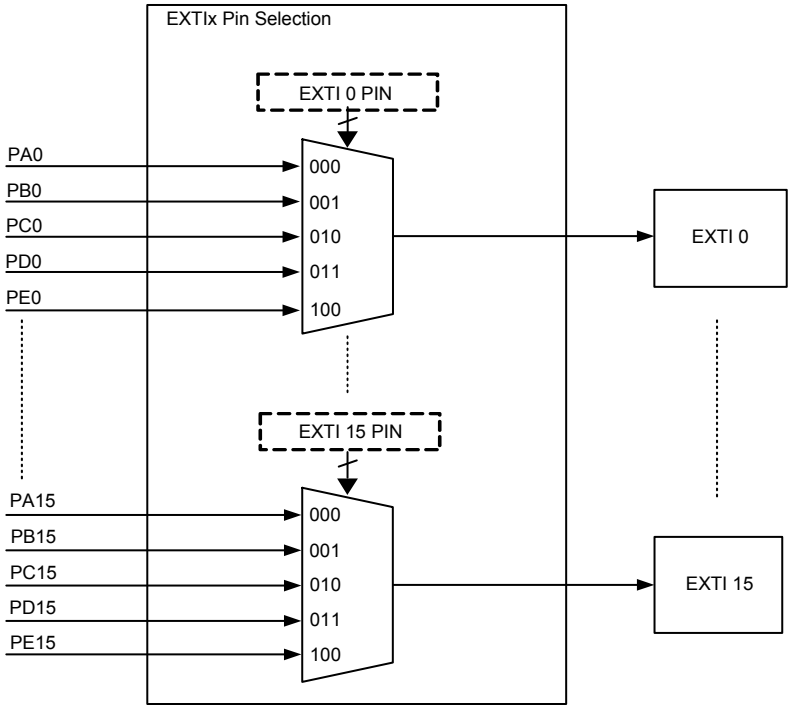


Figure 21. EXTI Channel Input Selection

Alternate Function

Up to sixteen alternative functions can be chosen for each I/O pad by setting the PxCFGn [3:0] field in the GPxCFGLR or GPxCFGHR (n = 0~15, x = A~ B) registers. If the pin is selected as an unavailable item which is noted as a "N/A" item in the "Alternate Function Mapping" table in the device datasheet, this pin will be defined as default alternate function. Please refer to the "Alternate Function Mapping" table in the device datasheet for the detailed mapping of the alternate function I/O pins. In addition to this flexible I/O multiplexing architecture, each peripheral has alternate functions mapped onto different I/O pins to optimize the number of peripherals available in smaller packages. The following description shows the setting of the PxCFGn [3:0] field.

- PxCFGn [3:0] = 0000: The default alternated function (after reset, AF0)
- PxCFGn [3:0] = 0001: Alternate Function 1 (AF1)
- PxCFGn [3:0] = 0010: Alternate Function 2 (AF2)

  …….
- PxCFGn [3:0] = 1110: Alternate Function 14 (AF14)
- PxCFGn [3:0] = 1111: Alternate Function 15 (AF15)

Table 22. AFIO Selection for Peripheral Map Example

AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
System Default	GPIO	ADC	N/A	GPTM	SPI	USART /UART	I²C	N/A	N/A	N/A	N/A	N/A	SCTM	N/A	System Other

Lock Mechanism

The device also offers a lock function to lock the AFIO configuration using the GPIO lock register, PxLOCKR, until a reset event occurs. Refer to the GPIO Locking Mechanism section in the GPIO chapter for more details.

Register Map

The following table shows the AFIO registers and reset value.

Table 23. AFIO Register Map

Register	Offset	Description	Reset Value
ESSR0	0x000	EXTI Source Selection Register 0	0x0000_0000
ESSR1	0x004	EXTI Source Selection Register 1	0x0000_0000
GPACFGLR	0x020	GPIO Port A AFIO Configuration Register 0	0x0000_0000
GPACFGHR	0x024	GPIO Port A AFIO Configuration Register 1	0x0000_0000
GPBCFGLR	0x028	GPIO Port B AFIO Configuration Register 0	0x0000_0000
GPBCFGHR	0x02C	GPIO Port B AFIO Configuration Register 1	0x0000_0000

Register Descriptions

EXTI Source Selection Register 0 – ESSR0

This register specifies the IO selection of EXTI0 ~ EXTI7.

Offset: 0x000

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	EXTI7PIN				EXTI6PIN			
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	EXTI5PIN				EXTI4PIN			
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	EXTI3PIN				EXTI2PIN			
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	EXTI1PIN				EXTI0PIN			
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[31:0]	EXTInPIN[3:0]	EXTIn Pin Selection (n = 0 ~ 7) 0000: PA Bit n is selected as EXTIn source signal 0001: PB Bit n is selected as EXTIn source signal Others: Reserved Note: Since not all GPIO pins are available in all products and package types, refer to the pin assignment section for detailed pin information. The EXTInPIN [3:0] field setting is invalid when the corresponding pin is not available.

EXTI Source Selection Register 1 – ESSR1

This register specifies the IO selection of EXTI8~EXTI15.

Offset: 0x004

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	EXTI15PIN				EXTI14PIN			
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	23	22	21	20	19	18	17	16
	EXTI13PIN				EXTI12PIN			
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
	EXTI11PIN				EXTI10PIN			
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	EXTI9PIN				EXTI8PIN			
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[31:0]	EXTInPIN[3:0]	EXTIn Pin Selection (n = 8 ~ 15) 0000: PA Bit n is selected as EXTIn source signal 0001: PB Bit n is selected as EXTIn source signal Others: Reserved Note: Since not all GPIO pins are available in all products and package types, refer to the pin assignment section for detailed pin information. The EXTInPIN [3:0] field setting is invalid when the corresponding pin is not available.

GPIO x Configuration Low Register – GPxCFGLR, x = A, B

This low register specifies the alternate function of GPIO Port x. x = A, B

Offset: 0x020, 0x028

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	PxCFG7				PxCFG6			
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	23	22	21	20	19	18	17	16
	PxCFG5				PxCFG4			
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
	PxCFG3				PxCFG2			
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	PxCFG1				PxCFG0			
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[31:0]	PxCFGn[3:0]	Port x Pin n Alternate function selection (n = 0~7) 0000: Port x pin n is selected as AF0 0001: Port x pin n is selected as AF1 . . 1110: Port x pin n is selected as AF14 1111: Port x pin n is selected as AF15 If the pin is selected as an unavailable item which is noted as a “N/A” item in the “Alternate Function Mapping” table in the device datasheet, this pin will be defined as the default alternate function. Please refer to the “Alternate Function Mapping” table in the device datasheet for the detailed mapping of the alternate function I/O pins.

GPIO x Configuration High Register – GPxCFGHR, x = A, B

This high register specifies the alternate function of GPIO Port x. x = A, B

Offset: 0x024, 0x02C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	PxCFG15				PxCFG14			
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	23	22	21	20	19	18	17	16
	PxCFG13				PxCFG12			
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
	PxCFG11				PxCFG10			
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	PxCFG9				PxCFG8			
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[31:0]	PxCFGn[3:0]	Port x Pin n Alternate function selection (n = 8~15) 0000: Port x pin n is selected as AF0 0001: Port x pin n is selected as AF1 . . 1110: Port x pin n is selected as AF14 1111: Port x pin n is selected as AF15 If the pin is selected as an unavailable item which is noted as a “N/A” item in the “Alternate Function Mapping” table in the device datasheet, this pin will be defined as the default alternate function. Please refer to the “Alternate Function Mapping” table in the device datasheet for the detailed mapping of the alternate function I/O pins.

10 Nested Vectored Interrupt Controller (NVIC)

Introduction

In order to reduce the latency and increase the interrupt processing efficiency, a tightly coupled integrated section, which is named as Nested Vectored Interrupt Controller (NVIC) is provided by the Cortex®-M0+. The NVIC controls the system exceptions and the peripheral interrupt which include functions such as the enable/disable control, priority, clear-pending, active status report, software trigger and vector table remapping. Refer to the Technical Reference Manual of Cortex®-M0+ for more details.

Additionally, an integrated simple, 24-bit down count timer (SysTick) is provided by the Cortex®-M0+ to be used as a tick timer for the Real Timer Operation System (RTOS) or as a simple counter. The SysTick counts down from the reloaded value and generates a system interrupt when it reached zero. The accompanying table lists the 16 system exceptions types and a variety of peripheral interrupts.

Table 24. Exception Types

Interrupt Number	Exception Number	Exception type	Priority	Vector Address	Description
—	0	—	—	0x000	Initial Stack Point value
—	1	Reset	-3 (Highest)	0x004	Reset
-14	2	NMI	-2	0x008	Non-Maskable Interrupt. The clock stuck interrupt signal (clock monitor function provided by Clock Control Unit) is connected to the NMI input
-13	3	Hard Fault	-1	0x00C	All fault classes
—	4-10	Reserved	—	—	—
-5	11	SVCall	Configurable(1)	0x02C	SVC instruction System service call
—	12-13	Reserved	—	—	—
-2	14	PendSV	Configurable(1)	0x038	System Service Pendable request
-1	15	SysTick	Configurable(1)	0x03C	SysTick timer decremented to zero
0	16	LVD	Configurable(2)	0x040	Low voltage detection interrupt
1	17	Reserved	—	0x044	—
2	18	FMC	Configurable(2)	0x048	FMC global interrupt
3	19	WKUP	Configurable(2)	0x04C	EXTI event wakeup or external WAKEUP pin interrupt
4	20	EXTI0 ~ 1	Configurable(2)	0x050	EXTI Line 0 & 1 interrupt
5	21	EXTI2 ~ 3	Configurable(2)	0x054	EXTI Line 2 & 3 interrupt
6	22	EXTI4 ~ 15	Configurable(2)	0x058	EXTI Line 4 ~ 15 interrupt
7	23	Reserved	—	0x05C	—
8	24	ADC	Configurable(2)	0x060	ADC global interrupt
9	25	Reserved	—	0x064	—
10	26	Reserved	—	0x068	—
11	27	Reserved	—	0x06C	—
12	28	GPTM	Configurable(2)	0x070	GPTM global interrupt
13	29	SCTM0	Configurable(2)	0x074	SCTM0 global interrupt
14	30	SCTM1	Configurable(2)	0x078	SCTM1 global interrupt

Interrupt Number	Exception Number	Exception type	Priority	Vector Address	Description
15	31	Reserved	—	0x07C	—
16	32	Reserved	—	0x080	—
17	33	BFTM	Configurable(2)	0x084	BFTM global interrupt
18	34	Reserved	—	0x088	—
19	35	I^2C	Configurable(2)	0x08C	I2C global interrupt
20	36	Reserved	—	0x090	—
21	37	SPI	Configurable(2)	0x094	SPI global interrupt
22	38	Reserved	—	0x098	—
23	39	USART	Configurable(2)	0x09C	USART global interrupt
24	40	Reserved	—	0x0A0	—
25	41	UART	Configurable(2)	0x0A4	UART global interrupt
26	42	Reserved	—	0x0A8	—
27	43	Reserved	—	0x0AC	—
28	44	Reserved	—	0x0B0	—
29	45	Reserved	—	0x0B4	—
30	46	Reserved	—	0x0B8	—
31	47	Reserved	—	0x0BC	—

Notes: 1. The exception priority can be changed using the NVIC System Handler Priority Registers. For more information, refer to the Arm® "Cortex®-M0+ Devices Generic User Guide" document.

2. The interrupt priority can be changed using the NVIC Interrupt Priority Registers. For more information, refer to the Arm® "Cortex®-M0+ Devices Generic User Guide" document.

Features

- 7 system Cortex®-M0+ exceptions
- Up to 32 Maskable peripheral interrupts
- 16 programmable priority levels (4 bits for interrupt priority setting)
- Non-Maskable interrupt
- Low-latency exception and interrupt handling
- Vector table remapping capability
  - Integrated simple, 24-bit system timer, SYSTICK
  - 24-bit down counter
  - Auto-reloading capability
  - Maskable system interrupt generation when counter decrements to 0
  - SysTick clock source derived from the HCLK clock divided by 8

Function Descriptions

SysTick Calibration

The SysTick Calibration Value Register (SCALIB) is provided by the NVIC to give a reference time base of 1ms for the RTOS tick timer or other purpose. The TENMS field in the SCALIB register has a fixed value of 5000 which is the counter reload value to indicate 1 ms when the clock source comes from the SysTick reference input clock STCLK with a frequency of 5 MHz (40 MHz divide by 8).

Register Map

The following table shows the NVIC registers and reset values.

Table 25. NVIC Register Map

Register	Offset	Description	Reset Value
NVIC Base Address = 0xE000_E000			
SYST_CSR	0x010	SysTick Control and Status Register	0x0000_0000
SYST_RVR	0x014	SysTick Reload Value Register	Unpredictable
SYST_CVR	0x018	SysTick Current Value Register	Unpredictable
SYST_CALIB	0x01C	SysTick Calibration Value Register	0x4000_1388
NVIC_ISER	0x100	Interrupt Set Enable Register	0x0000_0000
NVIC_ICER	0x180	Interrupt Clear Enable Register	0x0000_0000
NVIC_ISPR	0x200	Interrupt Set Pending Register	0x0000_0000
NVIC_ICPR	0x280	Interrupt Clear Pending Register	0x0000_0000
NVIC_IPR0	0x400	Interrupt 0 ~ 3 Priority Register	0x0000_0000
NVIC_IPR1	0x404	Interrupt 4 ~ 7 Priority Register	0x0000_0000
NVIC_IPR2	0x408	Interrupt 8 ~ 11 Priority Register	0x0000_0000
NVIC_IPR3	0x40C	Interrupt 12 ~ 15 Priority Register	0x0000_0000
NVIC_IPR4	0x410	Interrupt 16 ~ 19 Priority Register	0x0000_0000
NVIC_IPR5	0x414	Interrupt 20 ~ 23 Priority Register	0x0000_0000
NVIC_IPR6	0x418	Interrupt 24 ~ 27 Priority Register	0x0000_0000
NVIC_IPR7	0x41C	Interrupt 28 ~ 31 Priority Register	0x0000_0000
CPUID	0xD00	CPUID register	0x410C_C601
ICSR	0xD04	Interrupt Control and State Register	0x0000_0000
VTOR	0xD08	Vector Table Offset Register	0x0000_0000
AIRCR	0xD0C	Application Interrupt and Reset Control Register	0xFA05_0000
SCR	0xD10	System Control Register	0x0000_0000
CCR	0xD14	Configuration and Control Register	0x0000_0204
SHPR2	0xD1C	System Handlers Priority Register 2	0x0000_0000
SHPR3	0xD20	System Handlers Priority Register 3	0x0000_0000

Note: For more information of the above detail register descriptions, please refer to the "Cortex®-M0+ Devices Generic User Guide" document from Arm®.

11 External Interrupt/Event Controller (EXTI)

Introduction

The External Interrupt/Event Controller, EXTI, comprises 16 edge detectors which can generate a wake-up event or interrupt requests independently. In interrupt mode there are five trigger types which can be selected as the external interrupt trigger type, low level, high level, negative edge, positive edge and both edges, selectable using the SRCnTYPE field in the EXTICFGRn (n = 0 ~ 15) register. In the wake-up event mode, the wake-up event polarity can be configured by setting the EXTInWPOL (n = 0 ~ 15) field in the EXTIWAKUPPOLR register. If the EVWUPIEN bit in the EXTIWAKUPCR Register is set, the EVWUP interrupt can be generated when the associated wake-up event occurs and the corresponding EXTI wake-up enable bit is set. Each EXTI line can also be masked independently.

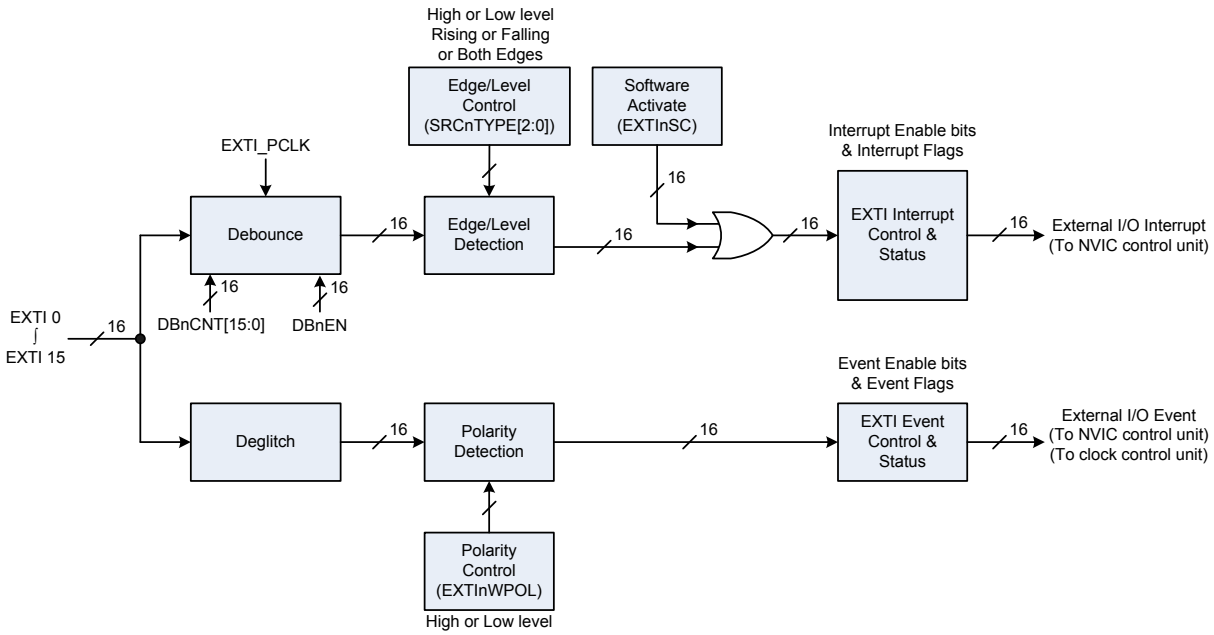


Figure 22. EXTI Block Diagram

Features

- Up to 16 EXTI lines with configurable trigger source and type
  - All GPIO pins can be selected as EXTI trigger source
  - Source trigger type includes high level, low level, negative edge, positive edge, or both edge
- Individual interrupt enable, wakeup enable and status bits for each EXTI line
- Software interrupt trigger mode for each EXTI line
- Integrated deglitch filter for short pulse blocking

Function Descriptions

Wakeup Event Management

In order to wakeup the system from the power saving mode, the EXTI controller provides a function which can monitor external events and send them to the CPU core and the Clock Control Unit, CKCU. These external events include EXTI events, Low Voltage Detection, WAKEUP input pin. By configuring the wakeup event enable bit in the corresponding peripheral, the wakeup signal will be sent to the CPU and the CKCU via the EXTI controller when the corresponding wakeup event occurs. Additionally, the software can enable the event wakeup interrupt function by setting the EVWUPIEN bit in the EXTIWAKUPCR register and the EXTI controller will then assert an interrupt when the wakeup event occurs.

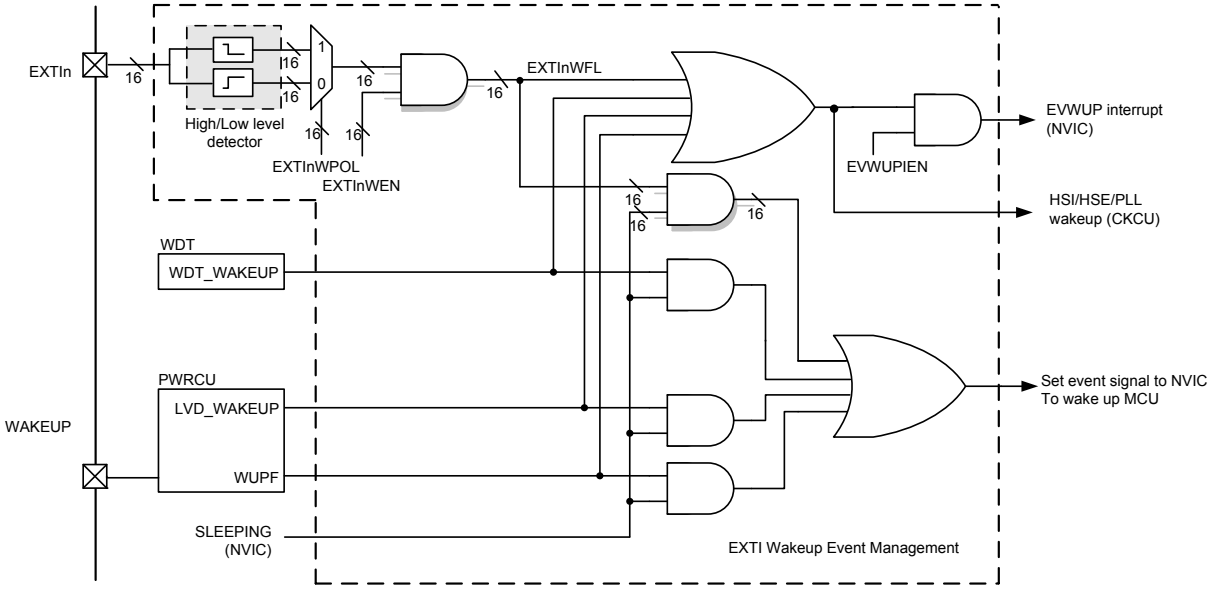


Figure 23. EXTI Wake-up Event Management

External Interrupt/Event Line Mapping

All GPIO pins can be selected as EXTI trigger sources by configuring the EXTInPIN [3:0] field in the AFIO ESSRn (n = 0 ~ 1) register to trigger an interrupt or event. Refer to the AFIO section for more details.

Interrupt and Debounce

The application software can set the DBnEN bit in the EXTIn Interrupt Configuration Register EXTICFGRn (n = 0 ~ 15) to enable the corresponding pin de-bounce function and configure the DBnCNT field in the EXTICFGRn so as to select an appropriate de-bounce time for specific applications. The interrupt signal will however be delayed due to the de-bounce function. When the device is woken up from the power saving mode by an external interrupt, an interrupt request will be generated by the EXTI wakeup flag. After the device has been woken up and the clock has recovered, the EXTI wake-up flag that was triggered by the EXTI line must be read and then cleared by application software. The accompanying diagram shows the relationship between the EXTI input signal and the EXTI interrupt/event request signal.

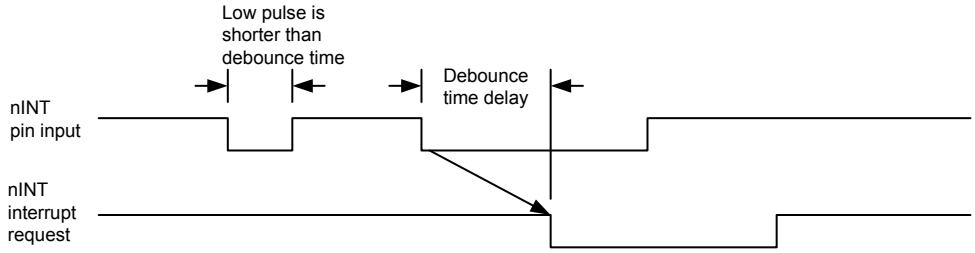


Figure 24. EXTI Interrupt Debounce Function

Register Map

The following table shows the EXTI registers and reset values.

Table 26. EXTI Register Map

Register	Offset	Description	Reset Value
EXTICFGR0	0x000	EXTI Interrupt 0 Configuration Register	0x0000_0000
EXTICFGR1	0x004	EXTI Interrupt 1 Configuration Register	0x0000_0000
EXTICFGR2	0x008	EXTI Interrupt 2 Configuration Register	0x0000_0000
EXTICFGR3	0x00C	EXTI Interrupt 3 Configuration Register	0x0000_0000
EXTICFGR4	0x010	EXTI Interrupt 4 Configuration Register	0x0000_0000
EXTICFGR5	0x014	EXTI Interrupt 5 Configuration Register	0x0000_0000
EXTICFGR6	0x018	EXTI Interrupt 6 Configuration Register	0x0000_0000
EXTICFGR7	0x01C	EXTI Interrupt 7 Configuration Register	0x0000_0000
EXTICFGR8	0x020	EXTI Interrupt 8 Configuration Register	0x0000_0000
EXTICFGR9	0x024	EXTI Interrupt 9 Configuration Register	0x0000_0000
EXTICFGR10	0x028	EXTI Interrupt 10 Configuration Register	0x0000_0000
EXTICFGR11	0x02C	EXTI Interrupt 11 Configuration Register	0x0000_0000
EXTICFGR12	0x030	EXTI Interrupt 12 Configuration Register	0x0000_0000
EXTICFGR13	0x034	EXTI Interrupt 13 Configuration Register	0x0000_0000
EXTICFGR14	0x038	EXTI Interrupt 14 Configuration Register	0x0000_0000
EXTICFGR15	0x03C	EXTI Interrupt 15 Configuration Register	0x0000_0000
EXTICR	0x040	EXTI Interrupt Control Register	0x0000_0000
EXTIEDGEFLGR	0x044	EXTI Interrupt Edge Flag Register	0x0000_0000
EXTIEDGESR	0x048	EXTI Interrupt Edge Status Register	0x0000_0000
EXTISSCR	0x04C	EXTI Interrupt Software Set Command Register	0x0000_0000
EXTIWAKUPCR	0x050	EXTI Interrupt Wakeup Control Register	0x0000_0000
EXTIWAKUPPOLR	0x054	EXTI Interrupt Wakeup Polarity Register	0x0000_0000
EXTIWAKUPFLG	0x058	EXTI Interrupt Wakeup Flag Register	0x0000_0000

Register Descriptions

EXTI Interrupt Configuration Register n – EXTICFGRn, n = 0 ~ 15

This register is used to specify the debounce function and select the trigger type.

Offset: 0x000 (0) ~ 0x03C (15)

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	DBnEN	SRCnTYPE			Reserved			
Type/Reset	RW 0	RW 0	RW 0	RW 0				
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	DBnCNT							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	DBnCNT							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[31]	DBnEN	EXTIn De-bounce Circuit Enable Bit (n = 0 ~ 15) 0: De-bounce circuit is disabled 1: De-bounce circuit is enabled
[30:28]	SRCnTYPE	EXTIn Interrupt Source Trigger Type (n = 0 ~ 15)
[15:0]	DBnCNT	EXTIn De-bounce Counter (n = 0 ~ 15) The de-bounce time is calculated with DBnCNT x APB clock (EXTI_PCLK) period and should be long enough to take effect on the input signal.

SRCnTYPE [2:0]			Interrupt Source Type
0	0	0	Low-level Sensitive
0	0	1	High-level Sensitive
0	1	0	Negative-edge Triggered
0	1	1	Positive-edge Triggered
1	X	X	Both-edge Triggered

EXTI Interrupt Control Register – EXTICR

This register is used to control the EXTI interrupt.

Offset: 0x040

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	EXTI15EN	EXTI14EN	EXTI13EN	EXTI12EN	EXTI11EN	EXTI10EN	EXTI9EN	EXTI8EN
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	EXTI7EN	EXTI6EN	EXTI5EN	EXTI4EN	EXTI3EN	EXTI2EN	EXTI1EN	EXTI0EN
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	EXTInEN	EXTIn Interrupt Enable Bit (n = 0 ~ 15) 0: EXTI line n interrupt is disabled 1: EXTI line n interrupt is enabled

EXTI Interrupt Edge Flag Register – EXTIEDGEFLGR

This register is used to indicate if an EXTI edge has been detected.

Offset: 0x044

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	Reserved							
Type/Reset								
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	EXTI15EDF	EXTI14EDF	EXTI13EDF	EXTI12EDF	EXTI11EDF	EXTI10EDF	EXTI9EDF	EXTI8EDF
Type/Reset	WC 0	WC 0	WC 0	WC 0	WC 0	WC 0	WC 0	WC 0
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	EXTI7EDF	EXTI6EDF	EXTI5EDF	EXTI4EDF	EXTI3EDF	EXTI2EDF	EXTI1EDF	EXTI0EDF
Type/Reset	WC 0	WC 0	WC 0	WC 0	WC 0	WC 0	WC 0	WC 0

Bits	Field	Descriptions
[15:0]	EXTInEDF	EXTIn Both Edge Detection Flag (n = 0 ~ 15) 0: No edge is detected 1: Positive or negative edge is detected This bit is set by the hardware circuitry when a positive or negative edge is detected on the corresponding EXTI line. Software should write 1 to clear it.

EXTI Interrupt Edge Status Register – EXTIEDGESR

This register indicates the polarity of a detected EXTI edge.

Offset: 0x048

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	EXTI15EDS	EXTI14EDS	EXTI13EDS	EXTI12EDS	EXTI11EDS	EXTI10EDS	EXTI9EDS	EXTI8EDS
Type/Reset	WC 0	WC 0	WC 0	WC 0	WC 0	WC 0	WC 0	WC 0
	7	6	5	4	3	2	1	0
	EXTI7EDS	EXTI6EDS	EXTI5EDS	EXTI4EDS	EXTI3EDS	EXTI2EDS	EXTI1EDS	EXTI0EDS
Type/Reset	WC 0	WC 0	WC 0	WC 0	WC 0	WC 0	WC 0	WC 0

Bits	Field	Descriptions
[15:0]	EXTInEDS	EXTIn Both Edge Detection Status (n = 0 ~ 15) 0: Negative edge is detected 1: Positive edge is detected Software should write 1 to clear it.

EXTI Interrupt Software Set Command Register – EXTISSCR

This register is used to activate the EXTI interrupt.

Offset: 0x04C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	EXTI15SC	EXTI14SC	EXTI13SC	EXTI12SC	EXTI11SC	EXTI10SC	EXTI9SC	EXTI8SC
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	EXTI7SC	EXTI6SC	EXTI5SC	EXTI4SC	EXTI3SC	EXTI2SC	EXTI1SC	EXTI0SC
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	EXTInSC	EXTIn Software Set Command (n = 0 ~ 15) 0: Deactivates the corresponding EXTI interrupt 1: Activates the corresponding EXTI interrupt

EXTI Interrupt Wakeup Control Register – EXTIWAKUPCR

This register is used to control the EXTI interrupt and wakeup function.

Offset: 0x050

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	EVWUPIEN	Reserved						
Type/Reset	RW 0							
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	EXTI15WEN	EXTI14WEN	EXTI13WEN	EXTI12WEN	EXTI11WEN	EXTI10WEN	EXTI9WEN	EXTI8WEN
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	EXTI7WEN	EXTI6WEN	EXTI5WEN	EXTI4WEN	EXTI3WEN	EXTI2WEN	EXTI1WEN	EXTI0WEN
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[31]	EVWUPIEN	EXTI Event Wakeup Interrupt Enable Bit 0: Disable EVWUP interrupt 1: Enable EVWUP interrupt
[15:0]	EXTInWEN	EXTIn Wakeup Enable Bit (n = 0 ~ 15) 0: Power saving mode wakeup is disabled 1: Power saving mode wakeup is enabled

EXTI Interrupt Wakeup Polarity Register – EXTIWAKUPPOLR

This register is used to select the EXTI line interrupt wakeup polarity.

Offset: 0x054

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	EXTI15WPOL	EXTI14WPOL	EXTI13WPOL	EXTI12WPOL	EXTI11WPOL	EXTI10WPOL	EXTI9WPOL	EXTI8WPOL
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	EXTI7WPOL	EXTI6WPOL	EXTI5WPOL	EXTI4WPOL	EXTI3WPOL	EXTI2WPOL	EXTI1WPOL	EXTI0WPOL
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	EXTInWPOL	EXTIn Wakeup Polarity (n = 0 ~ 15) 0: EXTIn wakeup is high level active 1: EXTIn wakeup is low level active

EXTI Interrupt Wakeup Flag Register – EXTIWAKUPFLG

This register is the EXTI interrupt wake flag register.

Offset: 0x058

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								

	15	14	13	12	11	10	9	8
	EXTI15WFL	EXTI14WFL	EXTI13WFL	EXTI12WFL	EXTI11WFL	EXTI10WFL	EXTI9WFL	EXIT8WFL
Type/Reset	WC 0	WC 0	WC 0	WC 0	WC 0	WC 0	WC 0	WC 0

	7	6	5	4	3	2	1	0
	EXTI7WFL	EXTI6WFL	EXTI5WFL	EXTI4WFL	EXTI3WFL	EXTI2WFL	EXTI1WFL	EXTI0WFL
Type/Reset	WC 0	WC 0	WC 0	WC 0	WC 0	WC 0	WC 0	WC 0

Bits	Field	Descriptions
[15:0]	EXTInWFL	EXTIn Wakeup Flag (n = 0 ~ 15) 0: No wakeup occurs 1: System is waken up by EXTIn Software should write 1 to clear it.

12 Analog to Digital Converter (ADC)

Introduction

A 12-bit multi-channel Analog to Digital Converter is integrated in the device. There are a total of 10 multiplexed channels including 8 external channels on which the external analog signal can be supplied and 2 internal channels. If the input voltage is required to remain within a specific threshold window, the Analog Watchdog function will monitor and detect the signal. An interrupt will then be generated to inform that the input voltage is higher or lower than the set thresholds. There are three conversion modes to convert an analog signal to digital data. The A/D conversion can be operated in one shot, continuous and discontinuous conversion mode. A 16-bit data register is provided to store the data after conversion.

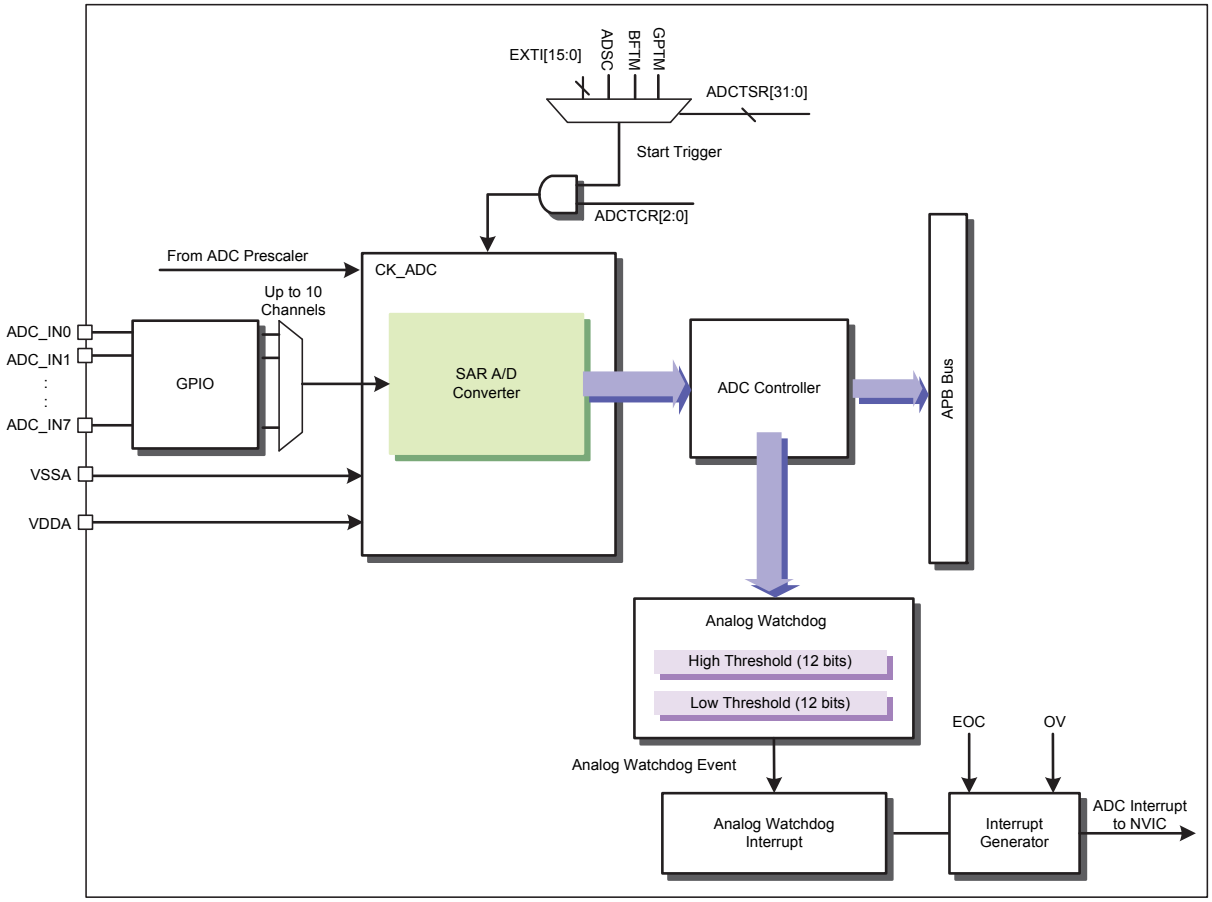


Figure 25. ADC Block Diagram

Features

- 12-bit SAR ADC engine
- Up to 1 MSPS conversion rate
- 8 external analog input channels
- 2 internal analog input channels for reference voltage detection
- Programmable sampling time for conversion channel
- Up to 8 programmable conversion channel sequence and dedicated data registers for conversion result
- Three conversion mode
  - One shot conversion mode
  - Continuous conversion mode
  - Discontinuous conversion mode.
- Analog watchdog for predefined voltage range monitor
  - Lower/upper threshold register
  - Interrupt generation
- Various trigger start source for conversion modes
  - Software trigger
  - EXTI – external interrupt input pin
  - GPTM trigger
  - BFTM trigger
- Multiple generated interrupts
  - End of single conversion
  - End of subgroup conversion
  - End of cycle conversion
  - Analog Watchdog
  - Data register overwriting

Function Descriptions

ADC Clock Setup

The ADC clock, CK_ADC, is provided by the Clock Controller, which is synchronous and divided by with the AHB clock known as HCLK. Refer to the Clock Control Unit chapter for more details. Notes that the ADC requires at least two ADC clock cycles to switch between power-on and power-off conditions (ADEN bit = '0').

Channel Selection

The A/D converter supports 10 multiplexed channels and arranges the conversion results into a specific group. A conversion group can organize a sequence which can be implemented on the channels arranged in a specific conversion sequence length from 1 to 8. For example, conversion can be carried out with the following channel sequence: CH2, CH4, CH7, CH5, CH6, CH3, CH1 and CH0 one after another.

A group is composed of up to 8 conversions. The selected channels of the group conversion can be specified in the ADCLST0~ADCLST1 registers. The total conversion sequence length is setup using the ADSEQL[2:0] bits in the ADCCONV register.

Modifying the ADCCR register during a conversion process will reset the current conversion, after which a new start pulse is required to restart a new conversion.

Conversion Mode

The A/D converter has three operating conversion modes. The conversion modes are One Shot Conversion Mode, Continuous Conversion Mode, and Discontinuous Conversion mode. Details are provided later.

One Shot Conversion Mode

In the One Shot Conversion mode, the ADC will perform conversion cycles on the channels specified in the A/D conversion list registers ADCLSTn with a specific sequence when an A/D converter trigger event occurs. When the A/D conversion mode field ADMODE [1:0] in the ADCCR register is set to 0x0, the A/D converter will operate in the One Shot Conversion Mode. This mode can be started by a software trigger, an external EXTI event or a TM event determined by the Trigger Control Register ADCTCR and the Trigger Source Register ADCTSR.

After Conversion:

- The converted data will be stored in the 16-bit ADCDRy (y = 0~7) registers.
- The ADC single sample end of conversion event raw status flag, ADIRAWS, in the ADCIRAW register will be set when the single sample conversion is finished.
- An interrupt will be generated after a single sample end of conversion if the ADIES bit in the ADCIER register is enabled.
- An interrupt will be generated after a group cycle end of conversion if the ADIEC bit in the ADCIER register is enabled.

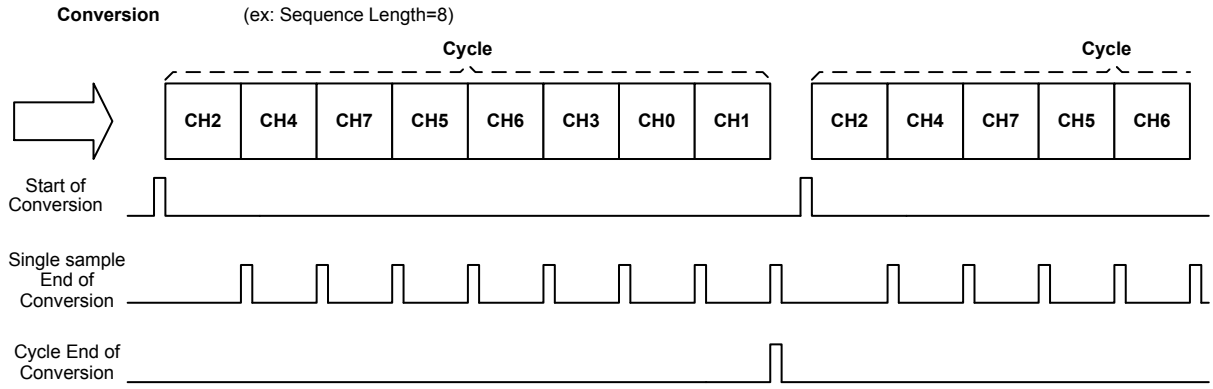


Figure 26. One Shot Conversion Mode

Continuous Conversion Mode

In the Continuous Conversion Mode, repeated conversion cycle will start automatically without requiring additional A/D start trigger signals after a channels group conversion has completed. When the A/D conversion mode field ADMODE[1:0] is set to 0x2, the A/D converter will operate in the Continuous Conversion Mode which can be started by a software trigger, an external EXTI event or a TM event determined by the Trigger Control Register ADCTCR and the Trigger Source Register ADCTSR.

After conversion:

- The converted data will be stored in the 16-bit ADCDRy (y = 0~7) registers.
- The ADC group cycle end of conversion event raw status flag, ADIRAWC, in the ADCIRAW register will be set when the conversion cycle is finished.
- An interrupt will be generated after a group cycle end of conversion if the ADIEC bit in the ADCIER register is enabled.

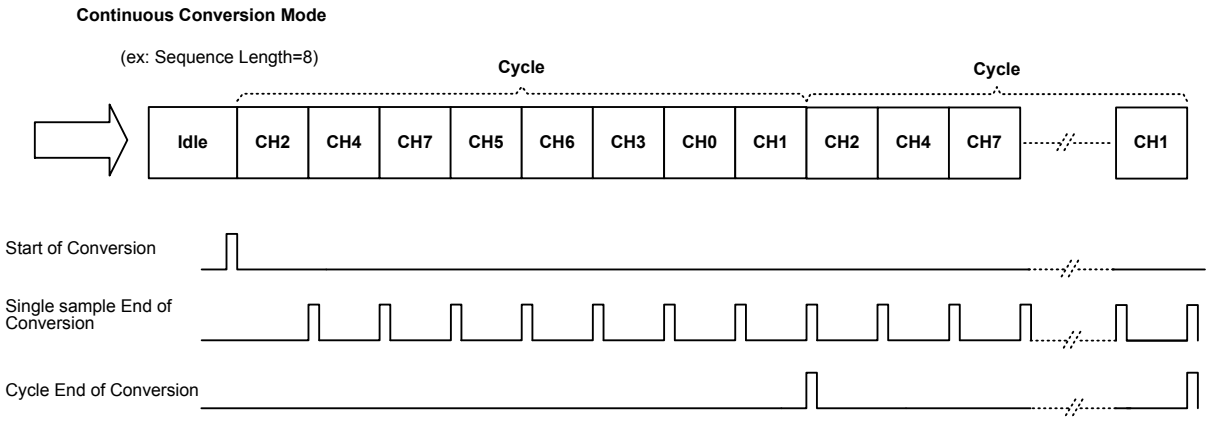


Figure 27. Continuous Conversion Mode

Discontinuous Conversion Mode

The A/D converter will operate in the Discontinuous Conversion Mode for channels group when the A/D conversion mode bit field ADMODE [1:0] in the ADCCONV register is set to 0x3. The group to be converted can have up to 8 channels and can be arranged in a specific sequence by configuring the ADCLSTn registers where n ranges from 0 to 1. This mode is provided to convert data for the group with a short sequence, named as the A/D conversion subgroup, each time a trigger event occurs. The subgroup length is defined by the ADSUBL [2:0] field in the ADCCONV register to specify the subgroup length. In the Discontinuous Conversion Mode the A/D converter can be started by a software trigger, an external EXTI event or a TM event for the groups determined by the Trigger Control Register ADCTCR and the Trigger Source Register ADCTSR.

In the Discontinuous Conversion Mode, the A/D Converter will start to convert the next n conversions where the number n is the subgroup length defined by the ADSUBL field. When a trigger event occurs, the channels to be converted with a specific sequence are specified in the ADCLSTn registers. After n conversions have completed, the subgroup EOC interrupt raw flag ADIRAWG in the ADCIRAW register will be asserted. The A/D converter will now not continue to perform the next n conversions until the next trigger event occurs. The conversion cycle will end after all the group channels, of which the total number is defined by the ADSEQL[2:0] bits in the ADCCONV register, have finished their conversion, at which point the cycle EOC interrupt raw flag ADIRAWC in the ADCIRAW register will be asserted. If a new trigger event occurs after all the subgroup channels have all been converted, i.e., a complete conversion cycle has been finished, the conversion will restart from the first subgroup.

Example:

A/D subgroup length = 3 (ADSUBL=2) and sequence length = 8 (ADSEQL=7), channels to be converted = 2, 4, 7, 5, 6, 3, 0 and 1 – specific converting sequence as defined in the ADCLSTn registers,

- Trigger 1: subgroup channels to be converted are CH2, CH4 and CH7 with the ADIRAWG flag being asserted after subgroup EOC.
- Trigger 2: subgroup channels to be converted are CH5, CH6 and CH3 with the ADIRAWG flag being asserted after subgroup EOC.
- Trigger 3: subgroup channels to be converted are CH0 and CH1 with the ADIRAWG flag being asserted after subgroup EOC. Also a Cycle end of conversion (EOC) interrupt raw flag ADIRAWC will be asserted.
- Trigger 4: subgroup channels to be converted are CH2, CH4 and CH7 with the ADIRAWG flag being asserted – conversion sequence restarts from the beginning.

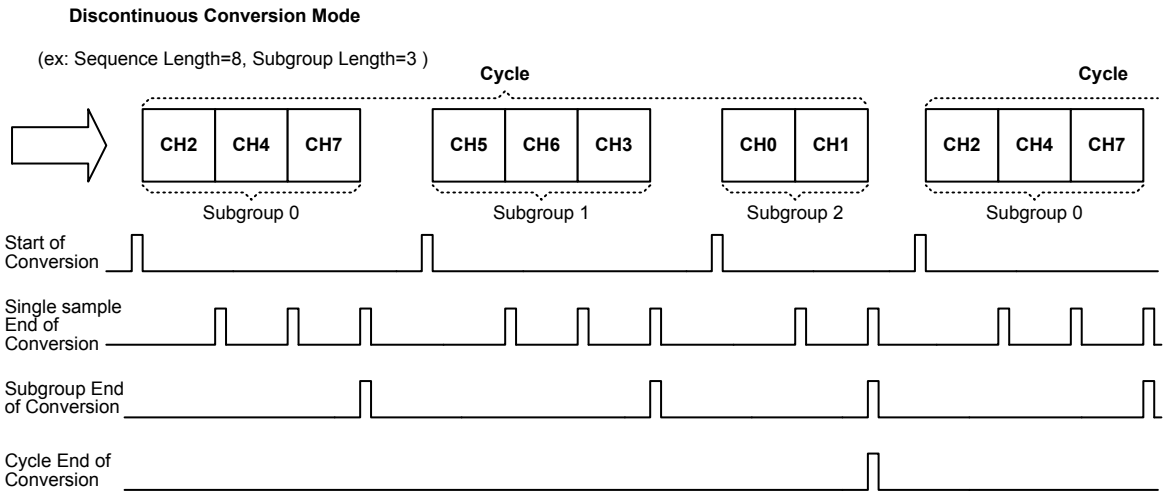


Figure 28. Discontinuous Conversion Mode

Start Conversion on External Event

An A/D converter conversion can be initiated by a software trigger, a General-Purpose Timer Module (GPTM) event, a Basic Function Timer Module (BFTM) event or an external trigger. Each trigger source can be enabled by setting the corresponding enable control bit in the ADCTCR register and then selected by configuring the associated selection bits in the ADCTSR register to start a group channel conversion.

An A/D converter conversion can be started by setting the software trigger bit, ADSC, in the ADCTSR register for the group channel when the software trigger enable bit, ADSW, in the ADCTCR register is set to 1. After the A/D converter starts converting the analog data, the corresponding enable bit ADSC will be cleared to 0 automatically.

The A/D converter can also be triggered to start a group conversion by a TM event. The TM events include a GPTM master trigger output MTO, four GPTM channel outputs CH0~CH3 and a BFTM trigger output. If the corresponding Timer trigger enable bit is set to 1 and the trigger output or the TM channel event is selected via the relevant TM event selection bits, the A/D converter will start a conversion when a rising edge of the selected trigger event occurs.

In addition to the internal trigger sources, the A/D converter can be triggered to start a conversion by an external trigger event. The external trigger event is derived from the external lines, EXTIn. If the external trigger enable bit ADEXTI is set to 1 and the corresponding EXTI line is selected by configuring the ADEXTIS field in the ADCTSR register, the A/D converter will start a conversion when an EXTI line active edge determined in the EXIT Unit occurs.

Sampling Time Setting

The conversion channel sampling time can be programmed according to the input resistance of the input voltage source. This sampling time must be enough for the input voltage source to charge the internal sample and hold capacitor in the A/D converter to the input voltage level. Each conversion channel is sampled with the same sampling time. By modifying the ADST[7:0] bits in the ADCSTR register, the sampling time of the analog input signal can be determined.

The total conversion time (T_{conv}) is calculated using the following formula:

$$T_{conv} = T_{Sampling} + T_{Latency}$$

Where the minimum sampling time $T_{Sampling}$ = 1.5 cycles (when ADST[7:0] = 0) and the minimum channel conversion latency $T_{Latency}$ = 12.5 cycles.

Example:

With the A/D Converter clock CK_ADC = 14 MHz and a sampling time =1.5 cycles:

$$T_{conv} = 1.5 + 12.5 = 14 \text{ cycles} = 1\ \mu s$$

Data Format

The ADC conversion result can be read in the ADCDRy register and the data format is shown in the following Table 27.

Table 27. Data format in ADCDR [15:0]

Description	ADCDR register Data Format
Right aligned	"0_0_0_0_d11_d10_d9_d8_d7_d6_d5_d4_d3_d2_d1_d0"

Analog Watchdog

The A/D converter includes a watchdog function to monitor the converted data. There are two kinds of thresholds for the watchdog monitor function, known as the watchdog upper threshold and watchdog lower threshold, which are specified in the Watchdog Upper and Lower Threshold Registers respectively. The watchdog monitor function is enabled by setting the watchdog upper and lower threshold monitor function enable bits, ADWUE and ADWLE, in the watchdog control register ADCWCR. The channel to be monitored can be specified by configuring the ADWCH and ADWALL bits. When the converted data is less or higher than the lower or upper threshold, as defined in the ADCLTR or ADCUTR registers respectively, the watchdog lower or upper threshold interrupt raw flags, ADIRAWL or ADIRAWU in the ADCIRAW register, will be asserted if the watchdog lower or upper threshold monitor function is enabled. If the lower or upper threshold interrupt raw flag is asserted and the corresponding interrupt is enabled by setting the ADIML or ADIMU bit in the ADCIME register, the A/D watchdog lower or upper threshold interrupt will be generated.

Interrupts

When an A/D conversion is completed, an End of Conversion EOC event will occur. There are three kinds of EOC events which are known as single sample EOC, subgroup EOC and cycle EOC for A/D conversion. A single sample EOC event will occur and the single sample EOC interrupt raw flag, ADIRAWS bits in the ADCIRAW register, will be asserted when a single channel conversion has completed. A subgroup EOC event will occur and the subgroup EOC interrupt raw flag, ADIRAWG in the ADCIRAW register, will be asserted when a subgroup conversion has completed. A cycle EOC event will occur and the cycle EOC interrupt raw flag, ADIRAWC bits in the ADCIRAW register, will be asserted when a cycle conversion is finished. When a single sample EOC, a subgroup EOC or a cycle EOC raw flag is asserted and the corresponding interrupt enable bit, ADIMC, ADIEG or ADIES bit in the ADCIER register, is set to 1, the associated interrupt will be generated.

After a conversion has completed, the 12-bit digital data will be stored in the associated ADCDRy registers and the value of the data valid flag named as ADVLDy will be changed from low to high. The converted data should be read by the application program, after which the data valid flag ADVLDy will be automatically changed from high to low. Otherwise, a data overwrite event will occur and the data overwrite interrupt raw flag ADIRAWO bit in the ADCIRAW register will be asserted. When the related data overwrite raw flag is asserted, the data overwrite interrupt will be generated if the interrupt enable bit ADIEO in the ADCIER register is set to 1.

If the A/D watchdog monitor function is enabled and the data after a channel conversion is less than the lower threshold or higher than the upper threshold, the watchdog lower or upper threshold interrupt raw flag ADIRAWL or ADIRAWU in the ADCIRAW register will be asserted. When the ADIRAWL or ADIRAWU flag is asserted and the corresponding interrupt enable bit, ADIEL or ADIEU in the ADCIER register, is set a watchdog lower or upper threshold interrupt will be generated.

The A/D Converter interrupt clear bits are used to clear the associated A/D converter interrupt raw and interrupt status bits. Writing a 1 into the specific A/D converter interrupt clear bit in the A/D converter interrupt clear register ADCICLR will clear the corresponding A/D converter interrupt raw and interrupt status bits. These bits are automatically cleared to 0 by hardware after being set to 1.

Register Map

The following table shows the A/D Converter registers and reset values.

Table 28. A/D Converter Register Map

Register	Offset	Description	Reset Value
ADCCR	0x000	ADC Conversion Control Register	0x0000_0000
ADCLST0	0x004	ADC Conversion List Register 0	0x0000_0000
ADCLST1	0x008	ADC Conversion List Register 1	0x0000_0000
ADCSTR	0x020	ADC Input Sampling Time Register	0x0000_0000
ADCDR0	0x030	ADC Conversion Data Register 0	0x0000_0000
ADCDR1	0x034	ADC Conversion Data Register 1	0x0000_0000
ADCDR2	0x038	ADC Conversion Data Register 2	0x0000_0000
ADCDR3	0x03C	ADC Conversion Data Register 3	0x0000_0000
ADCDR4	0x040	ADC Conversion Data Register 4	0x0000_0000
ADCDR5	0x044	ADC Conversion Data Register 5	0x0000_0000
ADCDR6	0x048	ADC Conversion Data Register 6	0x0000_0000
ADCDR7	0x04C	ADC Conversion Data Register 7	0x0000_0000
ADCTCR	0x070	ADC Trigger Control Register	0x0000_0000
ADCTSR	0x074	ADC Trigger Source Register	0x0000_0000
ADCWCR	0x078	ADC Watchdog Control Register	0x0000_0000
ADCTR	0x07C	ADC Watchdog Threshold Register	0x0000_0000
ADCIER	0x080	ADC Interrupt Enable register	0x0000_0000
ADCIRAW	0x084	ADC Interrupt Raw Status Register	0x0000_0000
ADCISR	0x088	ADC Interrupt Status Register	0x0000_0000
ADCICLR	0x08C	ADC Interrupt Clear Register	0x0000_0000

Register Descriptions

ADC Conversion Control Register – ADCCR

This register specifies the mode setting, sequence length, and subgroup length of the ADC conversion mode. Note that once the content of ADCCR is changed, the conversion in progress will be aborted and the A/D converter will return to idle state. The application program has to wait for at least one CK_ADC clock before issuing the next command.

Offset: 0x000

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved					ADSUBL		
Type/Reset						RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
	Reserved					ADSEQL		
Type/Reset						RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	ADCEN	ADCRST	Reserved					ADMODE
Type/Reset	RW 0	RW 0					RW 0	RW 0

Bits	Field	Descriptions
[18:16]	ADSUBL	ADC Conversion Subgroup Length The ADSUBL field specifies the conversion channel length of each subgroup in the Discontinuous Conversion Mode. The subgroup length = ADSUBL [2:0] + 1. If the sequence length (ADSEQL [2:0] + 1) is not a multiple of the subgroup length (ADSUBL [2:0] + 1), the last subgroup will be the rest of the group channels that have not been converted.
[10:8]	ADSEQL	ADC Conversion Length 0x00: The channel specified by the ADSEQ0 field in the ADCLST0 register will be converted. Others: Sequence length = ADSEQL [2:0] + 1.
[7]	ADCEN	ADC Enable 0: ADC disable 1: ADC enable When this bit is cleared to 0, the A/D converter will be disabled and the CK_ADC clock will also be switched off.
[6]	ADCRST	ADC Reset 0: No effect 1: Reset A/D converter except for the A/D Converter controller

Bits	Field	Descriptions
[1:0]	ADMODE	ADC Conversion Mode

ADMODE [1:0]	Mode	Descriptions
00	One shot mode	After a start trigger, the conversion will be executed on the specific channels for the whole conversion sequence once.
01	Reserved	
10	Continuous mode	After a start trigger, the conversion will be executed on the specific channels for the whole sequence continuously until the conversion mode is changed.
11	Discontinuous mode	After a start trigger, the conversion will be executed on the current subgroup. When the last subgroup is finished, the conversion will restart from the first subgroup if another start trigger occurs.

ADC Conversion List Register 0 – ADCLST0

This register specifies the conversion sequence order No.0 ~ No.3 of the ADC.

Offset: 0x004

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved			ADSEQ3				
Type/Reset				RW 0	RW 0	RW 0	RW 0	RW 0
	23	22	21	20	19	18	17	16
	Reserved			ADSEQ2				
Type/Reset				RW 0	RW 0	RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
	Reserved			ADSEQ1				
Type/Reset				RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	Reserved			ADSEQ0				
Type/Reset				RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[28:24]	ADSEQ3	ADC Conversion Sequence Select 3 Select the ADC input channel for the 3rd ADC conversion sequence. 0x0: ADC_IN0 0x1: ADC_IN1 0x2: ADC_IN2 0x3: ADC_IN3 0x4: ADC_IN4 0x5: ADC_IN5 0x6: ADC_IN6 0x7: ADC_IN7 0x8 ~ 0xF: Reserved 0x10: Analog ground, AVSS (V_{REF-}) 0x11: Analog power, AVDD (V_{REF+}) 0x12 ~ 0x1F: Invalid setting. These values must not be selected as it may cause the ADC abnormal operations.
[20:16]	ADSEQ2	ADC Conversion Sequence Select 2
[12:8]	ADSEQ1	ADC Conversion Sequence Select 1
[4:0]	ADSEQ0	ADC Conversion Sequence Select 0

ADC Conversion List Register 1 – ADCLST1

This register specifies the conversion sequence order No.4 ~ No.7 of the ADC.

Offset: 0x008

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved			ADSEQ7				
Type/Reset				RW 0	RW 0	RW 0	RW 0	RW 0
	23	22	21	20	19	18	17	16
	Reserved			ADSEQ6				
Type/Reset				RW 0	RW 0	RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
	Reserved			ADSEQ5				
Type/Reset				RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	Reserved			ADSEQ4				
Type/Reset				RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[28:24]	ADSEQ7	ADC Conversion Sequence Select 7 Select the ADC input channel for the 7th ADC conversion sequence. 0x0: ADC_IN0 0x1: ADC_IN1 0x2: ADC_IN2 0x3: ADC_IN3 0x4: ADC_IN4 0x5: ADC_IN5 0x6: ADC_IN6 0x7: ADC_IN7 0x8 ~ 0xF: Reserved 0x10: Analog ground, AVSS (V_{REF-}) 0x11: Analog power, AVDD (V_{REF+}) 0x12 ~ 0x1F: Invalid setting. These values must not be selected as it may cause the ADC abnormal operations.
[20:16]	ADSEQ6	ADC Conversion Sequence Select 6
[12:8]	ADSEQ5	ADC Conversion Sequence Select 5
[4:0]	ADSEQ4	ADC Conversion Sequence Select 4

ADC Input Sampling Time Register – ADCSTR

This register specifies the A/D conversion input channel sampling time.

Offset: 0x020

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	ADST							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[7:0]	ADST	ADC Input Channel Sampling Time Sampling time = (ADST[7:0] + 1.5) × CK_ADC clocks.

ADC Conversion Data Register y – ADCDRy, y = 0 ~ 7

This register is used to store the conversion data of the ADC conversion sequence order No.y which is specified by the ADSEQy field in the ADCLSTn (n=0~1) registers.

Offset: 0x030 ~ 0x04C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	ADVLDy	Reserved						
Type/Reset	RC	0						
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	ADDy							
Type/Reset	RO	0	RO	0	RO	0	RO	0	RO	0	RO	0	RO	0	RO	0
	7	6	5	4	3	2	1	0
	ADDy							
Type/Reset	RO	0	RO	0	RO	0	RO	0	RO	0	RO	0	RO	0	RO	0

Bits	Field	Descriptions
[31]	ADVLDy	ADC Conversion Data of Sequence Order No.y Valid Bit (y = 0 ~ 7) 0: Data invalid or have been read 1: New data valid
[15:0]	ADDy	ADC Conversion Data of Sequence Order No.y (y = 0 ~ 7) The conversion result of Sequence Order No.y in the ADCLSTn (n=0 ~1) registers.

ADC Trigger Control Register – ADCTCR

This register contains the ADC start conversion trigger enable bits.

Offset: 0x070

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved				BFTM	TM	ADEXTI	ADSW
Type/Reset					RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[3]	BFTM	ADC Conversion BFTM Event Trigger enable control 0: Disable conversion trigger by BFTM events 1: Enable conversion trigger by BFTM events
[2]	TM	ADC Conversion GPTM Event Trigger enable control 0: Disable conversion trigger by GPTM events 1: Enable conversion trigger by GPTM events
[1]	ADEXTI	ADC Conversion EXTI Event Trigger enable control 0: Disable conversion trigger by EXTI lines 1: Enable conversion trigger by EXTI lines
[0]	ADSW	ADC Conversion Software Trigger enable control 0: Disable conversion trigger by software trigger bit 1: Enable conversion trigger by software trigger bit

ADC Trigger Source Register – ADCTSR

This register contains the trigger source selection and the software trigger bit of the conversion.

Offset: 0x074

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved					TME		
Type/Reset						RW 0	RW 0	RW 0
	23	22	21	20	19	18	17	16
	Reserved					TMS		
Type/Reset						RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
	Reserved				ADEXTIS			
Type/Reset					RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	Reserved							ADSC
Type/Reset								RW 0

Bits	Field	Descriptions
[26:24]	TME	GPTM Trigger Event Selection of ADC Conversion 000: GPTM MTO event 001: GPTM CH0O event 010: GPTM CH1O event 011: GPTM CH2O event 100: GPTM CH3O event Others: Reserved – Should not be used to avoid unpredictable results
[18:16]	TMS	GPTM Trigger Timer Selection of ADC Conversion 010: GPTM Others: Reserved – Should not be used to avoid unpredictable results
[11:8]	ADEXTIS	EXTI Trigger Source Selection of ADC Conversion 0x00: EXTI line 0 0x01: EXTI line 1 … 0x0F: EXTI line 15 Note that the EXTI line active edge to start an A/D conversion is determined in the External Interrupt/Event Control Unit, EXTI.
[0]	ADSC	ADC Conversion Software Trigger Bit 0: No Operation 1: Start conversion immediately This bit is set by software to start a conversion manually and cleared by hardware automatically after conversion started.

ADC Watchdog Control Register – ADCWCR

This register provides the control bits and status of the ADC watchdog function.

Offset: 0x078

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved				ADUCH			
Type/Reset					RO 0	RO 0	RO 0	RO 0
	23	22	21	20	19	18	17	16
	Reserved				ADLCH			
Type/Reset					RO 0	RO 0	RO 0	RO 0
	15	14	13	12	11	10	9	8
	Reserved				ADWCH			
Type/Reset					RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	Reserved					ADWALL	ADWUE	ADWLE
Type/Reset						RW 0	RW 0	RW 0

Bits	Field	Descriptions
[27:24]	ADUCH	Upper Threshold Channel Status 0000: ADC_IN0 converted data is higher than the upper threshold 0001: ADC_IN1 converted data is higher than the upper threshold ... 1011: ADC_IN7 converted data is higher than the upper threshold Others: Reserved If one of these status bits is set to 1 by the watchdog monitor function, the status field value should first be stored in the user-defined memory location in the corresponding ISR. Otherwise, the ADUCH field will be changed if another input channel converted data is higher than the upper threshold.
[19:16]	ADLCH	Lower Threshold Channel Status 0000: ADC_IN0 converted data is lower than the lower threshold 0001: ADC_IN1 converted data is lower than the lower threshold ... 1011: ADC_IN7 converted data is lower than the lower threshold Others: Reserved If one of these status bits is set to 1 by the watchdog monitor function, the status field value should first be stored in the user-defined memory location in the corresponding ISR. Otherwise, the ADLCH field will be changed if another input channel converted data is lower than the lower threshold.
[11:8]	ADWCH	ADC Watchdog Specific Channel Selection 0000: ADC_IN0 is monitored 0001: ADC_IN1 is monitored ... 1011: ADC_IN7 is monitored Others: Reserved
[2]	ADWALL	ADC Watchdog Specific or All Channel Setting 0: Only the channel which specified by the ASWCH field is monitored 1: All channels are monitored

Bits	Field	Descriptions
[1]	ADWUE	ADC Watchdog Upper Threshold Enable Bit 0: Disable upper threshold monitor function 1: Enable upper threshold monitor function
[0]	ADWLE	ADC Watchdog Lower Threshold Enable Bit 0: Disable lower threshold monitor function 1: Enable lower threshold monitor function

ADC Watchdog Threshold Register – ADCTR

This register specifies the upper and lower threshold of the ADC watchdog function.

Offset: 0x07C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved				ADUT			
Type/Reset					RW 0	RW 0	RW 0	RW 0
	23	22	21	20	19	18	17	16
	ADUT							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
	Reserved				ADLT			
Type/Reset					RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	ADLT							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[27:16]	ADUT	ADC Watchdog Upper Threshold Value Specify the upper threshold for the ADC watchdog monitor function.
[11:0]	ADLT	ADC Watchdog Lower Threshold Value Specify the lower threshold for the ADC watchdog monitor function.

ADC Interrupt Enable Register – ADCIER

This register contains the ADC interrupt enable bits.

Offset: 0x080

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							ADIEO
Type/Reset								RW 0
	23	22	21	20	19	18	17	16
	Reserved						ADIEU	ADIEL
Type/Reset							RW 0	RW 0
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved					ADIEC	ADIEG	ADIES
Type/Reset						RW 0	RW 0	RW 0

Bits	Field	Descriptions
[24]	ADIEO	ADC Data Register Overwrite Interrupt enable 0: ADC data register overwrite interrupt is disabled 1: ADC data register overwrite interrupt is enabled
[17]	ADIEU	ADC Watchdog Upper Threshold Interrupt enable 0: ADC watchdog upper threshold interrupt is disabled 1: ADC watchdog upper threshold interrupt is enabled
[16]	ADIEL	ADC Watchdog Lower Threshold Interrupt enable 0: ADC watchdog lower threshold interrupt is disabled 1: ADC watchdog lower threshold interrupt is enabled
[2]	ADIEC	ADC Cycle EOC Interrupt enable 0: ADC cycle end of conversion interrupt is disabled 1: ADC cycle end of conversion interrupt is enabled
[1]	ADIEG	ADC Subgroup EOC Interrupt enable 0: ADC subgroup end of conversion interrupt is disabled 1: ADC subgroup end of conversion interrupt is enabled
[0]	ADIES	ADC Single EOC Interrupt enable 0: ADC single end of conversion interrupt is disabled 1: ADC single end of conversion interrupt is enabled

ADC Interrupt Raw Status Register – ADCIRAW

This register contains the ADC interrupt raw status bits.

Offset: 0x084

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							ADIRAWO
Type/Reset								RO 0
	23	22	21	20	19	18	17	16
	Reserved						ADIRAWU	ADIRAWL
Type/Reset							RO 0	RO 0
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved					ADIRAWC	ADIRAWG	ADIRAWS
Type/Reset						RO 0	RO 0	RO 0

Bits	Field	Descriptions
[24]	ADIRAWO	ADC Data Register Overwrite Interrupt Raw Status 0: ADC data register overwrite event does not occur 1: ADC data register overwrite event occurs
[17]	ADIRAWU	ADC Watchdog Upper Threshold Interrupt Raw Status 0: ADC watchdog upper threshold event does not occur 1: ADC watchdog upper threshold event occurs
[16]	ADIRAWL	ADC Watchdog Lower Threshold Interrupt Raw Status 0: ADC watchdog lower threshold event does not occur 1: ADC watchdog lower threshold event occurs
[2]	ADIRAWC	ADC Cycle EOC Interrupt Raw Status 0: ADC cycle end of conversion event does not occur 1: ADC cycle end of conversion event occurs
[1]	ADIRAWG	ADC Subgroup EOC Interrupt Raw Status 0: ADC subgroup end of conversion event does not occur 1: ADC subgroup end of conversion event occurs
[0]	ADIRAWS	ADC Single EOC Interrupt Raw Status 0: ADC single end of conversion event does not occur 1: ADC single end of conversion event occurs

ADC Interrupt Status Register – ADCISR

This register contains the ADC interrupt masked status bits. The corresponding interrupt status will be set to 1 if the associated interrupt event occurs and the related enable bit is set to 1.

Offset: 0x088

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							ADISRO
Type/Reset								RO 0
	23	22	21	20	19	18	17	16
	Reserved						ADISRU	ADISRL
Type/Reset							RO 0	RO 0
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved					ADISRC	ADISRG	ADISRS
Type/Reset						RO 0	RO 0	RO 0

Bits	Field	Descriptions
[24]	ADISRO	ADC Data Register Overwrite Interrupt Status 0: ADC data register overwrite interrupt does not occur or the data register overwrite interrupt is disabled. 1: ADC data register overwrite interrupt occurs as the data register overwrite interrupt is enabled.
[17]	ADISRU	ADC Watchdog Upper Threshold Interrupt Status 0: ADC watchdog upper threshold interrupt does not occur or the watchdog upper threshold interrupt is disabled. 1: ADC watchdog upper threshold interrupt occurs as the watchdog upper threshold interrupt is enabled.
[16]	ADISRL	ADC Watchdog Lower Threshold Interrupt Status 0: ADC watchdog lower threshold interrupt does not occur or the watchdog lower threshold interrupt is disabled. 1: ADC watchdog lower threshold interrupt occurs as the watchdog lower threshold interrupt is enabled.
[2]	ADISRC	ADC Cycle EOC Interrupt Status 0: ADC cycle end of conversion interrupt does not occur or the cycle end of conversion interrupt is disabled. 1: ADC cycle end of conversion interrupt occurs as the cycle end of conversion interrupt is enabled.
[1]	ADISRG	ADC Subgroup EOC Interrupt Status 0: ADC subgroup end of conversion interrupt does not occur or the subgroup end of conversion interrupt is disabled. 1: ADC subgroup end of conversion interrupt occurs as the subgroup end of conversion interrupt is enabled.
[0]	ADISRS	ADC Single EOC Interrupt Status 0: ADC single end of conversion interrupt does not occur or the single end of conversion interrupt is disabled. 1: ADC single end of conversion interrupt occurs as the single end of conversion interrupt is enabled.

ADC Interrupt Clear Register – ADCICLR

This register provides the clear bits used to clear the interrupt raw and masked status of the ADC. These bits are set to 1 by software to clear the interrupt status and automatically cleared to 0 by hardware after being set to 1.

Offset: 0x08C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							ADICLRO
Type/Reset								WO 0
	23	22	21	20	19	18	17	16
	Reserved						ADICLRU	ADICLRL
Type/Reset							WO 0	WO 0
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved					ADICLRC	ADICLRG	ADICLRS
Type/Reset						WO 0	WO 0	WO 0

Bits	Field	Descriptions
[24]	ADICLRO	ADC Data Register Overwrite Interrupt Status Clear Bit 0: No effect 1: Clear ADISRO and ADIRAWO bits
[17]	ADICLRU	ADC Watchdog Upper Threshold Interrupt Status Clear Bit 0: No effect 1: Clear ADISRU and ADIRAWU bits
[16]	ADICLRL	ADC Watchdog Lower Threshold Interrupt Status Clear Bit 0: No effect 1: Clear ADISRL and ADIRAWL bits
[2]	ADICLRC	ADC Cycle EOC Interrupt Status Clear Bit 0: No effect 1: Clear ADISRC and ADIRAWC bits
[1]	ADICLRG	ADC Subgroup EOC Interrupt Status Clear Bit 0: No effect 1: Clear ADISRG and ADIRAWG bits
[0]	ADICLRS	ADC Single EOC Interrupt Status Clear Bit 0: No effect 1: Clear ADISRS and ADIRAWS bits

13 General-Purpose Timer (GPTM)

Introduction

The General-Purpose Timer consists of one 16-bit up/down-counter, four 16-bit Capture/Compare Registers (CCRs), one 16-bit Counter-Reload Register (CRR) and several control/status registers. It can be used for a variety of purposes including general timer, input signal pulse width measurement or output waveform generation such as single pulse generation or PWM output. The GPTM supports an encoder interface using a quadrature decoder with two inputs.

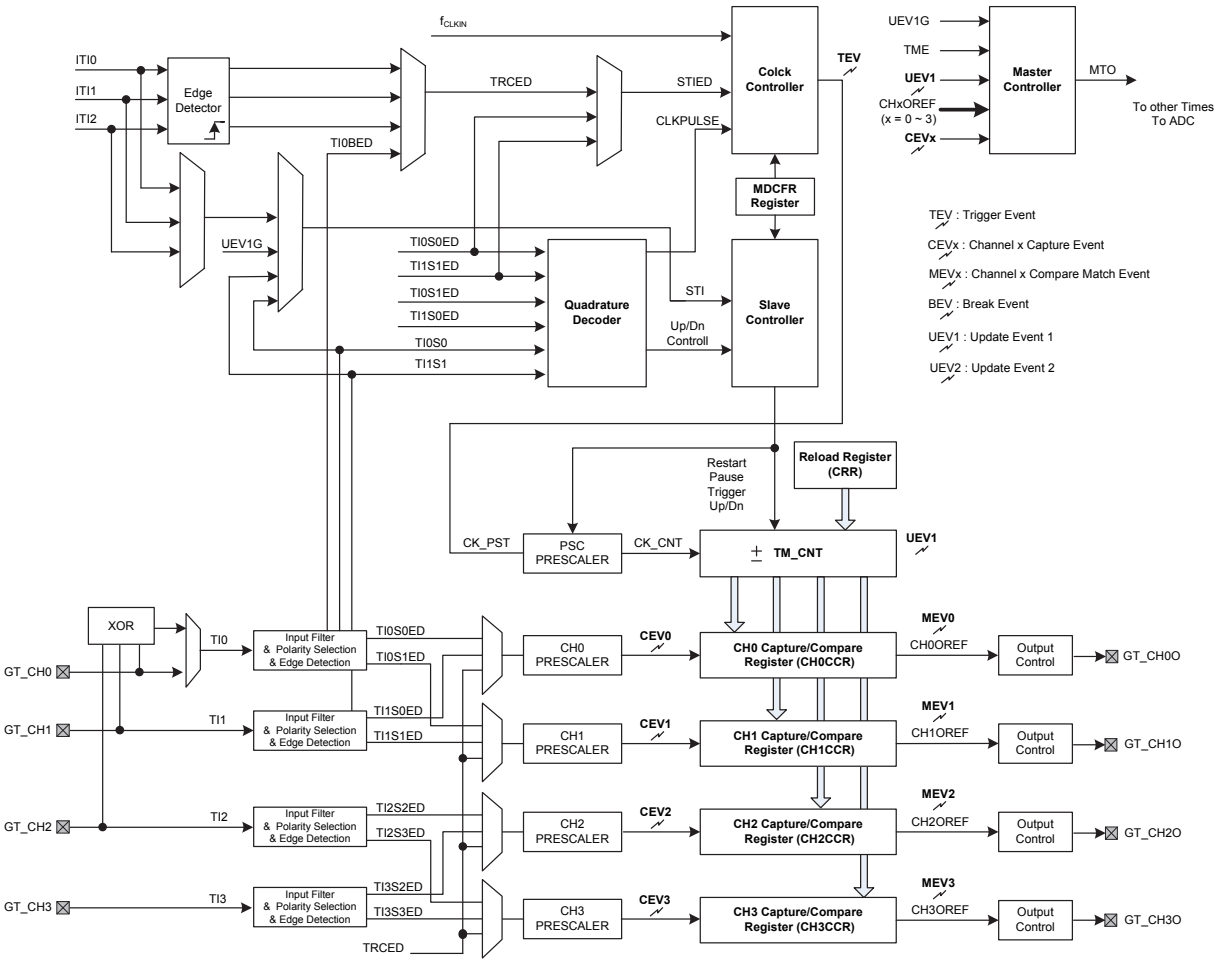


Figure 29. GPTM Block Diagram

Features

- 16-bit up/down auto-reload counter
- 16-bit programmable prescaler that allows division of the counter clock frequency by any factor between 1 and 65536
- Up to 4 independent channels for:
  - Input Capture function
  - Compare Match Output
  - Generation of PWM waveform – Edge and Center-aligned Mode
  - Single Pulse Mode Output
- Encoder interface controller with two inputs using quadrature decoder
- Synchronization circuit to control the timer with external signals and to interconnect several timers together
- Interrupt generation with the following events:
  - Update event
  - Trigger event
  - Input capture event
  - Output compare match event
- GPTM Master/Slave mode controller

Functional Descriptions

Counter Mode

Up-Counting

In this mode the counter counts continuously from 0 to the counter-reload value, which is defined in the CRR register, in a count-up direction. Once the counter reaches the counter-reload value, the Timer Module generates an overflow event and the counter restarts to count once again from 0. This action will continue repeatedly. The counting direction bit DIR in the CNTCFR register should be set to 0 for the up-counting mode.

When the update event is generated by setting the UEVG bit in the EVGR register to 1, the counter value will also be initialized to 0.

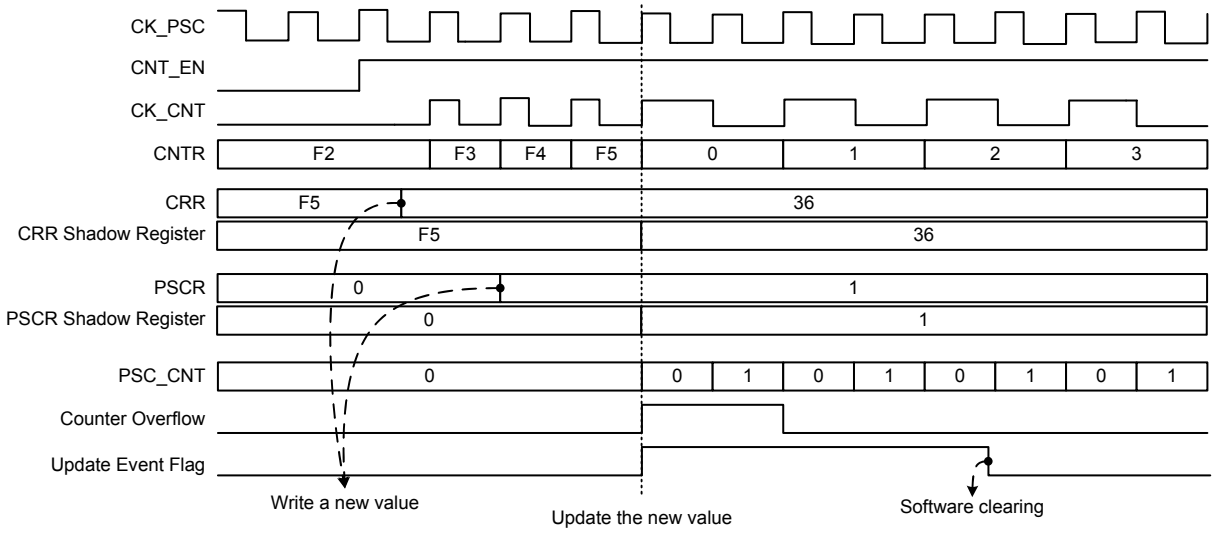


Figure 30. Up-counting Example

Down-Counting

In this mode the counter counts continuously from the counter-reload value, which is defined in the CRR register, to 0 in a count-down direction. Once the counter reaches 0, the Timer module generates an underflow event and the counter restarts to count once again from the counter-reload value. This action will continue repeatedly. The counting direction bit DIR in the CNTCFR register should be set to 1 for the down-counting mode.

When the update event is set by the UEVG bit in the EVGR register, the counter value will also be initialized to the counter-reload value.

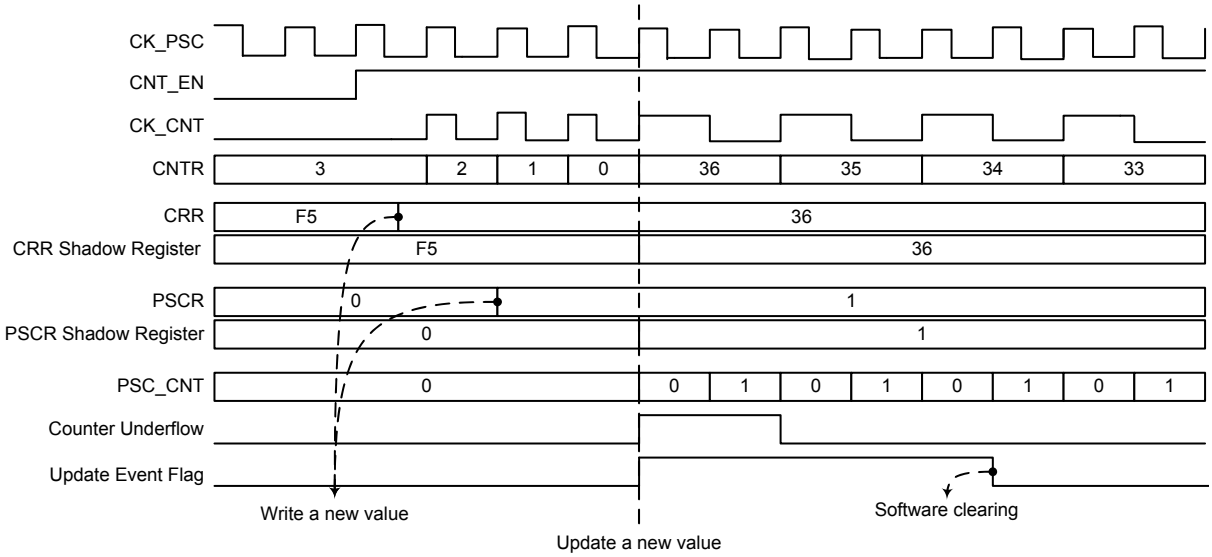


Figure 31. Down-counting Example

Center-Align Counting

In the center-aligned counting mode, the counter counts up from 0 to the counter-reload value and then counts down to 0 alternatively. The Timer module generates an overflow event when the counter counts to the counter-reload value in the up-counting mode and generates an underflow event when the counter counts to 0 in the down-counting mode. The counting direction bit DIR in the CNTCFR register is read-only and indicates the counting direction when in the center-align mode. The counting direction is updated by hardware automatically.

Setting the UEVG bit in the EVGR register will initialize the counter value to 0 irrespective of whether the counter is counting up or down in the center-align counting mode.

The UEVIF bit in the INTSR register can be set to 1 when an overflow or underflow event or both of them occur according to the CMSEL field setting in the CNTCFR register.

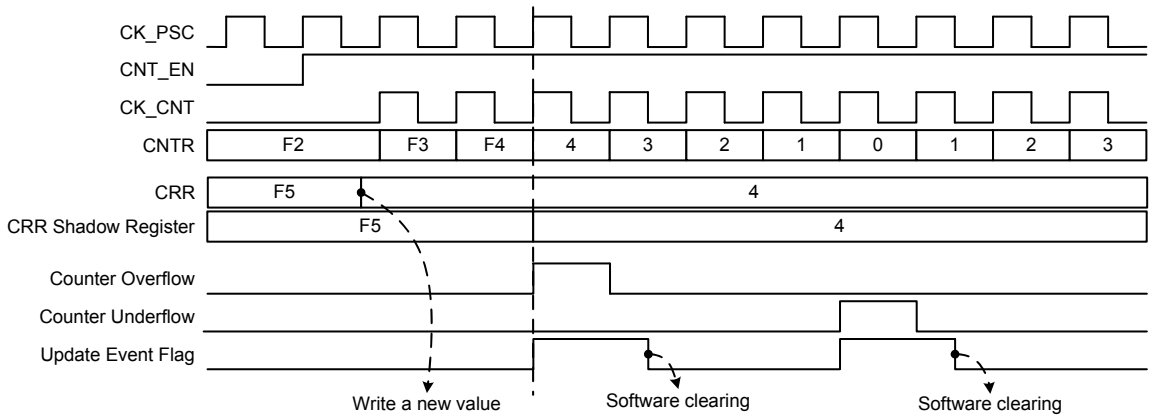


Figure 32. Center-aligned Counting Example

Clock Controller

The following describes the Timer Module clock controller which determines the clock source of the internal prescaler counter.

- Internal APB clock f_{CLKIN}:
  The default internal clock source is the APB clock f_{CLKIN} used to drive the counter prescaler when the slave mode is disabled. When the slave mode selection bits SMSEL are set to 0x4, 0x5 or 0x6, the internal APB clock f_{CLKIN} is the counter prescaler driving clock source. If the slave mode controller is enabled by setting SMSEL field in the MDCFR register to an available value including 0x1, 0x2, 0x3 and 0x7, the prescaler is clocked by other clock sources selected by the TRSEL field in the TRCFR register and described as follows.

- Quadrature Decoder:
  To select Quadrature Decoder mode the SMSEL field should be set to 0x1, 0x2 or 0x3 in the MDCFR register. The Quadrature Decoder function uses two input states of the GT_CH0 and GT_CH1 pins to generate the clock pulse to drive the counter prescaler. The counting direction bit DIR is modified by hardware automatically at each transition on the input source signal. The input source signal can be derived from the GT_CH0 pin only, the GT_CH1 pin only or both GT_CH0 and GT_CH1 pins.

- STIED:
  The counter prescaler can count during each rising edge of the STI signal. This mode can be selected by setting the SMSEL field to 0x7 in the MDCFR register. Here the counter will act as an event counter. The input event, known as STI here, can be selected by setting the TRSEL field to an available value except the value of 0x0. When the STI signal is selected as the clock source, the internal edge detection circuitry will generate a clock pulse during each STI signal rising edge to drive the counter prescaler. It is important to note that if the TRSEL field is set to 0x0 to select the software UEVG bit as the trigger source, then when the SMSEL field is set to 0x7, the counter will be updated instead of counting.

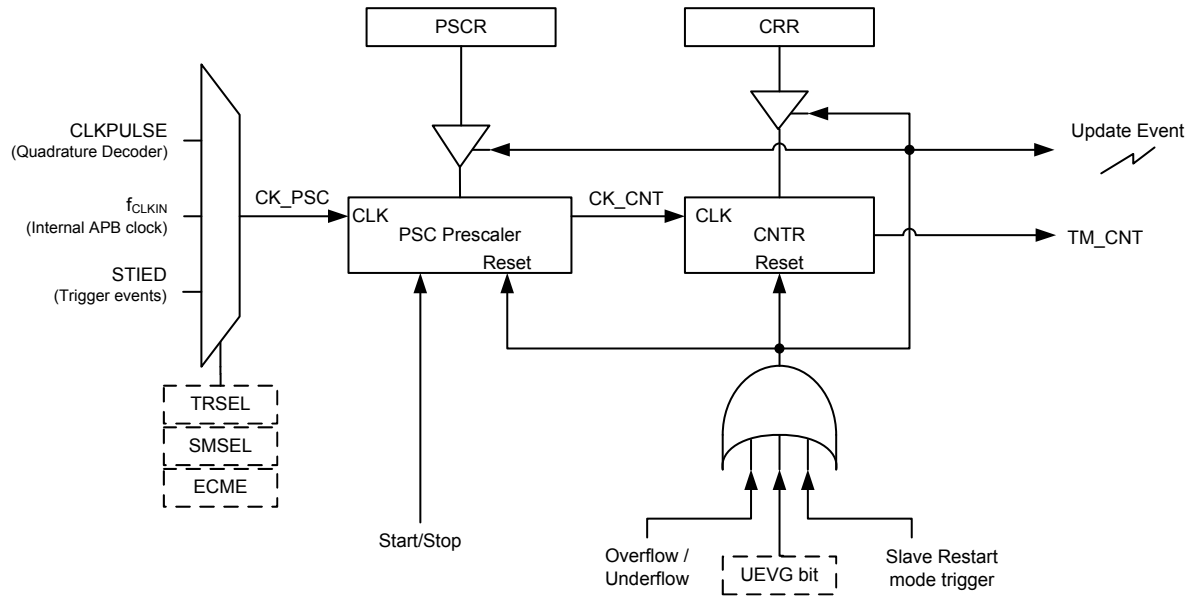


Figure 33. GPTM Clock Selection Source

Trigger Controller

The trigger controller is used to select the trigger source and setup the trigger level or edge trigger condition. For the internal trigger input, it can be selected by the Trigger Selection bits TRSEL in the TRCFR register. For all the trigger sources except the UEVG bit software trigger, the internal edge detection circuitry will generate a clock pulse at each trigger signal rising edge to stimulate some GPTM functions which are triggered by a trigger signal rising edge.

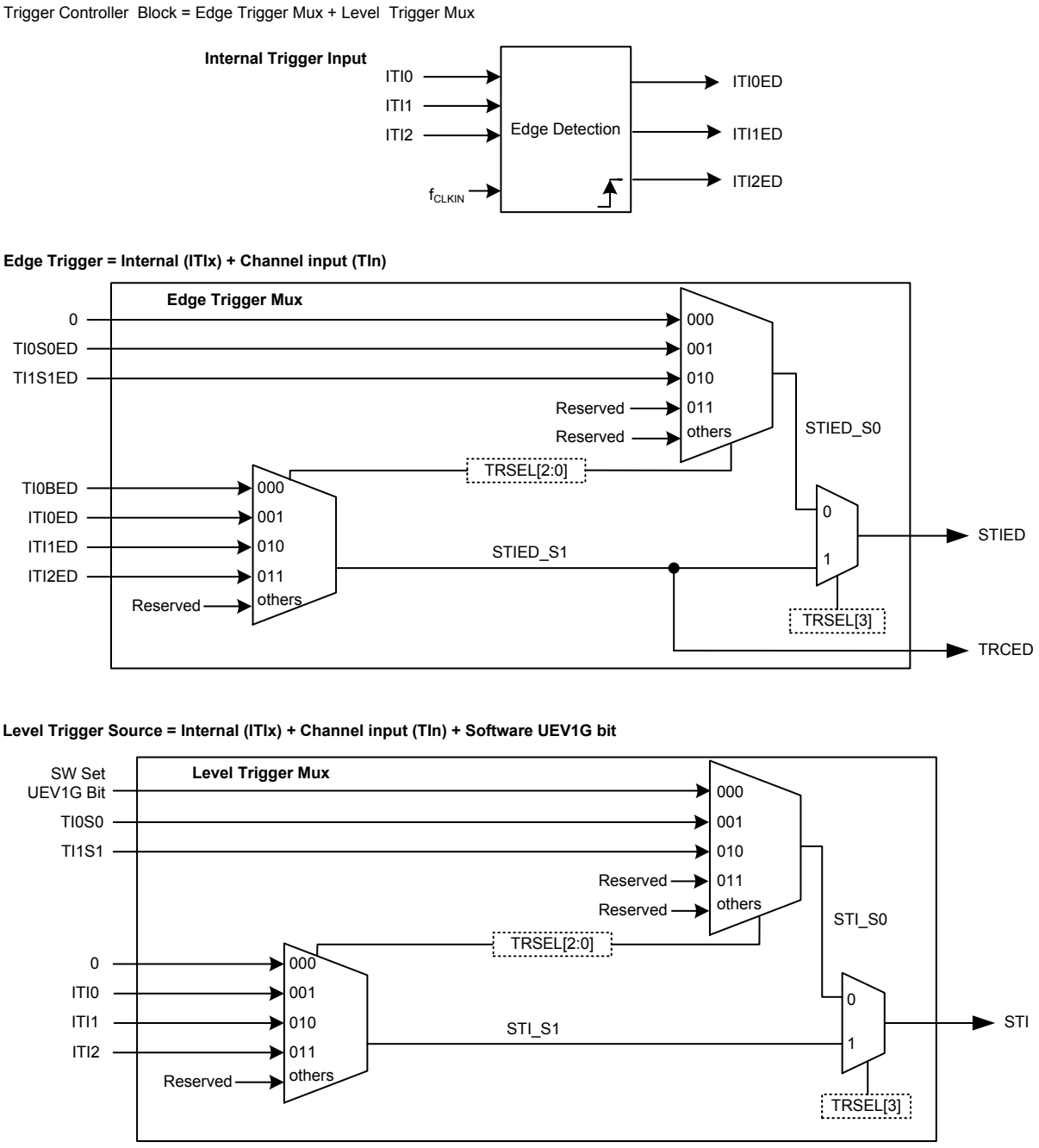


Figure 34. Trigger Controller Block

Slave Controller

The GPTM can be synchronized with an external trigger in several modes including the Restart mode, the Pause mode and the Trigger mode which is selected by the SMSEL field in the MDCFR register. The trigger input of these modes comes from the STI signal which is selected by the TRSEL field in the TRCFR register. The operation modes in the Slave Controller are described in the accompanying sections.

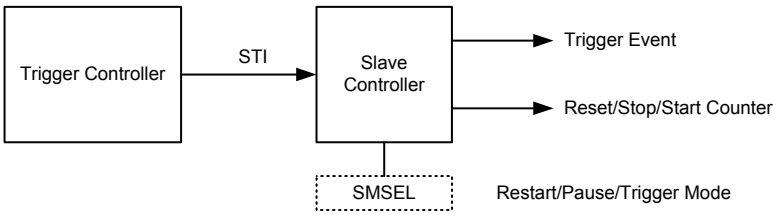


Figure 35. Slave Controller Diagram

Restart Mode

The counter and its prescaler can be reinitialized in response to a rising edge of the STI signal. When a STI rising edge occurs, the update event software generation bit named UEVG will automatically be asserted by hardware and the trigger event flag will also be set. Then the counter and prescaler will be reinitialized. Although the UEVG bit is set to 1 by hardware, the update event does not really occur. It depends upon whether the update event disable control bit UEVDIS is set to 1 or not. If the UEVDIS is set to 1 to disable the update event to occur, there will no update event be generated, however the counter and prescaler are still reinitialized when the STI rising edge occurs. If the UEVDIS bit in the CNTCFR register is cleared to enable the update event to occur, an update event will be generated together with the STI rising edge, then all the preloaded registers will be updated.

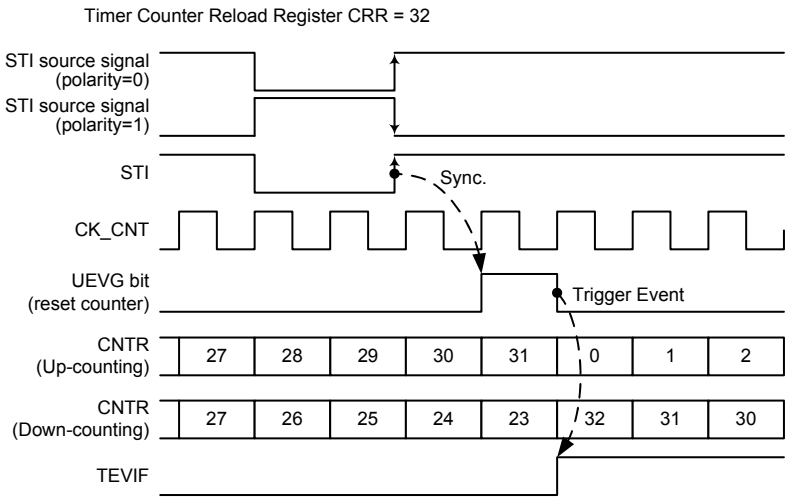


Figure 36. GPTM in Restart Mode

Pause Mode

In the Pause Mode, the selected STI input signal level is used to control the counter start/stop operation. The counter starts to count when the selected STI signal is at a high level and stops counting when the STI signal is changed to a low level, here the counter will maintain its present value and will not be reset. Since the Pause function depends upon the STI level to control the counter stop/start operation, the selected STI trigger signal can not be derived from the TI0BED signal.

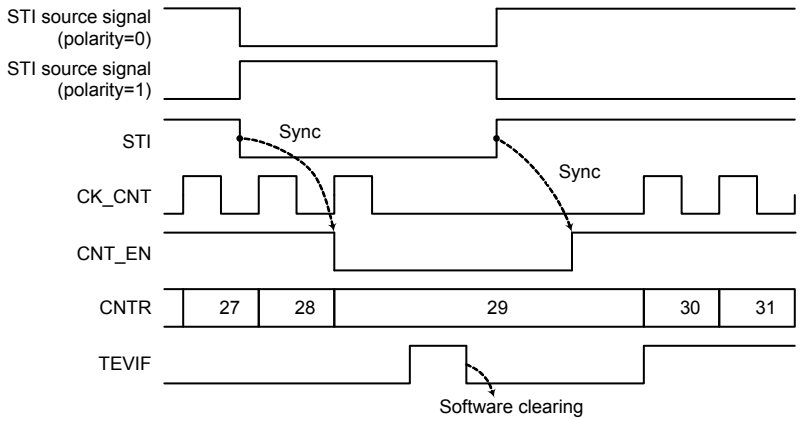


Figure 37. GPTM in Pause Mode

Trigger Mode

After the counter is disabled to count, the counter can resume counting when a STI rising edge signal occurs. When an STI rising edge occurs, the counter will start to count from the current value in the counter. Note that if the STI signal is selected to be derived from the UEVG bit software trigger, the counter will not resume counting. When software triggering using the UEVG bit is selected as the STI source signal, there will be no clock pulse generated which can be used to make the counter resume counting. Note that the STI signal is only used to enable the counter to resume counting and has no effect on controlling the counter to stop counting.

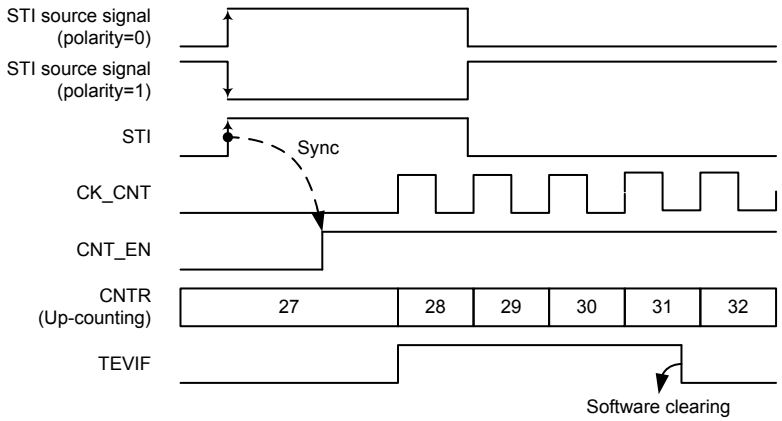


Figure 38. GPTM in Trigger Mode

Master Controller

The GPTMs and MCTMs can be linked together internally for timer synchronization or chaining. When one GPTM is configured to be in the Master Mode, the GPTM Master Controller will generate a Master Trigger Output (MTO) signal which includes a reset, a start, a stop signal or a clock source which is selected by the MMSEL field in the MDCFR register to trigger or drive another GPTM or MCTM, if exists, which is configured in the Slave Mode.

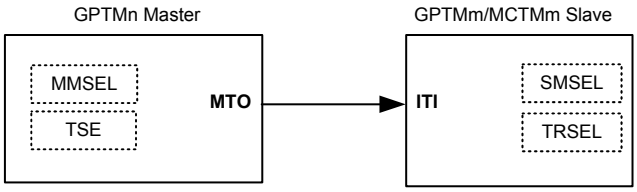


Figure 39. Master GPTMn and Slave GPTMm/MCTMm Connection

The Master Mode Selection bits, MMSEL, in the MDCFR register are used to select the MTO source for synchronizing another slave GPTM or MCTM if exists.

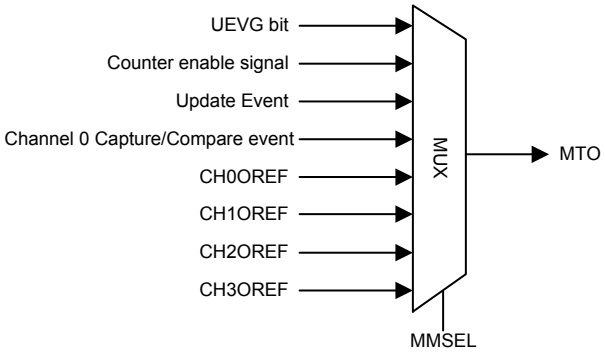


Figure 40. MTO Selection

For example, setting the MMSEL field to 0x5 is to select the CH1OREF signal as the MTO signal to synchronize another slave GPTM or MCTM. For a more detailed description, refer to the related MMSEL field definitions in the MDCFR register.

Channel Controller

The GPTM has four independent channels which can be used as capture inputs or compare match outputs. Each capture input or compare match output channel is composed of a preload register and a shadow register. Data access of the APB bus is always through the read/write preload register.

When used in the input capture mode, the counter value is captured into the CHxCCR shadow register first and then transferred into the CHxCCR preload register when the capture event occurs.

When used in the compare match output mode, the contents of the CHxCCR preload register is copied into the associated shadow register; the counter value is then compared with the register value.

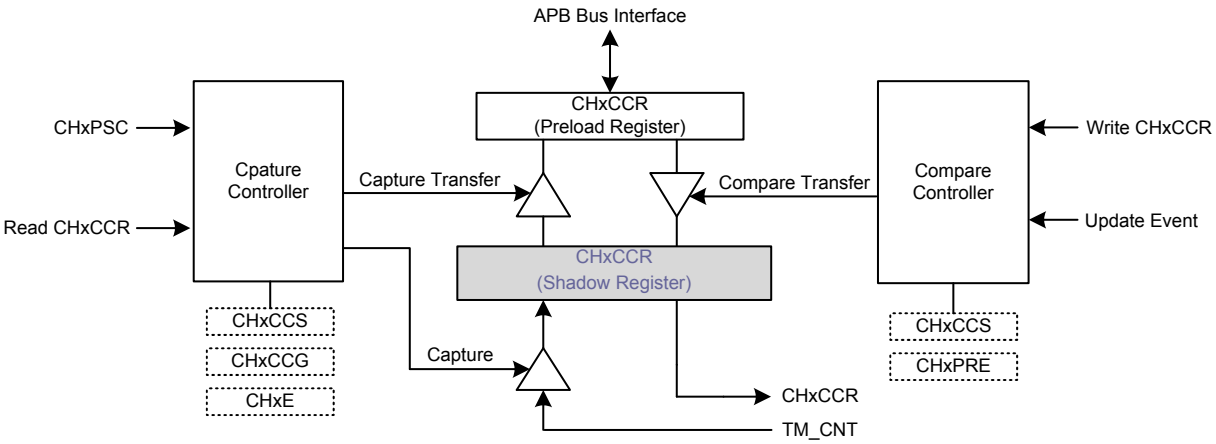


Figure 41. Capture/Compare Block Diagram

Capture Counter Value Transferred to CHxCCR

When the channel is used as a capture input, the counter value is captured into the Channel Capture/Compare Register (CHxCCR) when an effective input signal transition occurs. Once the capture event occurs, the CHxCCIF flag in the INTSR register is set accordingly. If the CHxCCIF bit is already set, i.e., the flag has not yet been cleared by software, and another capture event on this channel occurs, the corresponding channel Over-Capture flag, named CHxOCF, will be set.

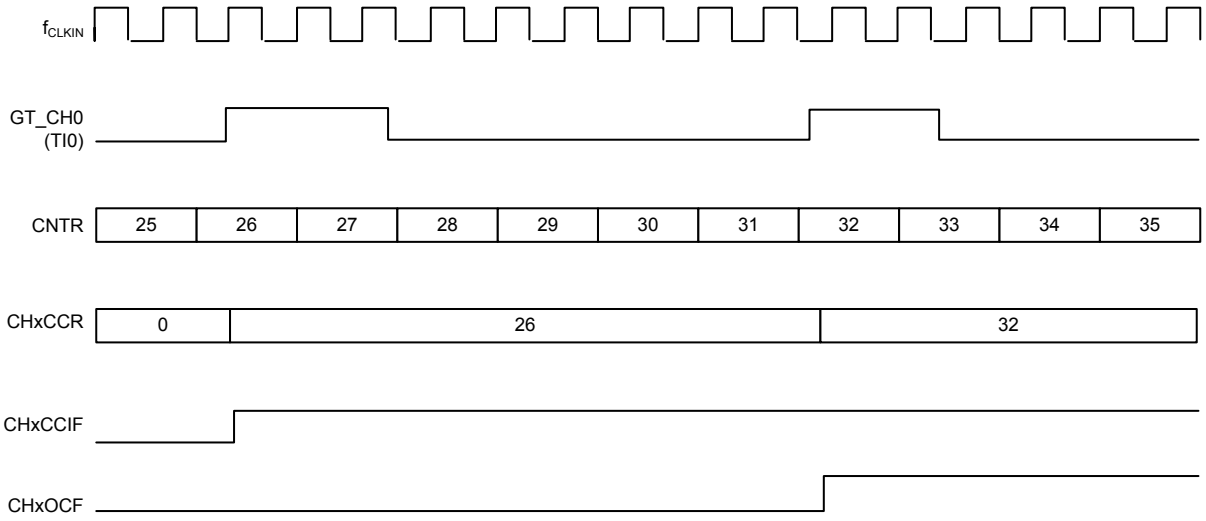


Figure 42. Input Capture Mode

Pulse Width Measurement

The input capture mode can be also used for pulse width measurement from signals on the GT_CHx pins, TIx. The following example shows how to configure the GPTM operated in the input capture mode to measure the high pulse width and the input period on the GT_CH0 pin using channel 0 and channel 1. The basic steps are shown as follows.

- Configure the capture channel 0 (CH0CCS = 0x1) to select the TI0 signal as the capture input.
- Configure the CH0P bit to 0 to choose the rising edge of the TI0 input as the active polarity.
- Configure the capture channel 1 (CH1CCS = 0x2) to select the TI0 signal as the capture input.
- Configure the CH1P bit to 1 to choose the falling edge of the TI0 input as the active polarity.
- Configure the TRSEL bits to 0x0001 to select TI0S0 as the trigger input.
- Configure the Slave controller to operate in the Restart mode by setting the SMSEL field in the MDCFR register to 0x4.
- Enable the input capture mode by setting the CH0E and CH1E bits in the CHCTR register to 1.

As the following diagram shows, the high pulse width on the GT_CH0 pin will be captured into the CH1CCR register while the input period will be captured into the CH0CCR register after input capture operation.

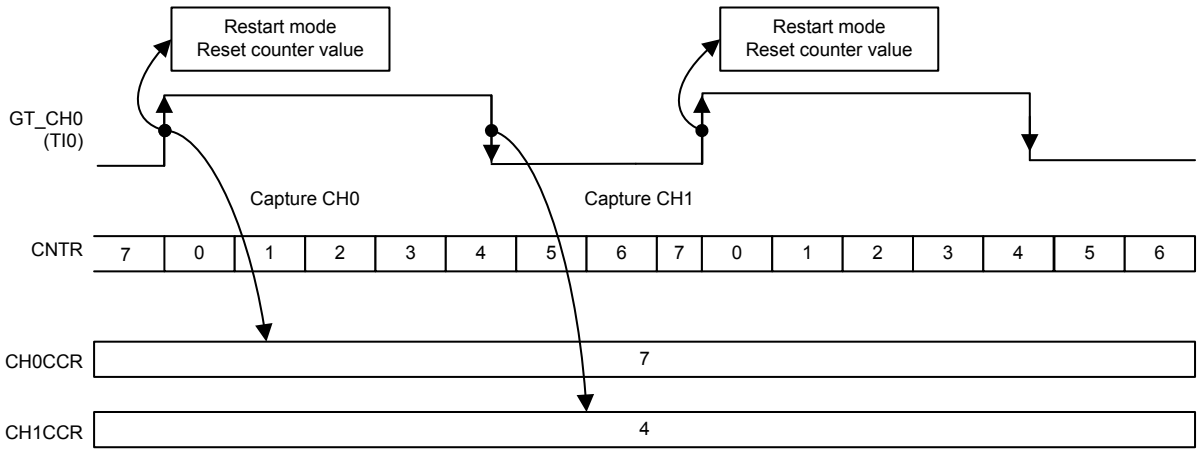


Figure 43. PWM Pulse Width Measurement Example

Input Stage

The input stage consists of a digital filter, a channel polarity selection, edge detection and a channel prescaler. The channel 0 input signal (TI0) can be chosen to come from the GT_CH0 signal or the Excusive-OR function of the GT_CH0, GT_CH1 and GT_CH2 signals. The channel input signal (TIx) is sampled by a digital filter to generate a filtered input signal TIxFP. Then the channel polarity and the edge detection block can generate a TIxS0ED or TIxS1ED signal for the input capture function. The effective input event number can be set by the channel input prescaler register (CHxPSC).

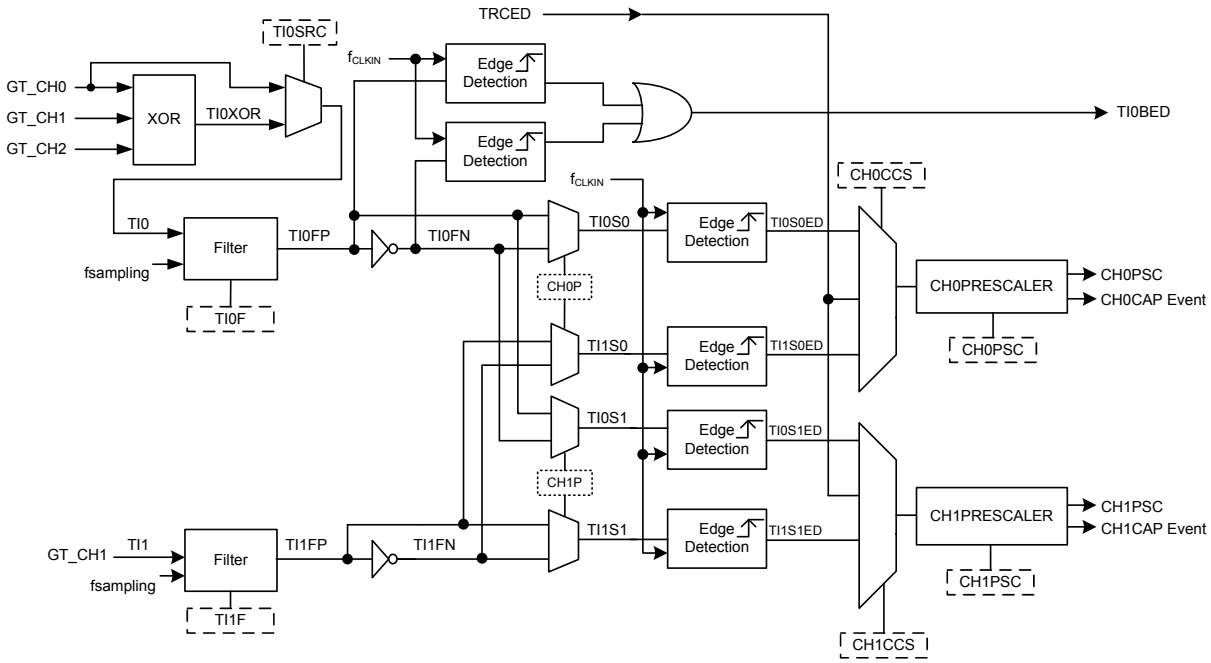


Figure 44. Channel 0 and Channel 1 Input Stages

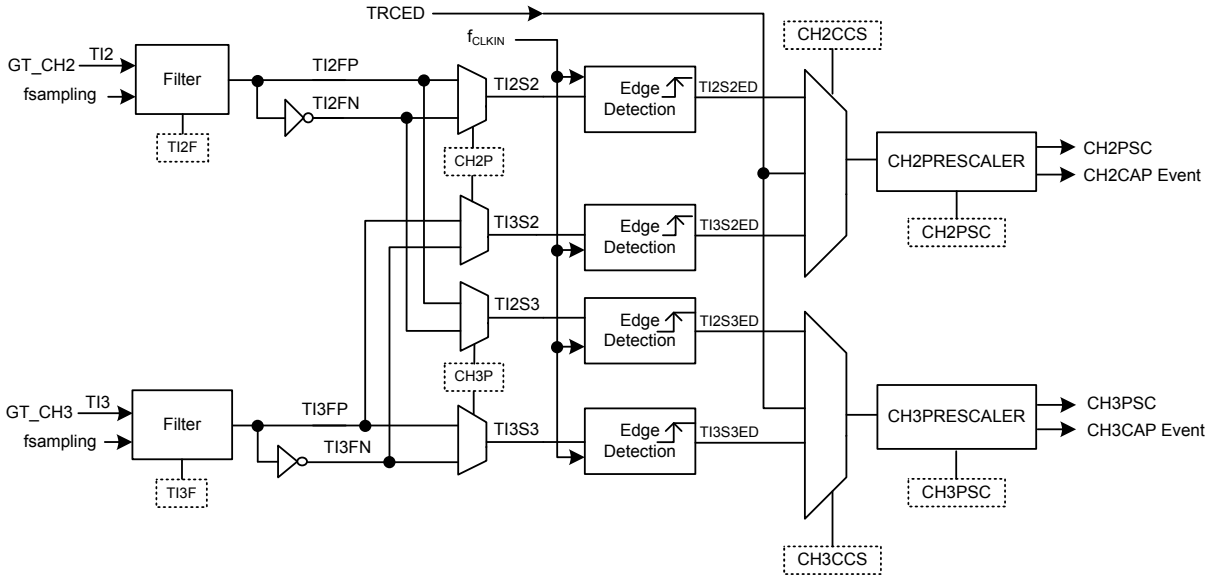


Figure 45. Channel 2 and Channel 3 Input Stages

Digital Filter

The digital filters are embedded in the input stage for the GT_CH0 ~ GT_CH3 pins respectively. The digital filter in the GPTM is an N-event counter where N refers to how many valid transitions are necessary to output a filtered signal. The N value can be 0, 2, 4, 5, 6 or 8 according to the user selection for each filter.

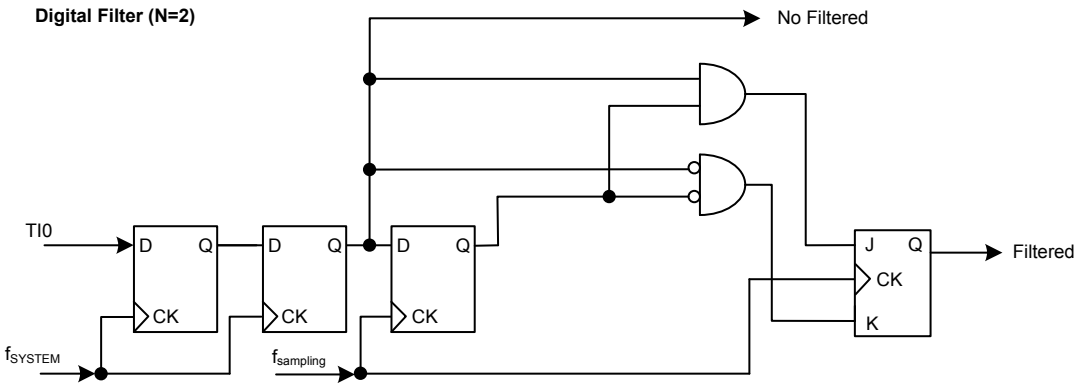


Figure 46. TI0 Digital Filter Diagram with N = 2

Quadrature Decoder

The Quadrature Decoder function uses two quadrantal inputs TI0 and TI1 derived from the GT_CH0 and GT_CH1 pins respectively to interact to generate the counter value. The DIR bit is modified by hardware automatically during each input source transition. The input source can be either TI0 only, TI1 only or both TI0 and TI1, the selection made by setting the SMSEL field to 0x01, 0x02 or 0x03. The mechanism for changing the counter direction is shown in the following table. The Quadrature decoder can be regarded as an external clock with a directional selection. This means that the counter counts continuously in the interval between 0 and the counter-reload value. Therefore, users must configure the CRR register before the counter starts to count.

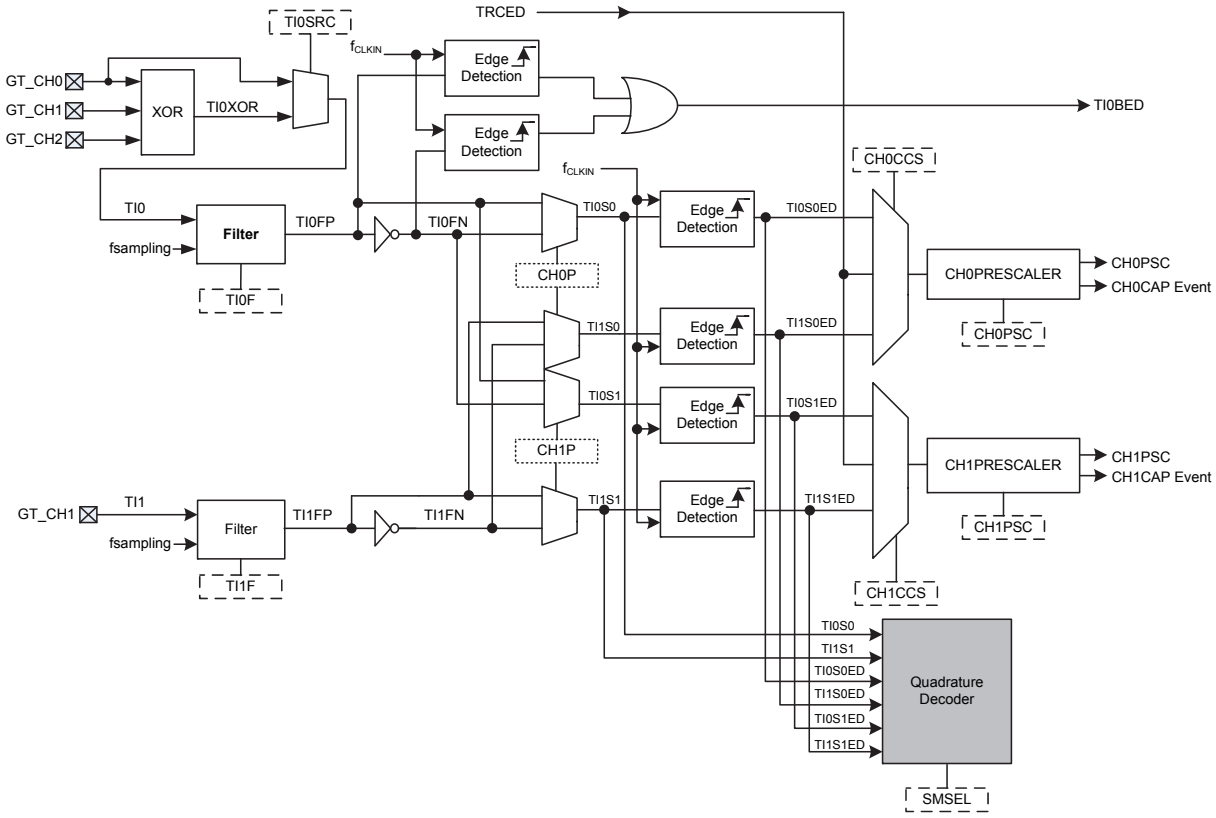


Figure 47. Input Stage and Quadrature Decoder Block Diagram

Table 29. Counting Direction and Encoding Signals

Counting mode	Level	TI0S0		TI1S1	
		Rising	Falling	Rising	Falling
Counting on TI0 only (SMSEL = 0x01)	TI1S1 = High	Down	Up	—	—
	TI1S1 = Low	Up	Down	—	—
Counting on TI1 only (SMSEL = 0x02)	TI0S0 = High	—	—	Up	Down
	TI0S0 = Low	—	—	Down	Up
Counting on TI0 and TI1 (SMSEL = 0x03)	TI1S1 = High	Down	Up	X	X
	TI1S1 = Low	Up	Down	X	X
	TI0S0 = High	X	X	Up	Down
	TI0S0 = Low	X	X	Down	Up

Note: "—" → means "no counting"; "X" → impossible

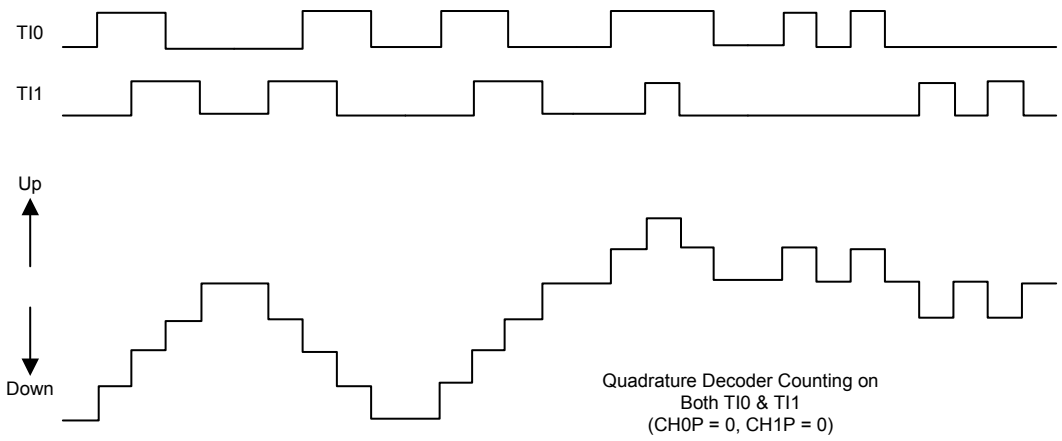


Figure 48. Both TI0 and TI1 Quadrature Decoder Counting

Output Stage

The GPTM has four channels for compare match, single pulse or PWM output function. The channel output GT_CHxO is controlled by the CHxOM, CHxP and CHxE bits in the corresponding CHxOCFR, CHPOLR and CHCTR registers.

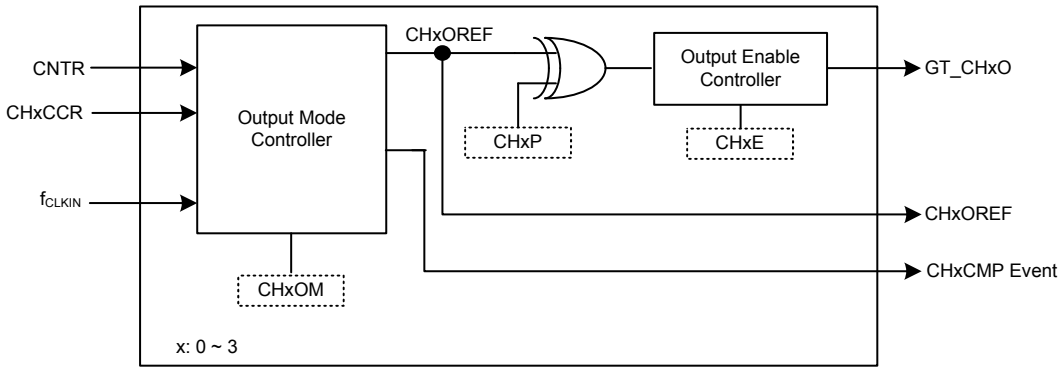


Figure 49. Output Stage Block Diagram

Channel Output Reference Signal

When the GPTM is used in the compare match output mode, the CHxOREF signal (Channel x Output Reference signal) is defined by the CHxOM bit setup. The CHxOREF signal has several types of output function which defines what happens to the output when the counter value matches the contents of the CHxCCR register. In addition to the low, high and toggle CHxOREF output types; there are also PWM mode 1 and PWM mode 2 outputs. In these modes, the CHxOREF signal level is changed according to the count direction and the relationship between the counter value and the CHxCCR content. There are also two modes which will force the output into an inactive or active state irrespective of the CHxCCR content or counter values. With regard to a more detailed description refer to the relative bit definition. The accompanying Table 30 shows a summary of the output type setup.

Table 30. Compare Match Output Setup

CHxOM value	Compare Match Level
0x00	No change
0x01	Clear Output to 0
0x02	Set Output to 1
0x03	Toggle Output
0x04	Force Inactive Level
0x05	Force Active Level
0x06	PWM Mode 1
0x07	PWM Mode 2

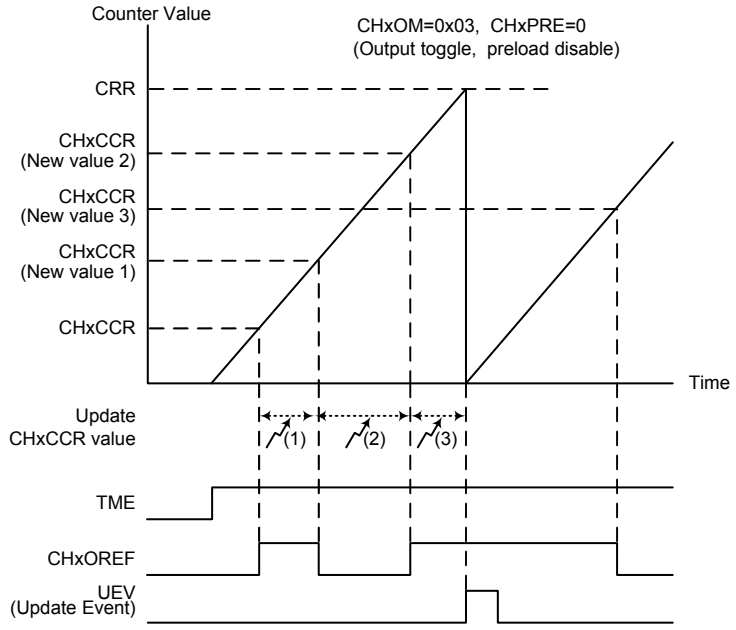


Figure 50. Toggle Mode Channel Output Reference Signal – CHxPRE = 0

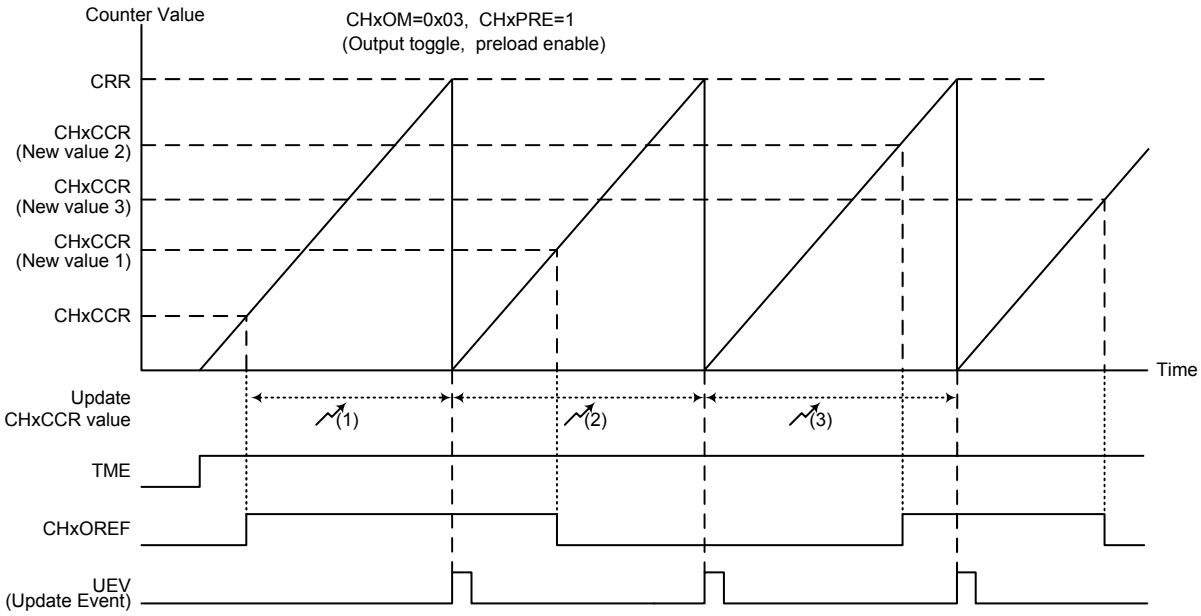


Figure 51. Toggle Mode Channel Output Reference Signal – CHxPRE = 1

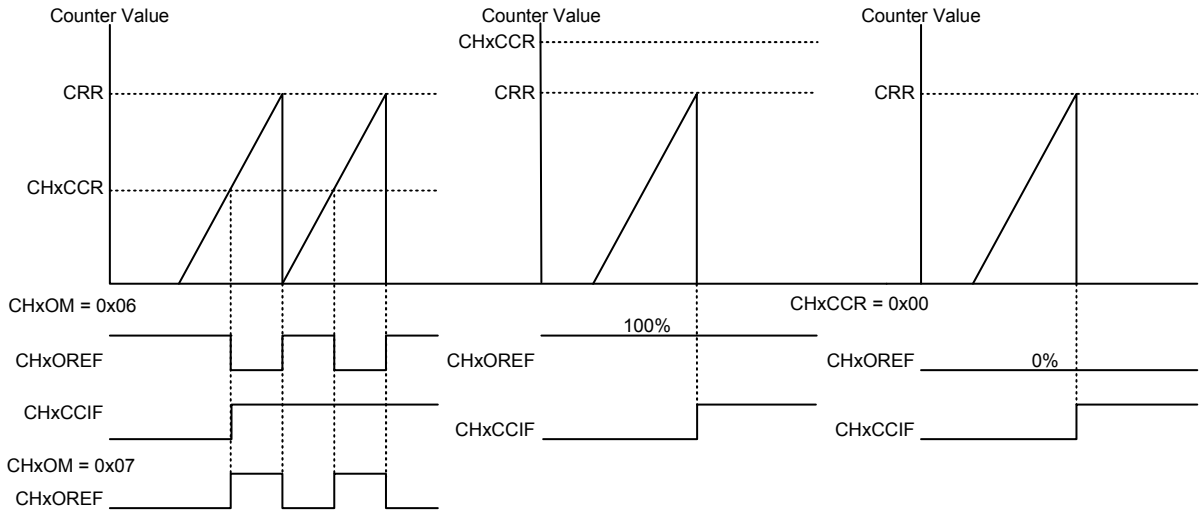


Figure 52. PWM Mode Channel Output Reference Signal and Counter in Up-counting Mode

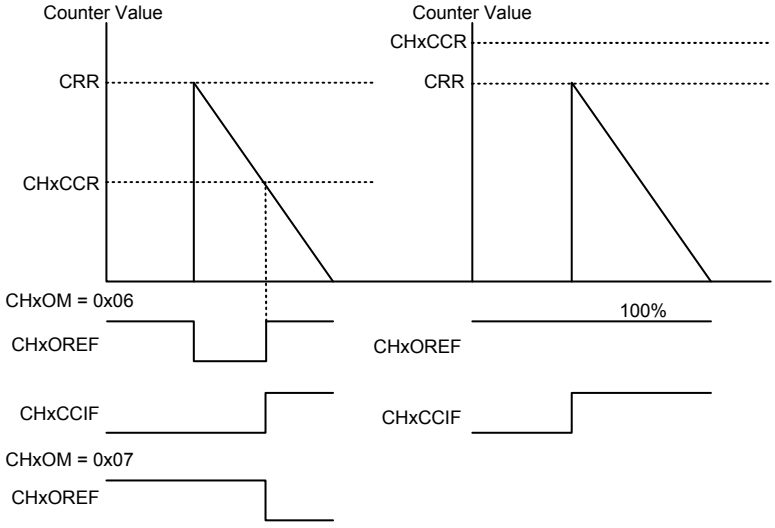


Figure 53. PWM Mode Channel Output Reference Signal and Counter in Down-counting Mode

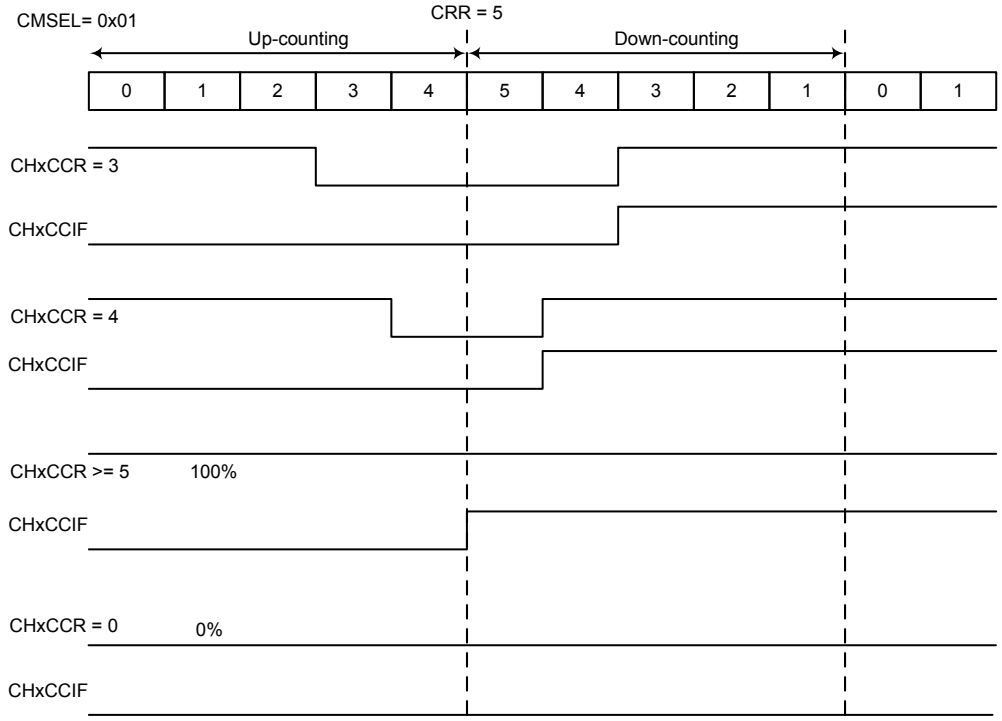


Figure 54. PWM Mode Channel Output Reference Signal and Counter in Centre-align Mode

Update Management

The Update event is used to update the CRR, the PSCR, the CHxACR and the CHxCCR values from the actual registers to the corresponding shadow registers. An update event occurs when the counter overflows or underflows, the software update control bit is triggered or an update event from the slave controller is generated.

The UEVDIS bit in the CNTCFR register can determine whether the update event occurs or not. When the update event occurs, the corresponding update event interrupt will be generated depending upon whether the update event interrupt generation function is enabled or not by configuring the UGDIS bit in the CNTCFR register. For more detail description, refer to the UEVDIS and UGDIS bit definition in the CNTCFR register.

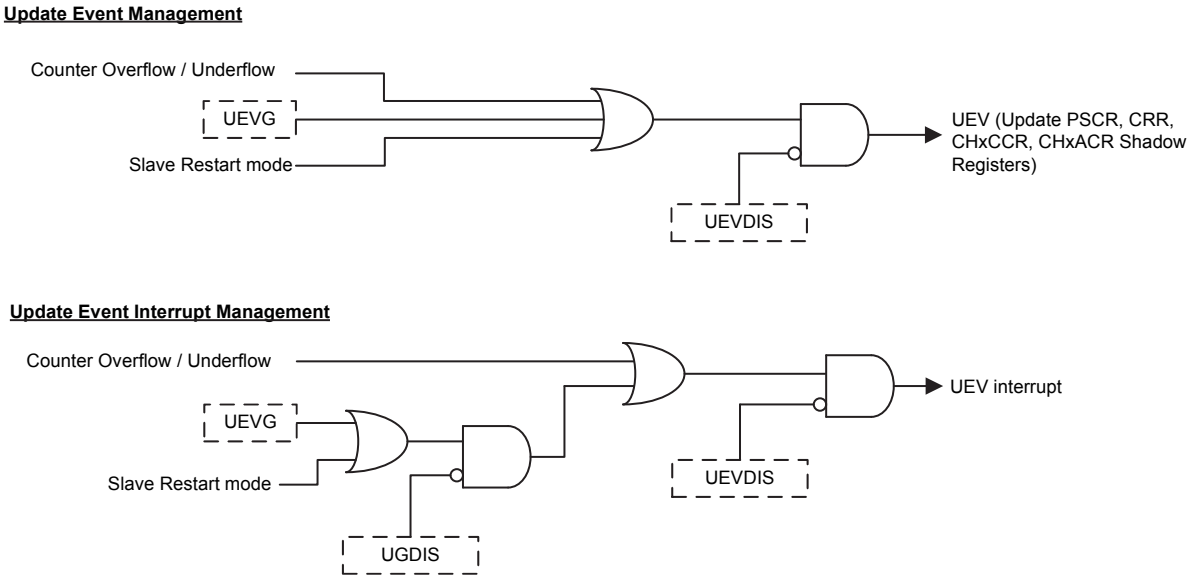


Figure 55. Update Event Setting Diagram

Single Pulse Mode

Once the timer is set to operate in the single pulse mode, it is not necessary to set the timer enable bit TME in the CTR register to 1 to enable the counter. The trigger to generate a pulse can be sourced from the STI signal rising edge or by setting the TME bit to 1 using software. Setting the TME bit to 1 or a trigger from the STI signal rising edge can generate a pulse and then keep the TME bit at a high state until the update event occurs or the TME bit is written to 0 by software. If the TME bit is cleared to 0 using software, the counter will be stopped and its value held. If the TME bit is automatically cleared to 0 by a hardware update event, the counter will be reinitialized.

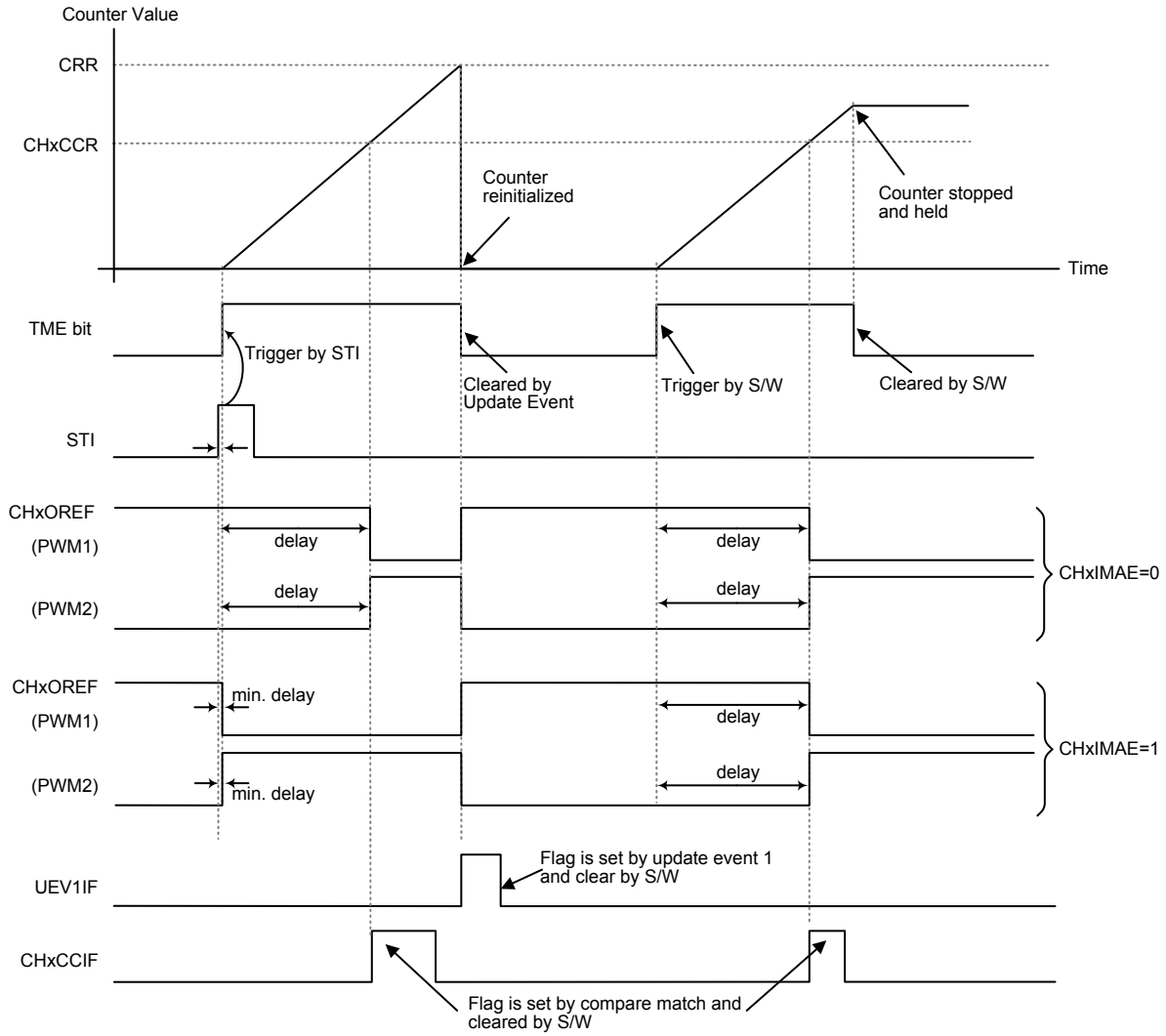


Figure 56. Single Pulse Mode

In the Single Pulse mode, the STI active edge which sets the TME bit to 1 will enable the counter. However, there exist several clock delays to perform the comparison result between the counter value and the CHxCCR value. In order to reduce the delay to a minimum value, the user can set the CHxIMAE bit in each CHxOCFR register. After a STI rising edge trigger occurs in the single pulse mode, the CHxOREF signal will immediately be forced to the state which the CHxOREF signal will change to as the compare match event occurs without taking the comparison result into account. The CHxIMAE bit is available only when the output channel is configured to operate in the PWM1 or PWM2 output mode and the trigger source is derived from the STI signal.

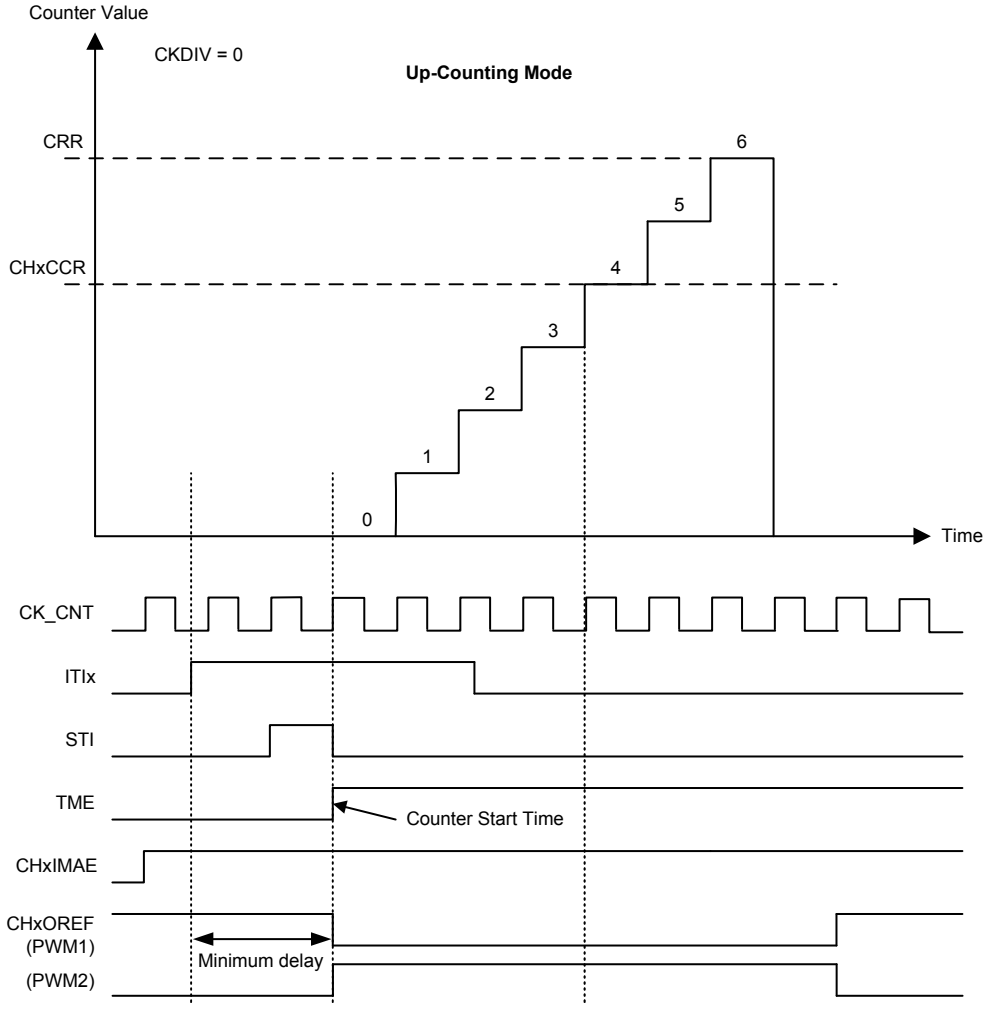


Figure 57. Immediate Active Mode Minimum Delay

Asymmetric PWM Mode

The asymmetric PWM mode allows two center-aligned PWM signals to be generated with a programmable phase shift. The PWM frequency is determined by the value of the CRR register while the duty cycle and the phase-shift are determined by the CHxCCR and CHxACR register. When the counter is counting up, the value in the CHxCCR register will be used as the up-count compare value for the PWM mode. When the counter is in the counting down stage, the value in the CHxACR register will be used as the down-count compare value. The Figure 58 is shown an example for asymmetric PWM mode in center-aligned counting mode.

Note: Asymmetric PWM mode can only be operated in center-aligned counting mode.

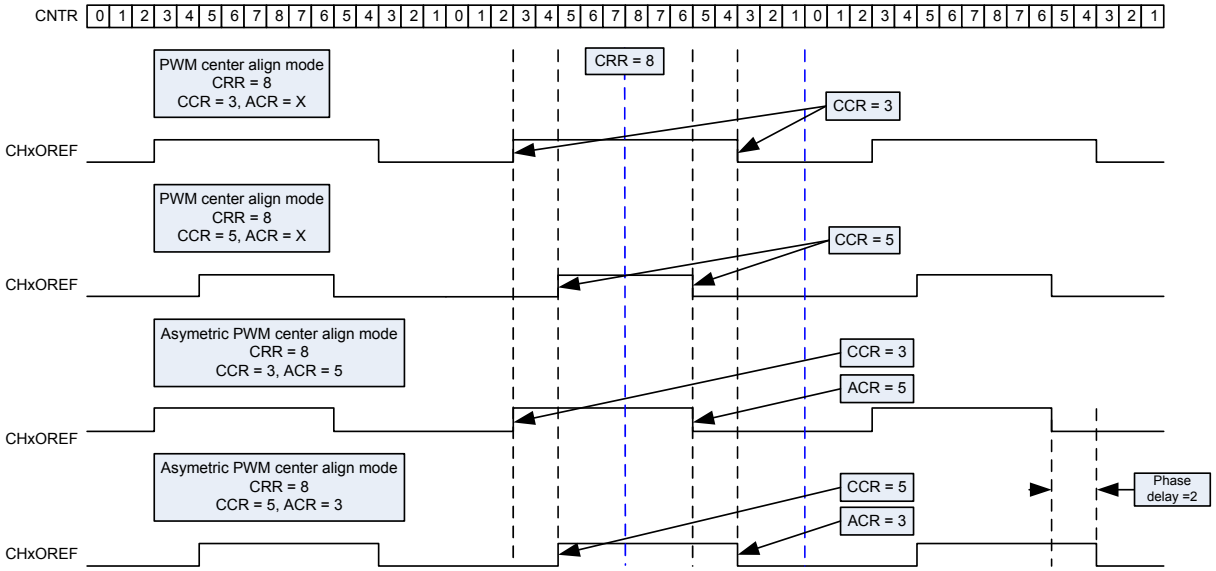


Figure 58. Asymmetric PWM Mode versus Center Align Counting Mode

Trigger ADC Start

To interconnect to the Analog-to-Digital Converter, the GPTM can output the MTO signal or the channel compare match output signal CHxOREF (x = 0 ~ 3) to be used as an Analog-to-Digital Converter input trigger signal.

Register Map

The following table shows the GPTM registers and reset values.

Table 31. GPTM Register Map

Register	Offset	Description	Reset Value
CNTCFR	0x000	Timer Counter Configuration Register	0x0000_0000
MDCFR	0x004	Timer Mode Configuration Register	0x0000_0000
TRCFR	0x008	Timer Trigger Configuration Register	0x0000_0000
CTR	0x010	Timer Control Register	0x0000_0000
CH0ICFR	0x020	Channel 0 Input Configuration Register	0x0000_0000
CH1ICFR	0x024	Channel 1 Input Configuration Register	0x0000_0000
CH2ICFR	0x028	Channel 2 Input Configuration Register	0x0000_0000
CH3ICFR	0x02C	Channel 3 Input Configuration Register	0x0000_0000
CH0OCFR	0x040	Channel 0 Output Configuration Register	0x0000_0000
CH1OCFR	0x044	Channel 1 Output Configuration Register	0x0000_0000
CH2OCFR	0x048	Channel 2 Output Configuration Register	0x0000_0000
CH3OCFR	0x04C	Channel 3 Output Configuration Register	0x0000_0000
CHCTR	0x050	Channel Control Register	0x0000_0000
CHPOLR	0x054	Channel Polarity Configuration Register	0x0000_0000
DICTR	0x074	Timer Interrupt Control Register	0x0000_0000
EVGR	0x078	Timer Event Generator Register	0x0000_0000
INTSR	0x07C	Timer Interrupt Status Register	0x0000_0000
CNTR	0x080	Timer Counter Register	0x0000_0000
PSCR	0x084	Timer Prescaler Register	0x0000_0000
CRR	0x088	Timer Counter Reload Register	0x0000_FFFF
CH0CCR	0x090	Channel 0 Capture/Compare Register	0x0000_0000
CH1CCR	0x094	Channel 1 Capture/Compare Register	0x0000_0000
CH2CCR	0x098	Channel 2 Capture/Compare Register	0x0000_0000
CH3CCR	0x09C	Channel 3 Capture/Compare Register	0x0000_0000
CH0ACR	0x0A0	Channel 0 Asymmetric Compare Register	0x0000_0000
CH1ACR	0x0A4	Channel 1 Asymmetric Compare Register	0x0000_0000
CH2ACR	0x0A8	Channel 2 Asymmetric Compare Register	0x0000_0000
CH3ACR	0x0AC	Channel 3 Asymmetric Compare Register	0x0000_0000

Register Descriptions

Timer Counter Configuration Register – CNTCFR

This register specifies the GPTM counter configuration.

Offset: 0x000

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							DIR
Type/Reset								RW 0
	23	22	21	20	19	18	17	16
	Reserved							CMSEL
Type/Reset							RW 0	RW 0
	15	14	13	12	11	10	9	8
	Reserved							CKDIV
Type/Reset							RW 0	RW 0
	7	6	5	4	3	2	1	0
	Reserved						UGDIS	UEVDIS
Type/Reset							RW 0	RW 0

Bits	Field	Descriptions
[24]	DIR	Counting Direction 0: Count-up 1: Count-down Note: This bit is read only when the Timer is configured to be in the Center-aligned mode or when used as a Quadrature decoder.
[17:16]	CMSEL	Counter Mode Selection 00: Edge aligned mode. Normal up-counting and down-counting available for this mode. Counting direction is defined by the DIR bit. 01: Center aligned mode 1. The counter counts up and down alternatively. The compare match interrupt flag is set during the count-down period. 10: Center aligned mode 2. The counter counts up and down alternatively. The compare match interrupt flag is set during the count-up period. 11: Center aligned mode 3. The counter counts up and down alternatively. The compare match interrupt flag is set during the count-up and count-down period.
[9:8]	CKDIV	Clock Division These two bits define the frequency ratio between the timer clock (f_{CLKIN}) and the dead-time clock (f_{DTS}). The dead-time clock is also used for digital filter sampling clock. 00: $f_{DTS} = f_{CLKIN}$ 01: $f_{DTS} = f_{CLKIN} / 2$ 10: $f_{DTS} = f_{CLKIN} / 4$ 11: Reserved
[1]	UGDIS	Update event interrupt generation disable control 0: Any of the following events will generate an update interrupt - Counter overflow/underflow - Setting the UEVG bit - Update generation through the slave mode 1: Only counter overflow/underflow generates an update interrupt

Bits	Field	Descriptions
[0]	UEVDIS	Update event Disable control 0: Enable the update event request by one of following events: - Counter overflow/underflow - Setting the UEVG bit - Update generation through the slave mode 1: Disable the update event (However the counter and the prescaler are reinitialized if the UEVG bit is set or if a hardware restart is received from the slave mode)

Timer Mode Configuration Register – MDCFR

This register specifies the GPTM master and slave mode selection and single pulse mode.

Offset: 0x004

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							SPMSET
Type/Reset								RW 0
	23	22	21	20	19	18	17	16
	Reserved					MMSEL		
Type/Reset						RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
	Reserved					SMSEL		
Type/Reset						RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	Reserved							TSE
Type/Reset								RW 0

Bits	Field	Descriptions
[24]	SPMSET	Single Pulse Mode Setting 0: Counter counts normally irrespective of whether the update event occurred or not. 1: Counter stops counting at the next update event and then the TME bit is cleared by hardware.

Bits	Field	Descriptions
[18:16]	MMSEL	Master Mode Selection Master mode selection is used to select the MTO signal source which is used to synchronize the other slave timer.

MMSEL [2:0]	Mode	Descriptions
000	Reset Mode	The MTO in the Reset mode is an output derived from one of the following cases: 1. Software setting UEVG bit 2. The STI trigger input signal which will be output on the MTO signal line when the Timer is used in the slave Restart mode
001	Enable Mode	The Counter Enable signal is used as the trigger output.
010	Update Mode	The update event is used as the trigger output according to one of the following cases when the UEVDIS bit is cleared to 0: 1. Counter overflow / underflow 2. Software setting UEVG 3. Slave trigger input when used in slave restart mode
011	Capture/Compare Mode	When a Channel 0 capture or compare match event occurs, it will generate a positive pulse used as the master trigger output.
100	Compare Mode 0	The Channel 0 Output reference signal named CH0OREF is used as the trigger output.
101	Compare Mode 1	The Channel 1 Output reference signal named CH1OREF is used as the trigger output.
110	Compare Mode 2	The Channel 2 Output reference signal named CH2OREF is used as the trigger output.
111	Compare Mode 3	The Channel 3 Output reference signal named CH3OREF is used as the trigger output.

<table>
<tr><th>Bits</th><th>Field</th><th>Descriptions</th></tr>
<tr><td>[10:8]</td><td>SMSEL</td><td>Slave Mode Selection
<table>
<tr><th>SMSEL [2:0]</th><th>Mode</th><th>Descriptions</th></tr>
<tr><td>000</td><td>Disable mode</td><td>The prescaler is clocked directly by the internal clock.</td></tr>
<tr><td>001</td><td>Quadrature Decoder mode 1</td><td>The counter uses the clock pulse generated from the interaction between the TI0 and TI1 signals to drive the counter prescaler. A transition of the TI0 edge is used in this mode depending upon the TI1 level.</td></tr>
<tr><td>010</td><td>Quadrature Decoder mode 2</td><td>The counter uses the clock pulse generated from the interaction between the TI0 and TI1 signals to drive the counter prescaler. A transition of the TI1 edge is used in this mode depending upon the TI0 level.</td></tr>
<tr><td>011</td><td>Quadrature Decoder mode 3</td><td>The counter uses the clock pulse generated from the interaction between the TI0 and TI1 signals to drive the counter prescaler. A transition of one channel edge is used in the quadrature decoder mode 3 depending upon the other channel level.</td></tr>
<tr><td>100</td><td>Restart Mode</td><td>The counter value restarts from 0 or the CRR shadow register value depending upon the counter mode on the rising edge of the STI signal. The registers will also be updated.</td></tr>
<tr><td>101</td><td>Pause Mode</td><td>The counter starts to count when the selected trigger input STI is high. The counter stops counting on the instant, not being reset, when the STI signal changes its state to a low level. Both the counter start and stop control are determined by the STI signal.</td></tr>
<tr><td>110</td><td>Trigger Mode</td><td>The counter starts to count from the original value in the counter on the rising edge of the selected trigger input STI. Only the counter start control is determined by the STI signal.</td></tr>
<tr><td>111</td><td>STIED</td><td>The rising edge of the selected trigger signal STI will clock the counter.</td></tr>
</table></td></tr>
<tr><td>[0]</td><td>TSE</td><td>Timer Synchronization Enable
0: No action
1: Master timer (current timer) will generate a delay to synchronize its slave timer through the MTO signal.</td></tr>
</table>

Timer Trigger Configuration Register – TRCFR

This register specifies the GPTM trigger source selection.

Offset: 0x008

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved				TRSEL			
Type/Reset					RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[3:0]	TRSEL	Trigger Source Selection These bits are used to select the trigger input (STI) for counter synchronizing. 0000: Software Trigger by setting the UEVG bit 0001: Filtered input of channel 0 (TI0S0) 0010: Filtered input of channel 1 (TI1S1) 0011: Reserved 1000: Channel 0 Edge Detector (TI0BED) 1001: Internal Timing Module Trigger 0 (ITI0) 1010: Internal Timing Module Trigger 1 (ITI1) 1011: Internal Timing Module Trigger 2 (ITI2) Others: Default 0 Note: These bits must be updated only when they are not in use, i.e. the slave mode is disabled by setting the SMSEL field to 0x00.

Table 32. GPTM Internal Trigger Connection

Slave Timing Module	ITI0	ITI1	ITI2
GPTM0	GPTM1	MCTM0	MCTM1
GPTM1	GPTM0	MCTM0	MCTM1

Timer Counter Register – CTR

This register specifies the timer enable bit (TME) and CRR buffer enable bit (CRBE).

Offset: 0x010

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved						CRBE	TME
Type/Reset							RW 0	RW 0

Bits	Field	Descriptions
[1]	CRBE	Counter-Reload register Buffer Enable 0: Counter reload register can be updated immediately 1: Counter reload register can not be updated until the update event occurs
[0]	TME	Timer Enable bit 0: GPTM off 1: GPTM on – GPTM functions normally When the TME bit is cleared to 0, the counter is stopped and the GPTM consumes no power in any operation mode except for the single pulse mode and the slave trigger mode. In these two modes the TME bit can automatically be set to 1 by hardware which permits all the GPTM registers to function normally.

Channel 0 Input Configuration Register – CH0ICFR

This register specifies the channel 0 input mode configuration.

Offset: 0x020

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	TI0SRC	Reserved						
Type/Reset	RW 0							
	23	22	21	20	19	18	17	16
	Reserved				CH0PSC		CH0CCS	
Type/Reset					RW 0	RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved				TI0F			
Type/Reset					RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[31]	TI0SRC	Channel 0 Input Source TI0 Selection 0: The GT_CH0 pin is connected to channel 0 input TI0 1: The XOR operation output of the GT_CH0, GT_CH1, and GT_CH2 pins are connected to the channel 0 input TI0
[19:18]	CH0PSC	Channel 0 Capture Input Source Prescaler Setting These bits define the effective events of the channel 0 capture input. Note that the prescaler is reset once the Channel 0 Capture/Compare Enable bit, CH0E, in the Channel Control register named CHCTR is cleared to 0. 00: No prescaler, channel 0 capture input signal is chosen for each active event 01: Channel 0 Capture input signal is chosen for every 2 events 10: Channel 0 Capture input signal is chosen for every 4 events 11: Channel 0 Capture input signal is chosen for every 8 events
[17:16]	CH0CCS	Channel 0 Capture/Compare Selection 00: Channel 0 is configured as an output 01: Channel 0 is configured as an input derived from the TI0 signal 10: Channel 0 is configured as an input derived from the TI1 signal 11: Channel 0 is configured as an input which comes from the TRCED signal derived from the Trigger Controller Note: The CH0CCS field can be accessed only when the CH0E bit is cleared to 0.

Bits	Field	Descriptions
[3:0]	TI0F	Channel 0 Input Source TI0 Filter Setting These bits define the frequency divided ratio used to sample the TI0 signal. The Digital filter in the GPTM is an N-event counter where N is defined as how many valid transitions are necessary to output a filtered signal. 0000: No filter, the sampling clock is f_{SYSTEM}. 0001: $f_{SAMPLING} = f_{CLKIN}$, N = 2 0010: $f_{SAMPLING} = f_{CLKIN}$, N = 4 0011: $f_{SAMPLING} = f_{CLKIN}$, N = 8 0100: $f_{SAMPLING} = f_{DTS}$ / 2, N = 6 0101: $f_{SAMPLING} = f_{DTS}$ / 2, N = 8 0110: $f_{SAMPLING} = f_{DTS}$ / 4, N = 6 0111: $f_{SAMPLING} = f_{DTS}$ / 4, N = 8 1000: $f_{SAMPLING} = f_{DTS}$ / 8, N = 6 1001: $f_{SAMPLING} = f_{DTS}$ / 8, N = 8 1010: $f_{SAMPLING} = f_{DTS}$ / 16, N = 5 1011: $f_{SAMPLING} = f_{DTS}$ / 16, N = 6 1100: $f_{SAMPLING} = f_{DTS}$ / 16, N = 8 1101: $f_{SAMPLING} = f_{DTS}$ / 32, N = 5 1110: $f_{SAMPLING} = f_{DTS}$ / 32, N = 6 1111: $f_{SAMPLING} = f_{DTS}$ / 32, N = 8

Channel 1 Input Configuration Register – CH1ICFR

This register specifies the channel 1 input mode configuration.

Offset: 0x024

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved				CH1PSC		CH1CCS	
Type/Reset					RW 0	RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved				TI1F			
Type/Reset					RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[19:18]	CH1PSC	Channel 1 Capture Input Source Prescaler Setting These bits define the effective events of the channel 1 capture input. Note that the prescaler is reset once the Channel 1 Capture/Compare Enable bit, CH1E, in the Channel Control register named CHCTR is cleared to 0. 00: No prescaler, channel 1 capture input signal is chosen for each active event 01: Channel 1 Capture input signal is chosen for every 2 events 10: Channel 1 Capture input signal is chosen for every 4 events 11: Channel 1 Capture input signal is chosen for every 8 events

Bits	Field	Descriptions
[17:16]	CH1CCS	Channel 1 Capture/Compare Selection 00: Channel 1 is configured as an output 01: Channel 1 is configured as an input derived from the TI1 signal 10: Channel 1 is configured as an input derived from the TI0 signal 11: Channel 1 is configured as an input which comes from the TRCED signal derived from the Trigger Controller Note: The CH1CCS field can be accessed only when the CH1E bit is cleared to 0.
[3:0]	TI1F	Channel 1 Input Source TI1 Filter Setting These bits define the frequency divided ratio used to sample the TI1 signal. The Digital filter in the GPTM is an N-event counter where N is defined as how many valid transitions are necessary to output a filtered signal. 0000: No filter, the sampling clock is f_{SYSTEM}. 0001: $f_{SAMPLING} = f_{CLKIN}$, N = 2 0010: $f_{SAMPLING} = f_{CLKIN}$, N = 4 0011: $f_{SAMPLING} = f_{CLKIN}$, N = 8 0100: $f_{SAMPLING} = f_{DTS} / 2$, N = 6 0101: $f_{SAMPLING} = f_{DTS} / 2$, N = 8 0110: $f_{SAMPLING} = f_{DTS} / 4$, N = 6 0111: $f_{SAMPLING} = f_{DTS} / 4$, N = 8 1000: $f_{SAMPLING} = f_{DTS} / 8$, N = 6 1001: $f_{SAMPLING} = f_{DTS} / 8$, N = 8 1010: $f_{SAMPLING} = f_{DTS} / 16$, N = 5 1011: $f_{SAMPLING} = f_{DTS} / 16$, N = 6 1100: $f_{SAMPLING} = f_{DTS} / 16$, N = 8 1101: $f_{SAMPLING} = f_{DTS} / 32$, N = 5 1110: $f_{SAMPLING} = f_{DTS} / 32$, N = 6 1111: $f_{SAMPLING} = f_{DTS} / 32$, N = 8

Channel 2 Input Configuration Register – CH2ICFR

This register specifies the channel 2 input mode configuration.

Offset: 0x028

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved				CH2PSC		CH2CCS	
Type/Reset					RW 0	RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved				TI2F			
Type/Reset					RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[19:18]	CH2PSC	Channel 2 Capture Input Source Prescaler Setting These bits define the effective events of the channel 2 capture input. Note that the prescaler is reset once the Channel 2 Capture/Compare Enable bit, CH2E, in the Channel Control register named CHCTR is cleared to 0. 00: No prescaler, channel 2 capture input signal is chosen for each active event 01: Channel 2 Capture input signal is chosen for every 2 events 10: Channel 2 Capture input signal is chosen for every 4 events 11: Channel 2 Capture input signal is chosen for every 8 events
[17:16]	CH2CCS	Channel 2 Capture/Compare Selection 00: Channel 2 is configured as an output 01: Channel 2 is configured as an input derived from the TI2 signal 10: Channel 2 is configured as an input derived from the TI3 signal 11: Channel 2 is configured as an input which comes from the TRCED signal derived from the Trigger Controller Note: The CH2CCS field can be accessed only when the CH2E bit is cleared to 0.

Bits	Field	Descriptions
[3:0]	TI2F	Channel 2 Input Source TI2 Filter Setting These bits define the frequency divided ratio used to sample the TI2 signal. The Digital filter in the GPTM is an N-event counter where N is defined as how many valid transitions are necessary to output a filtered signal. 0000: No filter, the sampling clock is f_{SYSTEM}. 0001: $f_{SAMPLING} = f_{CLKIN}$, N = 2 0010: $f_{SAMPLING} = f_{CLKIN}$, N = 4 0011: $f_{SAMPLING} = f_{CLKIN}$, N = 8 0100: $f_{SAMPLING} = f_{DTS}$ / 2, N = 6 0101: $f_{SAMPLING} = f_{DTS}$ / 2, N = 8 0110: $f_{SAMPLING} = f_{DTS}$ / 4, N = 6 0111: $f_{SAMPLING} = f_{DTS}$ / 4, N = 8 1000: $f_{SAMPLING} = f_{DTS}$ / 8, N = 6 1001: $f_{SAMPLING} = f_{DTS}$ / 8, N = 8 1010: $f_{SAMPLING} = f_{DTS}$ / 16, N = 5 1011: $f_{SAMPLING} = f_{DTS}$ / 16, N = 6 1100: $f_{SAMPLING} = f_{DTS}$ / 16, N = 8 1101: $f_{SAMPLING} = f_{DTS}$ / 32, N = 5 1110: $f_{SAMPLING} = f_{DTS}$ / 32, N = 6 1111: $f_{SAMPLING} = f_{DTS}$ / 32, N = 8

Channel 3 Input Configuration Register – CH3ICFR

This register specifies the channel 3 input mode configuration.

Offset: 0x02C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved				CH3PSC		CH3CCS	
Type/Reset					RW 0	RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved				TI3F			
Type/Reset					RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[19:18]	CH3PSC	Channel 3 Capture Input Source Prescaler Setting These bits define the effective events of the channel 3 capture input. Note that the prescaler is reset once the Channel 3 Capture/Compare Enable bit, CH3E, in the Channel Control register named CHCTR is cleared to 0. 00: No prescaler, channel 3 capture input signal is chosen for each active event 01: Channel 3 Capture input signal is chosen for every 2 events 10: Channel 3 Capture input signal is chosen for every 4 events 11: Channel 3 Capture input signal is chosen for every 8 events

Bits	Field	Descriptions
[17:16]	CH3CCS	Channel 3 Capture/Compare Selection 00: Channel 3 is configured as an output 01: Channel 3 is configured as an input derived from the TI3 signal 10: Channel 3 is configured as an input derived from the TI2 signal 11: Channel 3 is configured as an input which comes from the TRCED signal derived from the Trigger Controller Note: The CH3CCS field can be accessed only when the CH3E bit is cleared to 0.
[3:0]	TI3F	Channel 3 Input Source TI3 Filter Setting These bits define the frequency divided ratio used to sample the TI3 signal. The Digital filter in the GPTM is an N-event counter where N is defined as how many valid transitions are necessary to output a filtered signal. 0000: No filter, the sampling clock is f_{SYSTEM}. 0001: $f_{SAMPLING} = f_{CLKIN}$, N = 2 0010: $f_{SAMPLING} = f_{CLKIN}$, N = 4 0011: $f_{SAMPLING} = f_{CLKIN}$, N = 8 0100: $f_{SAMPLING} = f_{DTS}$ / 2, N = 6 0101: $f_{SAMPLING} = f_{DTS}$ / 2, N = 8 0110: $f_{SAMPLING} = f_{DTS}$ / 4, N = 6 0111: $f_{SAMPLING} = f_{DTS}$ / 4, N = 8 1000: $f_{SAMPLING} = f_{DTS}$ / 8, N = 6 1001: $f_{SAMPLING} = f_{DTS}$ / 8, N = 8 1010: $f_{SAMPLING} = f_{DTS}$ / 16, N = 5 1011: $f_{SAMPLING} = f_{DTS}$ / 16, N = 6 1100: $f_{SAMPLING} = f_{DTS}$ / 16, N = 8 1101: $f_{SAMPLING} = f_{DTS}$ / 32, N = 5 1110: $f_{SAMPLING} = f_{DTS}$ / 32, N = 6 1111: $f_{SAMPLING} = f_{DTS}$ / 32, N = 8

Channel 0 Output Configuration Register – CH0OCFR

This register specifies the channel 0 output mode configuration.

Offset: 0x040

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							CH0OM[3]
Type/Reset								RW 0
	7	6	5	4	3	2	1	0
		Reserved	CH0IMAE	CH0PRE	Reserved	CH0OM[2:0]		
Type/Reset			RW 0	RW 0		RW 0	RW 0	RW 0

Bits	Field	Descriptions
[5]	CH0IMAE	Channel 0 Immediate Active Enable 0: No action 1: Single pulse Immediate Active Mode is enabled The CH0OREF will be forced to the compare matched level immediately after an available trigger event occurs irrespective of the result of the comparison between the CNTR and the CH0CCR values. The effective duration ends automatically at the next overflow or underflow event. Note: The CH0IMAE bit is available only if the channel 0 is configured to be operated in the PWM mode 1 or the PWM mode 2.
[4]	CH0PRE	Channel 0 Capture/Compare Register (CH0CCR) Preload Enable 0: CH0CCR preload function is disabled. The CH0CCR register can be immediately assigned a new value when the CH0PRE bit is cleared to 0 and the updated CH0CCR value is used immediately. 1: CH0CCR preload function is enabled. The new CH0CCR value will not be transferred to its shadow register until the update event occurs.

Bits	Field	Descriptions
[8][2:0]	CH0OM[3:0]	Channel 0 Output Mode Setting These bits define the functional types of the output reference signal CH0OREF. 0000: No Change 0001: Output 0 on compare match 0010: Output 1 on compare match 0011: Output toggles on compare match 0100: Force inactive – CH0OREF is forced to 0 0101: Force active – CH0OREF is forced to 1 0110: PWM mode 1 - During up-counting, channel 0 has an active level when CNTR < CH0CCR or otherwise has an inactive level. - During down-counting, channel 0 has an inactive level when CNTR > CH0CCR or otherwise has an active level. 0111: PWM mode 2 - During up-counting, channel 0 is has an inactive level when CNTR < CH0CCR or otherwise has an active level. - During down-counting, channel 0 has an active level when CNTR > CH0CCR or otherwise has an inactive level. 1110: Asymmetric PWM mode 1 - During up-counting, channel 0 has an active level when CNTR < CH0CCR or otherwise has an inactive level. - During down-counting, channel 0 has an inactive level when CNTR > CH0ACR or otherwise has an active level. 1111: Asymmetric PWM mode 2 - During up-counting, channel 0 has an inactive level when CNTR < CH0CCR or otherwise has an active level. - During down-counting, channel 0 has an active level when CNTR > CH0ACR or otherwise has an inactive level Note: When channel 0 is used as asymmetric PWM output mode, the Counter Mode Selection bit in Counter Configuration Register must be configured as Center-aligned Counting mode (CMSEL = 01/02/03)

Channel 1 Output Configuration Register – CH1OCFR

This register specifies the channel 1 output mode configuration.

Offset: 0x044

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							CH1OM[3]
Type/Reset								RW 0
	7	6	5	4	3	2	1	0
		Reserved	CH1IMAE	CH1PRE	Reserved	CH1OM[2:0]		
Type/Reset			RW 0	RW 0		RW 0	RW 0	RW 0

Bits	Field	Descriptions
[5]	CH1IMAE	Channel 1 Immediate Active Enable 0: No action 1: Single pulse Immediate Active Mode is enabled The CH1OREF will be forced to the compare matched level immediately after an available trigger event occurs irrespective of the result of the comparison between the CNTR and the CH1CCR values. The effective duration ends automatically at the next overflow or underflow event. Note: The CH1IMAE bit is available only if the channel 1 is configured to be operated in the PWM mode 1 or the PWM mode 2.
[4]	CH1PRE	Channel 1 Capture/Compare Register (CH1CCR) Preload Enable 0: CH1CCR preload function is disabled. The CH1CCR register can be immediately assigned a new value when the CH1PRE bit is cleared to 0 and the updated CH1CCR value is used immediately. 1: CH1CCR preload function is enabled The new CH1CCR value will not be transferred to its shadow register until the update event occurs.

Bits	Field	Descriptions
[8][2:0]	CH1OM[3:0]	Channel 1 Output Mode Setting These bits define the functional types of the output reference signal CH1OREF. 0000: No Change 0001: Output 0 on compare match 0010: Output 1 on compare match 0011: Output toggles on compare match 0100: Force inactive – CH1OREF is forced to 0 0101: Force active – CH1OREF is forced to 1 0110: PWM mode 1 - During up-counting, channel 1 has an active level when CNTR < CH1CCR or otherwise has an inactive level. - During down-counting, channel 1 has an inactive level when CNTR > CH1CCR or otherwise has an active level. 0111: PWM mode 2 - During up-counting, channel 1 has an inactive level when CNTR < CH1CCR or otherwise has an active level. - During down-counting, channel 1 has an active level when CNTR > CH1CCR or otherwise has an inactive level. 1110: Asymmetric PWM mode 1 - During up-counting, channel 1 has an active level when CNTR < CH1CCR or otherwise has an inactive level. - During down-counting, channel 1 has an inactive level when CNTR > CH1ACR or otherwise has an active level. 1111: Asymmetric PWM mode 2 - During up-counting, channel 1 has an inactive level when CNTR < CH1CCR or otherwise has an active level. - During down-counting, channel 1 has an active level when CNTR > CH1ACR or otherwise has an inactive level Note: When channel 1 is used as asymmetric PWM output mode, the Counter Mode Selection bit in Counter Configuration Register must be configured as Center-aligned Counting mode (CMSEL = 01/02/03)

Channel 2 Output Configuration Register – CH2OCFR

This register specifies the channel 2 output mode configuration.

Offset: 0x048

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							CH2OM[3]
Type/Reset								RW 0
	7	6	5	4	3	2	1	0
		Reserved	CH2IMAE	CH2PRE	Reserved	CH2OM[2:0]		
Type/Reset			RW 0	RW 0		RW 0	RW 0	RW 0

Bits	Field	Descriptions
[5]	CH2IMAE	Channel 2 Immediate Active Enable 0: No action 1: Single pulse Immediate Active Mode is enabled The CH2OREF will be forced to the compare matched level immediately after an available trigger event occurs irrespective of the result of the comparison between the CNTR and the CH2CCR values. The effective duration ends automatically at the next overflow or underflow event. Note: The CH2IMAE bit is available only if the channel 2 is configured to be operated in the PWM mode 1 or the PWM mode 2.
[4]	CH2PRE	Channel 2 Capture/Compare Register (CH2CCR) Preload Enable 0: CH2CCR preload function is disabled. The CH2CCR register can be immediately assigned a new value when the CH2PRE bit is cleared to 0 and the updated CH2CCR value is used immediately. 1: CH2CCR preload function is enabled The new CH2CCR value will not be transferred to its shadow register until the update event occurs.
[8][2:0]	CH2OM[3:0]	Channel 2 Output Mode Setting These bits define the functional types of the output reference signal CH2OREF. 0000: No Change 0001: Output 0 on compare match 0010: Output 1 on compare match 0011: Output toggles on compare match 0100: Force inactive – CH2OREF is forced to 0 0101: Force active – CH2OREF is forced to 1 0110: PWM mode 1 - During up-counting, channel 2 has an active level when CNTR < CH2CCR or otherwise has an inactive level. - During down-counting, channel 2 has an inactive level when CNTR > CH2CCR or otherwise has an active level. 0111: PWM mode 2 - During up-counting, channel 2 has an inactive level when CNTR < CH2CCR or otherwise has an active level. - During down-counting, channel 2 has an active level when CNTR > CH2CCR or otherwise has an inactive level. 1110: Asymmetric PWM mode 1 - During up-counting, channel 2 has an active level when CNTR < CH2CCR or otherwise has an inactive level. - During down-counting, channel 2 has an inactive level when CNTR > CH2ACR or otherwise has an active level. 1111: Asymmetric PWM mode 2 - During up-counting, channel 2 has an inactive level when CNTR < CH2CCR or otherwise has an active level. - During down-counting, channel 2 has an active level when CNTR > CH2ACR or otherwise has an inactive level Note: When channel 2 is used as asymmetric PWM output mode, the Counter Mode Selection bit in Counter Configuration Register must be configured as Center-aligned Counting mode (CMSEL = 01/02/03)

Channel 3 Output Configuration Register – CH3OCFR

This register specifies the channel 3 output mode configuration.

Offset: 0x04C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							CH3OM[3]
Type/Reset								RW 0
	7	6	5	4	3	2	1	0
		Reserved	CH3IMAE	CH3PRE	Reserved	CH3OM[2:0]		
Type/Reset			RW 0	RW 0		RW 0	RW 0	RW 0

Bits	Field	Descriptions
[5]	CH3IMAE	Channel 3 Immediate Active Enable 0: No action 1: Single pulse Immediate Active Mode is enabled The CH3OREF will be forced to the compare matched level immediately after an available trigger event occurs irrespective of the result of the comparison between the CNTR and the CH3CCR values. The effective duration ends automatically at the next overflow or underflow event. Note: The CH3IMAE bit is available only if the channel 3 is configured to be operated in the PWM mode 1 or the PWM mode 2.
[4]	CH3PRE	Channel 3 Capture/Compare Register (CH3CCR) Preload Enable 0: CH3CCR preload function is disabled. The CH3CCR register can be immediately assigned a new value when the CH3PRE bit is cleared to 0 and the updated CH3CCR value is used immediately. 1: CH3CCR preload function is enabled The new CH3CCR value will not be transferred to its shadow register until the update event occurs.

Bits	Field	Descriptions
[8][2:0]	CH3OM[3:0]	Channel 3 Output Mode Setting These bits define the functional types of the output reference signal CH3OREF 0000: No Change 0001: Output 0 on compare match 0010: Output 1 on compare match 0011: Output toggles on compare match 0100: Force inactive – CH3OREF is forced to 0 0101: Force active – CH3OREF is forced to 1 0110: PWM mode 1 - During up-counting, channel 3 has an active level when CNTR < CH3CCR or otherwise has an inactive level. - During down-counting, channel 3 has an inactive level when CNTR > CH3CCR or otherwise has an active level. 0111: PWM mode 2 - During up-counting, channel 3 has an inactive level when CNTR < CH3CCR or otherwise has an active level. - During down-counting, channel 3 has an active level when CNTR > CH3CCR or otherwise has an inactive level 1110: Asymmetric PWM mode 1 - During up-counting, channel 3 has an active level when CNTR < CH3CCR or otherwise has an inactive level. - During down-counting, channel 3 has an inactive level when CNTR > CH3ACR or otherwise has an active level. 1111: Asymmetric PWM mode 2 - During up-counting, channel 3 has an inactive level when CNTR < CH3CCR or otherwise has an active level. - During down-counting, channel 3 has an active level when CNTR > CH3ACR or otherwise has an inactive level Note: When channel 3 is used as asymmetric PWM output mode, the Counter Mode Selection bit in Counter Configuration Register must be configured as Center-aligned Counting mode (CMSEL = 01/02/03)

Channel Control Register – CHCTR

This register contains the channel capture input or compare output function enable control bits.

Offset: 0x050

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								

	7	6	5	4	3	2	1	0
	Reserved	CH3E	Reserved	CH2E	Reserved	CH1E	Reserved	CH0E
Type/Reset		RW 0		RW 0		RW 0		RW 0

Bits	Field	Descriptions
[6]	CH3E	Channel 3 Capture/Compare Enable - Channel 3 is configured as an input (CH3CCS = 0x01/0x02/0x03) 0: Input Capture Mode is disabled 1: Input Capture Mode is enabled - Channel 3 is configured as an output (CH3CCS = 0x00) 0: Off – Channel 3 output signal CH3O is not active 1: On – Channel 3 output signal CH3O generated on the corresponding output pin
[4]	CH2E	Channel 2 Capture/Compare Enable - Channel 2 is configured as an input (CH2CCS = 0x01/0x02/0x03) 0: Input Capture Mode is disabled 1: Input Capture Mode is enabled - Channel 2 is configured as an output (CH2CCS = 0x00) 0: Off – Channel 2 output signal CH2O is not active 1: On – Channel 2 output signal CH2O generated on the corresponding output pin
[2]	CH1E	Channel 1 Capture/Compare Enable - Channel 1 is configured as an input (CH1CCS = 0x01/0x02/0x03) 0: Input Capture Mode is disabled 1: Input Capture Mode is enabled - Channel 1 is configured as an output (CH1CCS = 0x00) 0: Off – Channel 1 output signal CH1O is not active 1: On – Channel 1 output signal CH1O generated on the corresponding output pin
[0]	CH0E	Channel 0 Capture/Compare Enable - Channel 0 is configured as an input (CH0CCS = 0x01/0x02/0x03) 0: Input Capture Mode is disabled 1: Input Capture Mode is enabled - Channel 0 is configured as an output (CH0CCS = 0x00) 0: Off – Channel 0 output signal CH0O is not active 1: On – Channel 0 output signal CH0O generated on the corresponding output pin

Channel Polarity Configuration Register – CHPOLR

This register contains the channel capture input or compare output polarity control.

Offset: 0x054

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved	CH3P	Reserved	CH2P	Reserved	CH1P	Reserved	CH0P
Type/Reset		RW 0		RW 0		RW 0		RW 0

Bits	Field	Descriptions
[6]	CH3P	Channel 3 Capture/Compare Polarity - When Channel 3 is configured as an input (CH3CCS=0x01/0x02/0x03) 0: capture event occurs on a Channel 3 rising edge 1: capture event occurs on a Channel 3 falling edge - When Channel 3 is configured as an output (CH3CCS = 0x00) 0: Channel 3 Output is active high 1: Channel 3 Output is active low
[4]	CH2P	Channel 2 Capture/Compare Polarity (CH2CCS=0x01/0x02/0x03) - When Channel 2 is configured as an input 0: capture event occurs on a Channel 2 rising edge 1: capture event occurs on a Channel 2 falling edge - When Channel 2 is configured as an output (CH2CCS = 0x00) 0: Channel 2 Output is active high 1: Channel 2 Output is active low
[2]	CH1P	Channel 1 Capture/Compare Polarity - When Channel 1 is configured as an input (CH1CCS=0x01/0x02/0x03) 0: capture event occurs on a Channel 1 rising edge 1: capture event occurs on a Channel 1 falling edge - Channel 1 is configured as an output (CH1CCS = 0x00) 0: Channel 1 Output is active high 1: Channel 1 Output is active low
[0]	CH0P	Channel 0 Capture/Compare Polarity - When Channel 0 is configured as an input (CH0CCS=0x01/0x02/0x03) 0: capture event occurs on a Channel 0 rising edge 1: capture event occurs on a Channel 0 falling edge - When Channel 0 is configured as an output (CH0CCS = 0x00) 0: Channel 0 Output is active high 1: Channel 0 Output is active low

Timer Interrupt Control Register – DICTR

This register contains the timer interrupt enable control bits.

Offset: 0x074

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved					TEVIE	Reserved	UEVIE
Type/Reset						RW 0		RW 0
	7	6	5	4	3	2	1	0
	Reserved				CH3CCIE	CH2CCIE	CH1CCIE	CH0CCIE
Type/Reset					RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[10]	TEVIE	Trigger event Interrupt Enable 0: Trigger event interrupt is disabled 1: Trigger event interrupt is enabled
[8]	UEVIE	Update event Interrupt Enable 0: Update event interrupt is disabled 1: Update event interrupt is enabled
[3]	CH3CCIE	Channel 3 Capture/Compare Interrupt Enable 0: Channel 3 interrupt is disabled 1: Channel 3 interrupt is enabled
[2]	CH2CCIE	Channel 2 Capture/Compare Interrupt Enable 0: Channel 2 interrupt is disabled 1: Channel 2 interrupt is enabled
[1]	CH1CCIE	Channel 1 Capture/Compare Interrupt Enable 0: Channel 1 interrupt is disabled 1: Channel 1 interrupt is enabled
[0]	CH0CCIE	Channel 0 Capture/Compare Interrupt Enable 0: Channel 0 interrupt is disabled 1: Channel 0 interrupt is enabled

Timer Event Generator Register – EVGR

This register contains the software event generation bits.

Offset: 0x078

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved					TEVG	Reserved	UEVG
Type/Reset						WO 0		WO 0
	7	6	5	4	3	2	1	0
	Reserved				CH3CCG	CH2CCG	CH1CCG	CH0CCG
Type/Reset					WO 0	WO 0	WO 0	WO 0

Bits	Field	Descriptions
[10]	TEVG	Trigger Event Generation The trigger event TEV can be generated by setting this bit. It is cleared by hardware automatically. 0: No action 1: TEVIF flag is set
[8]	UEVG	Update Event Generation The update event UEV can be generated by setting this bit. It is cleared by hardware automatically. 0: No action 1: Reinitialize the counter The counter value returns to 0 or the CRR preload value, depending on the counter mode in which the current timer is being used. An update operation of any related registers will also be performed. For more detail descriptions, refer to the corresponding section.
[3]	CH3CCG	Channel 3 Capture/Compare Generation A Channel 3 capture/compare event can be generated by setting this bit. It is cleared by hardware automatically. 0: No action 1: Capture/compare event is generated on channel 3 If Channel 3 is configured as an input, the counter value is captured into the CH3CCR register and then the CH3CCIF bit is set. If Channel 3 is configured as an output, the CH3CCIF bit is set.
[2]	CH2CCG	Channel 2 Capture/Compare Generation A Channel 2 capture/compare event can be generated by setting this bit. It is cleared by hardware automatically. 0: No action 1: Capture/compare event is generated on channel 2 If Channel 2 is configured as an input, the counter value is captured into the CH2CCR register and then the CH2CCIF bit is set. If Channel 2 is configured as an output, the CH2CCIF bit is set.

Bits	Field	Descriptions
[1]	CH1CCG	Channel 1 Capture/Compare Generation A Channel 1 capture/compare event can be generated by setting this bit. It is cleared by hardware automatically. 0: No action 1: Capture/compare event is generated on channel 1 If Channel 1 is configured as an input, the counter value is captured into the CH1CCR register and then the CH1CCIF bit is set. If Channel 1 is configured as an output, the CH1CCIF bit is set.
[0]	CH0CCG	Channel 0 Capture/Compare Generation A Channel 0 capture/compare event can be generated by setting this bit. It is cleared by hardware automatically. 0: No action 1: Capture/compare event is generated on channel 0 If Channel 0 is configured as an input, the counter value is captured into the CH0CCR register and then the CH0CCIF bit is set. If Channel 0 is configured as an output, the CH0CCIF bit is set.

Timer Interrupt Status Register – INTSR

This register stores the timer interrupt status.

Offset: 0x07C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved					TEVIF	Reserved	UEVIF
Type/Reset						W0C 0		W0C 0
	7	6	5	4	3	2	1	0
	CH3OCF	CH2OCF	CH1OCF	CH0OCF	CH3CCIF	CH2CCIF	CH1CCIF	CH0CCIF
Type/Reset	W0C 0	W0C 0	W0C 0	W0C 0	W0C 0	W0C 0	W0C 0	W0C 0

Bits	Field	Descriptions
[10]	TEVIF	Trigger Event Interrupt Flag This flag is set by hardware on a trigger event and is cleared by software. 0: No trigger event occurs 1: Trigger event occurs

Bits	Field	Descriptions
[8]	UEVIF	Update Event Interrupt Flag. This bit is set by hardware on an update event and is cleared by software. 0: No update event occurs 1: Update event occurs Note: The update event is derived from the following conditions: - The counter overflows or underflows - The UEVG bit is asserted - A restart trigger event occurs from the slave trigger input
[7]	CH3OCF	Channel 3 Over-Capture Flag This flag is set by hardware and cleared by software. 0: No over-capture event is detected 1: Capture event occurs again when the CH3CCIF bit is already set and it is not yet cleared by software
[6]	CH2OCF	Channel 2 Over-Capture Flag This flag is set by hardware and cleared by software. 0: No over-capture event is detected 1: Capture event occurs again when the CH2CCIF bit is already set and it is not cleared yet by software
[5]	CH1OCF	Channel 1 Over-Capture Flag This flag is set by hardware and cleared by software. 0: No over-capture event is detected 1: Capture event occurs again when the CH1CCIF bit is already set and it is not cleared yet by software.
[4]	CH0OCF	Channel 0 Over-Capture Flag This flag is set by hardware and cleared by software. 0: No over-capture event is detected 1: Capture event occurs again when the CH0CCIFbit is already set and it is not yet cleared by software.
[3]	CH3CCIF	Channel 3 Capture/Compare Interrupt Flag - Channel 3 is configured as an output: 0: No match event occurs 1: The contents of the counter CNTR have matched the contents of the CH3CCR register. This flag is set by hardware when the counter value matches the CH3CCR value except in the center-aligned mode. It is cleared by software. - Channel 3 is configured as an input: 0: No input capture occurs 1: Input capture occurs This bit is set by hardware on a capture event. It is cleared by software or by reading the CH3CCR register.
[2]	CH2CCIF	Channel 2 Capture/Compare Interrupt Flag - Channel 2 is configured as an output: 0: No match event occurs 1: The contents of the counter CNTR have matched the contents of the CH2CCR register This flag is set by hardware when the counter value matches the CH2CCR value except in the center-aligned mode. It is cleared by software. - Channel 2 is configured as an input: 0: No input capture occurs 1: Input capture occurs. This bit is set by hardware on a capture event. It is cleared by software or by reading the CH2CCR register.

Bits	Field	Descriptions
[1]	CH1CCIF	Channel 1 Capture/Compare Interrupt Flag - Channel 1 is configured as an output: 0: No match event occurs 1: The contents of the counter CNTR have matched the contents of the CH1CCR register This flag is set by hardware when the counter value matches the CH1CCR value except in the center-aligned mode. It is cleared by software. - Channel 1 is configured as an input: 0: No input capture occurs 1: Input capture occurs This bit is set by hardware on a capture event. It is cleared by software or by reading the CH1CCR register.
[0]	CH0CCIF	Channel 0 Capture/Compare Interrupt Flag - Channel 0 is configured as an output: 0: No match event occurs 1: The contents of the counter CNTR have matched the content of the CH0CCR register This flag is set by hardware when the counter value matches the CH0CCR value except in the center-aligned mode. It is cleared by software. - Channel 0 is configured as an input: 0: No input capture occurs 1: Input capture occurs This bit is set by hardware on a capture event. It is cleared by software or by reading the CH0CCR register.

Timer Counter Register – CNTR

This register stores the timer counter value.

Offset: 0x080

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	CNTV							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	CNTV							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	CNTV	Counter Value.

Timer Prescaler Register – PSCR

This register specifies the timer prescaler value to generate the counter clock.

Offset: 0x084

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	PSCV							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	PSCV							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	PSCV	Prescaler Value These bits are used to specify the prescaler value to generate the counter clock frequency f_{CK_CNT}. $f_{CK\_CNT} = \frac{f_{CK\_PSC}}{PSCV[15:0] + 1}$, where the f_{CK_PSC} is the prescaler clock source.

Timer Counter Reload Register – CRR

This register specifies the timer counter reload value.

Offset: 0x088

Reset value: 0x0000_FFFF

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	CRV							
Type/Reset	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1
	7	6	5	4	3	2	1	0
	CRV							
Type/Reset	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1

Bits	Field	Descriptions
[15:0]	CRV	Counter Reload Value The CRV is the reload value which is loaded into the actual counter register.

Channel 0 Capture/Compare Register – CH0CCR

This register specifies the timer channel 0 capture/compare value.

Offset: 0x090

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	CH0CCV							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	CH0CCV							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	CH0CCV	Channel 0 Capture/Compare Value - When Channel 0 is configured as an output The CH0CCR value is compared with the counter value and the comparison result is used to trigger the CH0OREF output signal. - When Channel 0 is configured as an input The CH0CCR register stores the counter value captured by the last channel 0 capture event.

Channel 1 Capture/Compare Register – CH1CCR

This register specifies the timer channel 1 capture/compare value.

Offset: 0x094

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	CH1CCV							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	CH1CCV							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	CH1CCV	Channel 1 Capture/Compare Value - When Channel 1 is configured as an output The CH1CCR value is compared with the counter value and the comparison result is used to trigger the CH1OREF output signal. - When Channel 1 is configured as an input The CH1CCR register stores the counter value captured by the last channel 1 capture event.

Channel 2 Capture/Compare Register – CH2CCR

This register specifies the timer channel 2 capture/compare value.

Offset: 0x098

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	CH2CCV							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	CH2CCV							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	CH2CCV	Channel 2 Capture/Compare Value - When Channel 2 is configured as an output The CH2CCR value is compared with the counter value and the comparison result is used to trigger the CH2OREF output signal. - When Channel 2 is configured as an input The CH2CCR register stores the counter value captured by the last channel 2 capture event.

Channel 3 Capture/Compare Register – CH3CCR

This register specifies the timer channel 3 capture/compare value.

Offset: 0x09C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	CH3CCV							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	CH3CCV							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	CH3CCV	Channel 3 Capture/Compare Value - When Channel 3 is configured as an output The CH3CCR value is compared with the counter value and the comparison result is used to trigger the CH3OREF output signal. - When Channel 3 is configured as an input The CH3CCR register stores the counter value captured by the last channel 3 capture event.

Channel 0 Asymmetric Compare Register – CH0ACR

This register specifies the timer channel 0 asymmetric compare value.

Offset: 0x0A0

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	CH0ACV							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	CH0ACV							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	CH0ACV	Channel 0 Asymmetric Compare Value When channel 0 is configured as asymmetric PWM mode and the counter is counting down, the value written into this register will be compared to the counter.

Channel 1 Asymmetric Compare Register – CH1ACR

This register specifies the timer channel 1 asymmetric compare value.

Offset: 0x0A4

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	CH1ACV							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	CH1ACV							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	CH1ACV	Channel 1 Asymmetric Compare Value When channel 1 is configured as asymmetric PWM mode and the counter is counting down, the value written into this register will be compared to the counter.

Channel 2 Asymmetric Compare Register – CH2ACR

This register specifies the timer channel 2 asymmetric compare value.

Offset: 0x0A8

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	CH2ACV							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	CH2ACV							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	CH2ACV	Channel 2 Asymmetric Compare Value When channel 2 is configured as asymmetric PWM mode and the counter is counting down, the value written into this register will be compared to the counter.

Channel 3 Asymmetric Compare Register – CH3ACR

This register specifies the timer channel 3 asymmetric compare value.

Offset: 0x0AC

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	CH3ACV							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	CH3ACV							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	CH3ACV	Channel 3 Asymmetric Compare Value When channel 3 is configured as asymmetric PWM mode and the counter is counting down, the value written into this register will be compared to the counter.

14 Basic Function Timer (BFTM)

Introduction

The Basic Function Timer Module, BFTM, is a 32-bit up-counting counter designed to measure time intervals, generate one shot pulses or generate repetitive interrupts. The BFTM can operate in two modes which are repetitive and one shot modes. The repetitive mode restarts the counter at each compare match event which is generated by the internal comparator. The BFTM also supports a one shot mode which will force the counter to stop counting when a compare match event occurs.

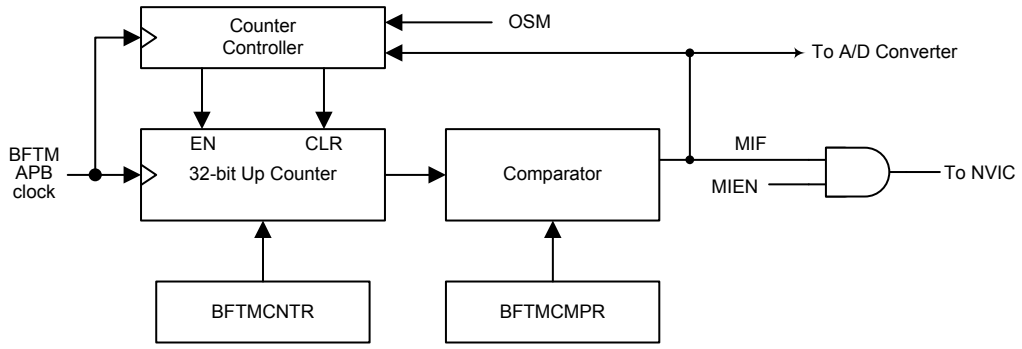


Figure 59. BFTM Block Diagram

Features

- 32-bit up-counting counter
- Compare Match function
- Includes debug mode
- Clock source: BFTM APB clock
- Counter value can be R/W on the fly
- One shot mode: counter stops counting when compare match occurs
- Repetitive mode: counter restarts when compare match occurs
- Compare Match interrupt enable/disable control

Functional Description

The BFTM is a 32-bit up-counting counter which is driven by the BFTM APB clock, PCLK. The counter value can be changed or read at any time even when the timer is counting. The BFTM supports two operating modes known as the repetitive mode and one shot mode allowing the measurement of time intervals or the generation of periodic time durations.

Repetitive Mode

The BFTM counts up from zero to a specific compare value which is pre-defined by the BFTMCMPR register. When the BFTM operates in the repetitive mode and the counter reaches a value equal to the specific compare value in the BFTMCMPR register, the timer will generate a compare match event signal, MIF. When this occurs, the counter will be reset to 0 and resume its counting operation. When the MIF signal is generated, a BFTM compare match interrupt will also be generated periodically if the compare match interrupt is enabled by setting the corresponding interrupt control bit, MIEN, to 1. The counter value will remain unchanged and the counter will stop counting if it is disabled by clearing the CEN bit to 0.

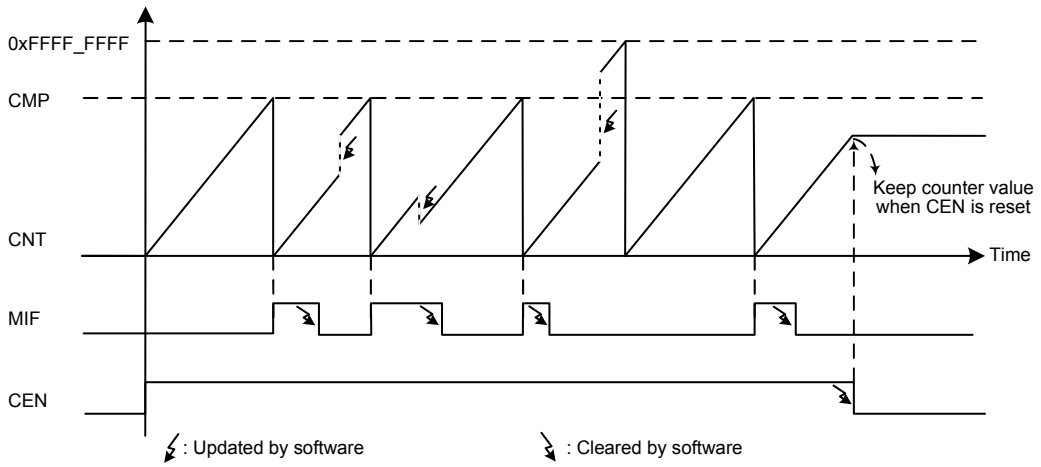


Figure 60. BFTM – Repetitive Mode

One Shot Mode

By setting the OSM bit in BFTMCR register to 1, the BFTM will operate in the one shot mode. The BFTM starts to count when the CEN bit is set to 1 by the application program. The counter value will remain unchanged if the CEN bit is cleared to 0 by the application program. However, the counter value will be reset to 0 and stop counting when the CEN bit is cleared automatically to 0 by the internal hardware when a counter compare match event occurs.

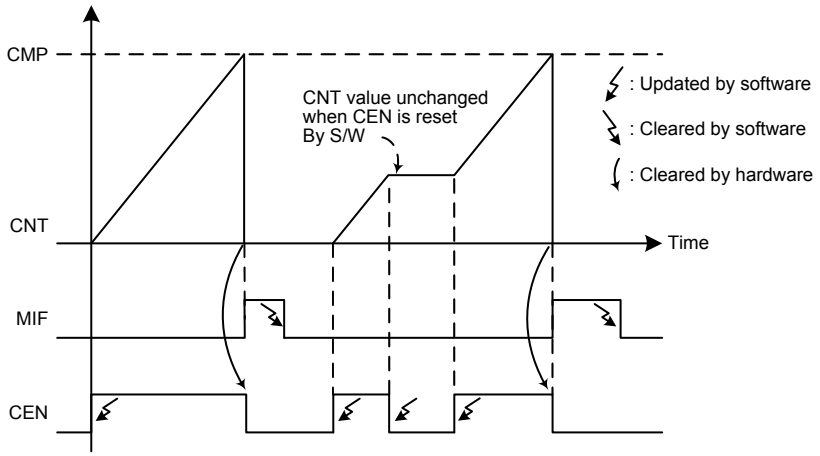


Figure 61. BFTM – One Shot Mode

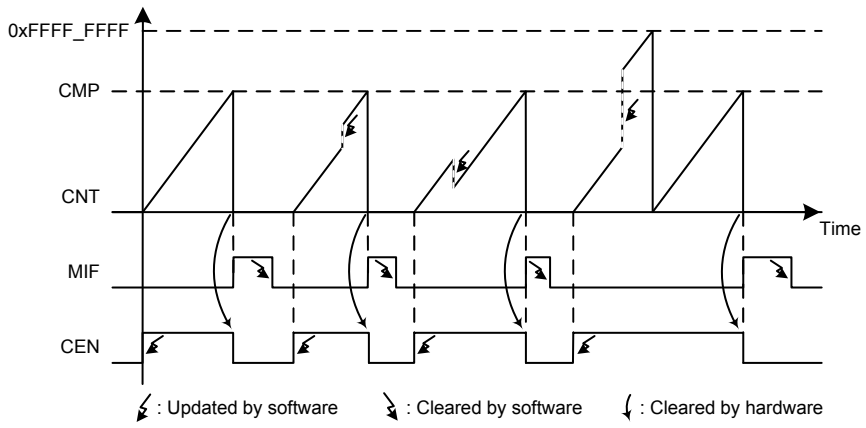


Figure 62. BFTM – One Shot Mode Counter Updating

Trigger ADC Start

When a BFTM compare match event occurs, a compare match interrupt flag, MIF, will be generated which can be used as an A/D Converter input trigger source.

Register Map

The following table shows the BFTM registers and their reset values.

Table 33. BFTM Register Map

Register	Offset	Description	Reset Value
BFTMCR	0x000	BFTM Control Register	0x0000_0000
BFTMSR	0x004	BFTM Status Register	0x0000_0000
BFTMCNTR	0x008	BFTM Counter Value Register	0x0000_0000
BFTMCMPR	0x00C	BFTM Compare Value Register	0xFFFF_FFFF

Register Descriptions

BFTM Control Register – BFTMCR

This register specifies the overall BFTM control bits.

Offset: 0x000

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved					CEN	OSM	MIEN
Type/Reset						RW 0	RW 0	RW 0

Bits	Field	Descriptions
[2]	CEN	BFTM Counter Enable Control 0: BFTM is disabled 1: BFTM is enabled When this bit is set to 1, the BFTM counter will start to count. The counter will stop counting and the counter value will remain unchanged when the CEN bit is cleared to 0 by the application program regardless of whether it is in the repetitive or one shot mode. However, in the one shot mode, the counter will stop counting and be reset to 0 when the CEN bit is cleared to 0 by the timer hardware circuitry which results from a compare match event.
[1]	OSM	BFTM One Shot Mode Selection 0: Counter operates in repetitive mode 1: Counter operates in one shot mode
[0]	MIEN	BFTM Compare Match Interrupt Enable Control 0: Compare Match Interrupt is disabled 1: Compare Match Interrupt is enabled

BFTM Status Register – BFTMSR

This register specifies the BFTM status.

Offset: 0x004

Reset value: 0x0000_0004

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved							MIF
Type/Reset								W0C 0

Bits	Field	Descriptions
[0]	MIF	BFTM Compare Match Interrupt Flag 0: No compare match event occurs 1: Compare match event occurs When the counter value, CNT, is equal to the compare register value, CMP, a compare match event will occur and the corresponding interrupt flag, MIF will be set. The MIF bit is cleared to 0 by writing a data "0".

BFTM Counter Register – BFTMCNTR

This register specifies the BFTM counter value.

Offset: 0x008

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	CNT							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	23	22	21	20	19	18	17	16
	CNT							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
	CNT							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	CNT							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[31:0]	CNT	BFTM Counter Value A 32-bit BFTM counter value is stored in this field which can be read or written on-the-fly.

BFTM Compare Value Register – BFTMCMPR

The register specifies the BFTM compare value.

Offset: 0x00C

Reset value: 0xFFFF_FFFF

	31	30	29	28	27	26	25	24
	CMP							
Type/Reset	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1
	23	22	21	20	19	18	17	16
	CMP							
Type/Reset	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1
	15	14	13	12	11	10	9	8
	CMP							
Type/Reset	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1
	7	6	5	4	3	2	1	0
	CMP							
Type/Reset	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1

Bits	Field	Descriptions
[31:0]	CMP	BFTM Compare Value This register specifies a 32-bit BFTM compare value which is used for comparison with the BFTM counter value.

15 Single-Channel Timer (SCTM)

Introduction

The Single-Channel Timer consists of one 16-bit up-counter, one 16-bit Capture/Compare Registers (CCRs), one 16-bit Counter-Reload Register (CRR) and several control/status registers. It can be used for a variety of purposes including general timer, input signal pulse width measurement or output waveform generation such as single pulse generation or PWM output.

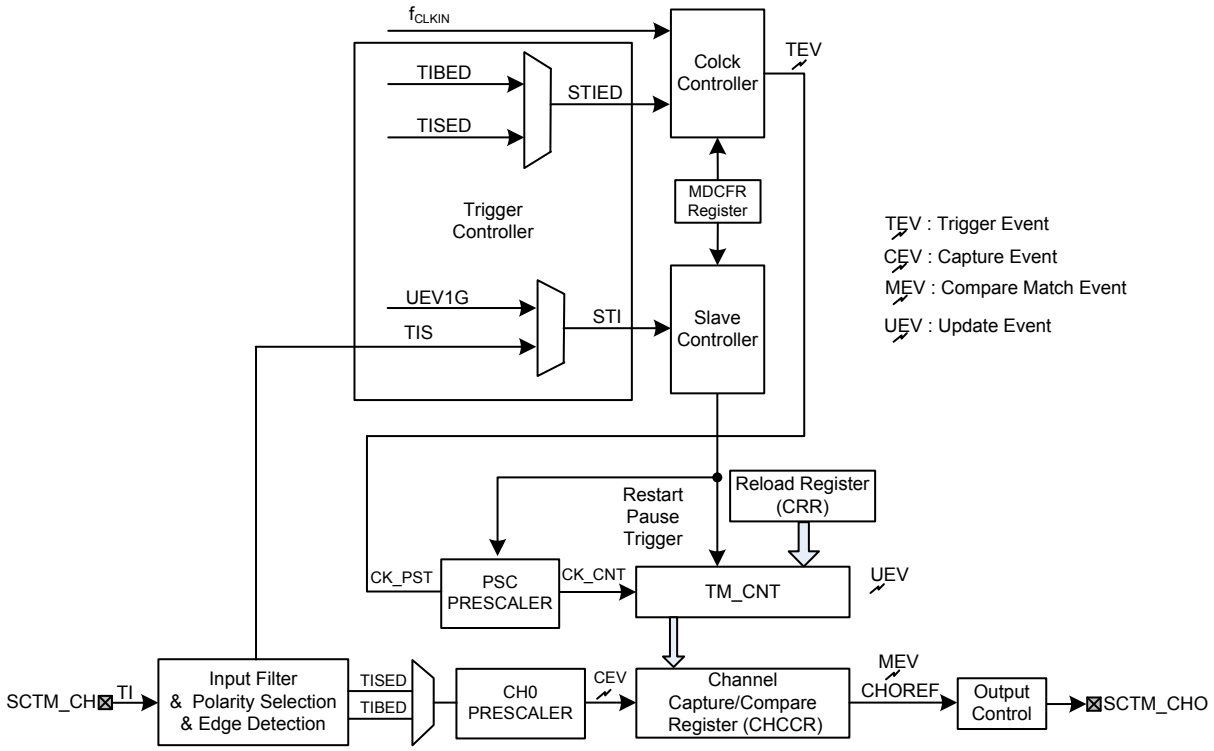


Figure 63. SCTM Block Diagram

Features

- 16-bit auto-reload up counter
- 16-bit programmable prescaler that allows division of the counter clock frequency by any factor between 1 and 65536
- Single channel for:
  - Input Capture function
  - Compare Match Output
- Interrupt generation with the following events:
  - Update event
  - Trigger event
  - Input capture event
  - Output compare match event

Functional Descriptions

Counter Mode

Up-Counting

The counter counts continuously from 0 to the counter-reload value, which is defined in the CRR register. Once the counter reaches the counter-reload value, the Timer Module generates an overflow event and the counter restarts to count once again from 0. This action will continue repeatedly. When the update event is generated by setting the UEVG bit in the EVGR register to 1, the counter value will also be initialized to 0.

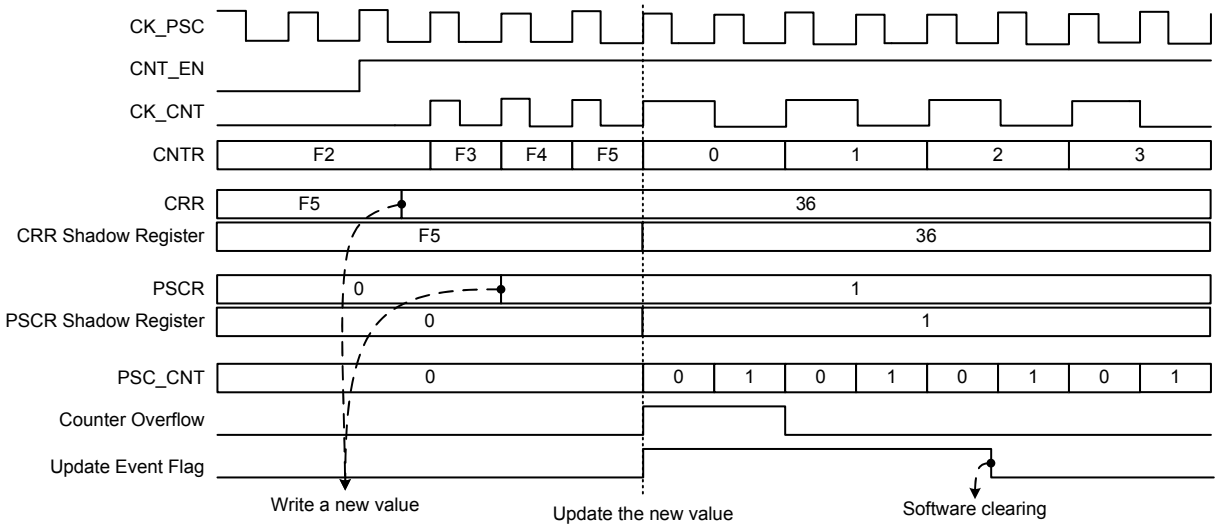


Figure 64. Up-counting Example

Clock Controller

The following describes the Timer Module clock controller which determines the clock source of the internal prescaler counter.

- Internal APB clock f_{CLKIN}:
  The default internal clock source is the APB clock f_{CLKIN} used to drive the counter prescaler when the slave mode is disabled. When the slave mode selection bits SMSEL are set to 0x4, 0x5 or 0x6, the internal APB clock f_{CLKIN} is the counter prescaler driving clock source. If the slave mode controller is enabled by setting SMSEL field in the MDCFR register to 0x7, the prescaler is clocked by other clock sources selected by the TRSEL field in the TRCFR register and described as follows.

- STIED:
  The counter prescaler can count during each rising edge of the STI signal. This mode can be selected by setting the SMSEL field to 0x7 in the MDCFR register. Here the counter will act as an event counter. The input event, known as STI here, can be selected by setting the TRSEL field to an available value except the value of 0x0. When the STI signal is selected as the clock source, the internal edge detection circuitry will generate a clock pulse during each STI signal rising edge to drive the counter prescaler. It is important to note that if the TRSEL field is set to 0x0 to select the software UEVG bit as the trigger source, then when the SMSEL field is set to 0x7, the counter will be updated instead of counting.

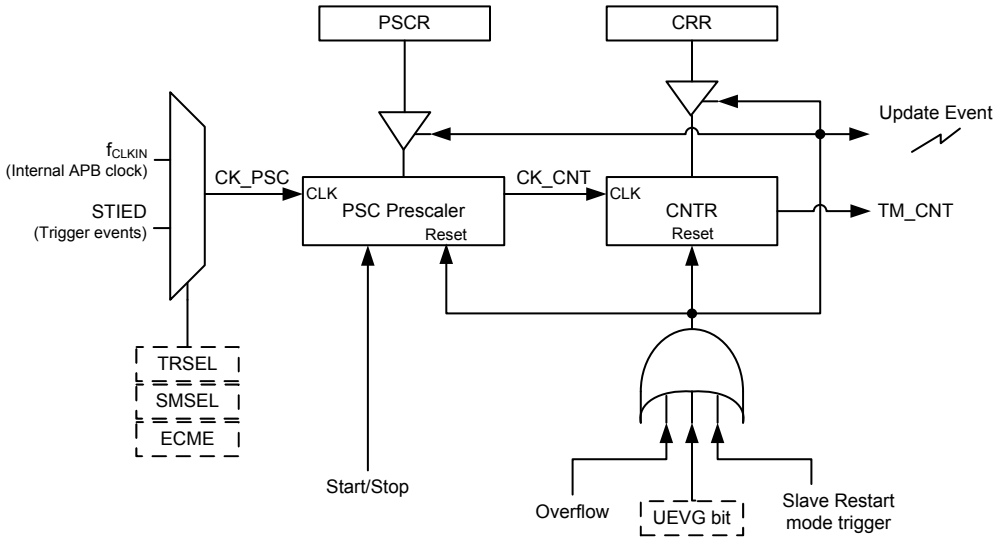


Figure 65. SCTM Clock Selection Source

Trigger Controller

The trigger controller is used to select the trigger source and setup the trigger level or edge trigger condition. For the internal trigger input, it can be selected by the Trigger Selection bits TRSEL in the TRCFR register. For all the trigger sources except the UEVG bit software trigger, the internal edge detection circuitry will generate a clock pulse at each trigger signal rising edge to stimulate some SCTM functions which are triggered by a trigger signal rising edge.

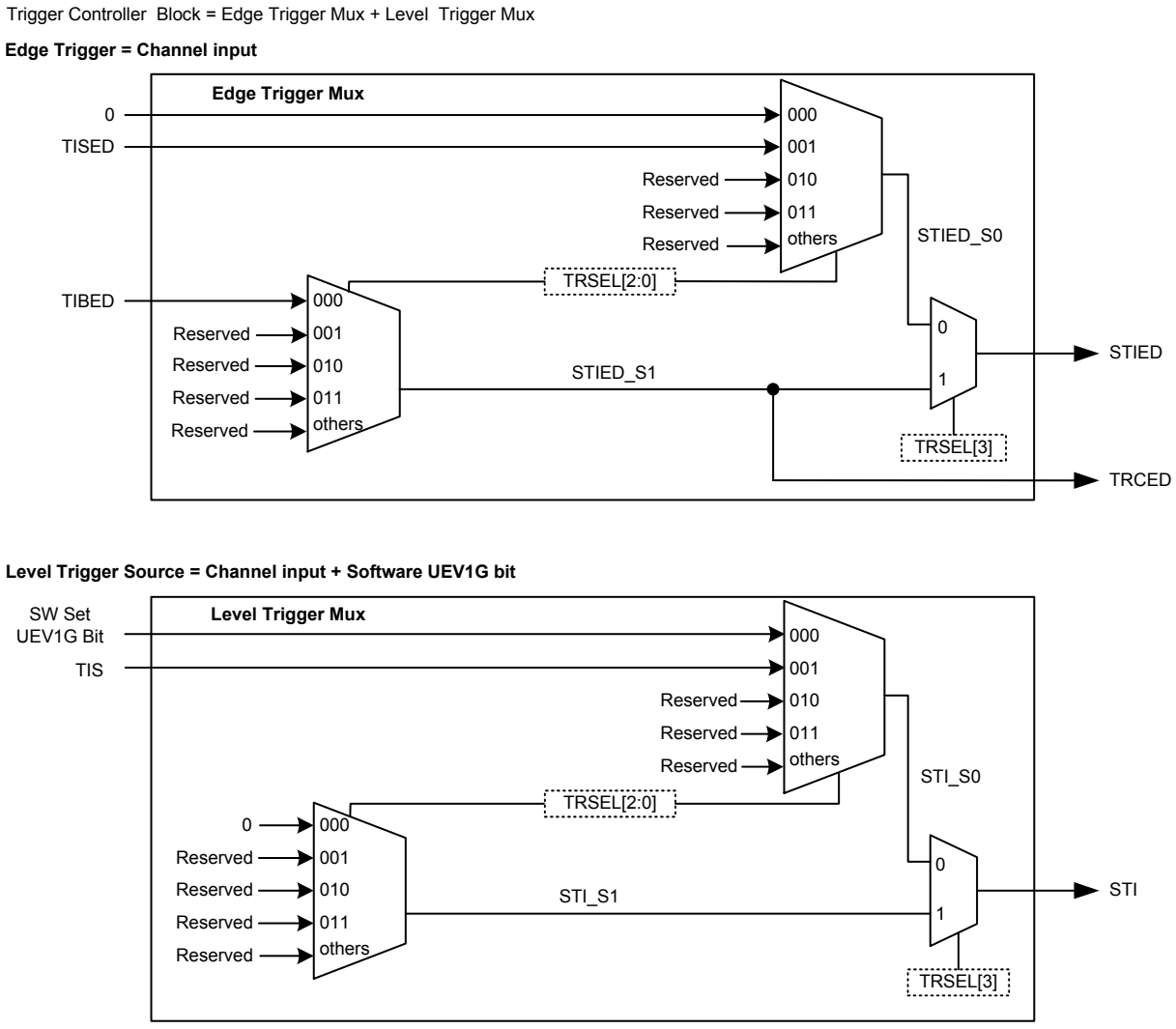


Figure 66. Trigger Control Block

Slave Controller

The SCTM can be synchronized with an external trigger in several modes including the Restart mode, the Pause mode and the Trigger mode which is selected by the SMSEL field in the MDCFR register. The trigger input of these modes comes from the STI signal which is selected by the TRSEL field in the TRCFR register. The operation modes in the Slave Controller are described in the accompanying sections.

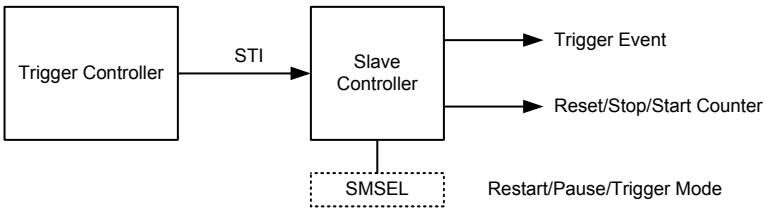


Figure 67. Slave Controller Diagram

Restart Mode

The counter and its prescaler can be reinitialized in response to a rising edge of the STI signal. When a STI rising edge occurs, the update event software generation bit named UEVG will automatically be asserted by hardware and the trigger event flag will also be set. Then the counter and prescaler will be reinitialized. Although the UEVG bit is set to 1 by hardware, the update event does not really occur. It depends upon whether the update event disable control bit UEVDIS is set to 1 or not. If the UEVDIS is set to 1 to disable the update event to occur, there will no update event be generated, however the counter and prescaler are still reinitialized when the STI rising edge occurs. If the UEVDIS bit in the CNTCFR register is cleared to enable the update event to occur, an update event will be generated together with the STI rising edge, then all the preloaded registers will be updated.

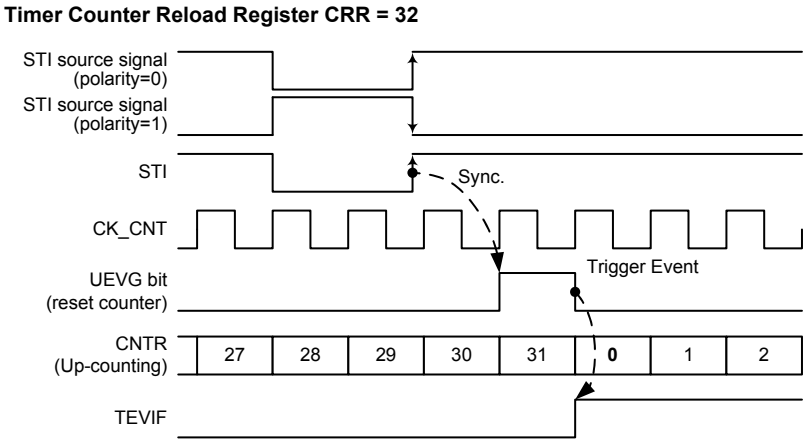


Figure 68. SCTM in Restart Mode

Pause Mode

In the Pause Mode, the selected STI input signal level is used to control the counter start/stop operation. The counter starts to count when the selected STI signal is at a high level and stops counting when the STI signal is changed to a low level, here the counter will maintain its present value and will not be reset. Since the Pause function depends upon the STI level to control the counter stop/start operation, the selected STI trigger signal can not be derived from the TIBED signal.

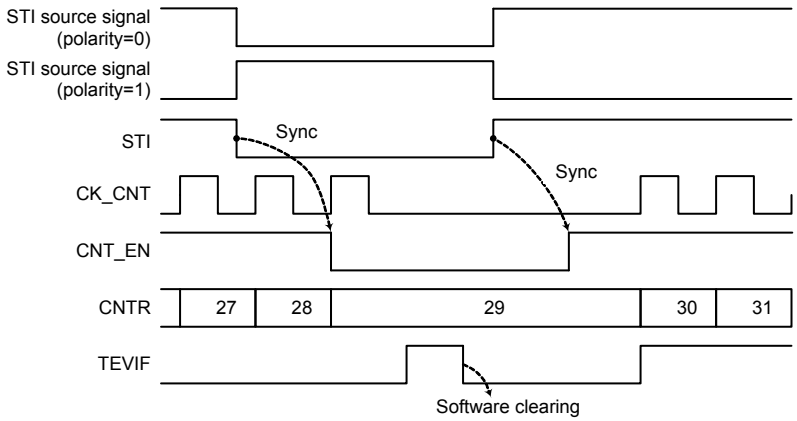


Figure 69. SCTM in Pause Mode

Trigger Mode

After the counter is disabled to count, the counter can resume counting when a STI rising edge signal occurs. When an STI rising edge occurs, the counter will start to count from the current value in the counter. Note that if the STI signal is selected to be derived from the UEVG bit software trigger, the counter will not resume counting. When software triggering using the UEVG bit is selected as the STI source signal, there will be no clock pulse generated which can be used to make the counter resume counting. Note that the STI signal is only used to enable the counter to resume counting and has no effect on controlling the counter to stop counting.

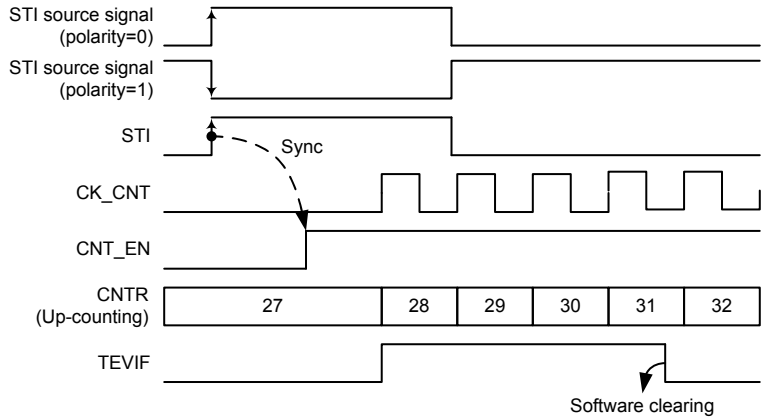


Figure 70. SCTM in Trigger Mode

Channel Controller

The SCTM channel can be used as the capture input or compare match output. The capture input or compare match output channel is composed of a preload register and a shadow register. The Data access of the APB bus is always through the read/write preload register.

In the input capture mode, the counter value is captured into the CHCCR shadow register first and then transferred into the CHCCR preload register when the capture event occurs.

In the compare match output mode, the contents of the CHCCR preload register is copied into the associated shadow register and the counter value is then compared with the register value.

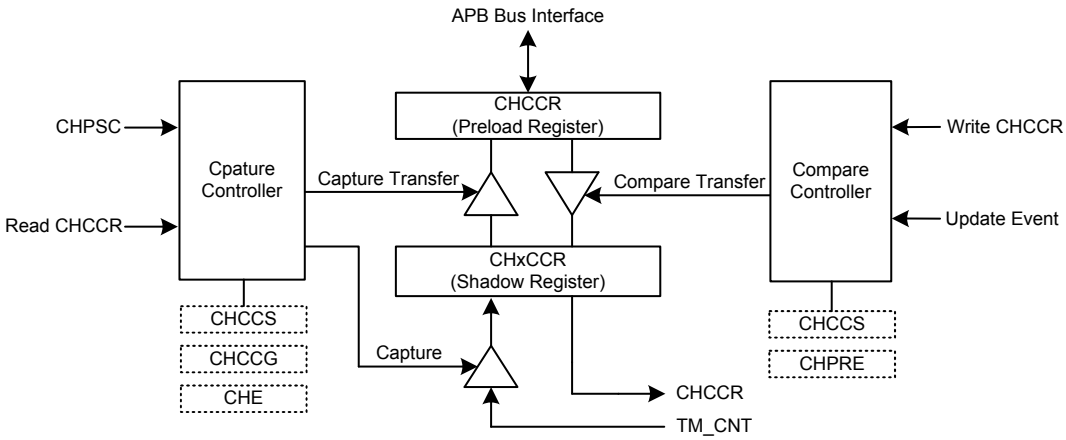


Figure 71. Capture/Compare Block Diagram

Capture Counter Value Transferred to CHCCR

When the channel is used as a capture input, the counter value is captured into the Channel Capture/Compare Register (CHCCR) when an effective input signal transition occurs. Once the capture event occurs, the CHCCIF flag in the INTSR register is set accordingly. If the CHCCIF bit is already set, i.e., the flag has not yet been cleared by software and another capture event on this channel occurs, the corresponding channel Over-Capture flag, named CHOCF, will be set.

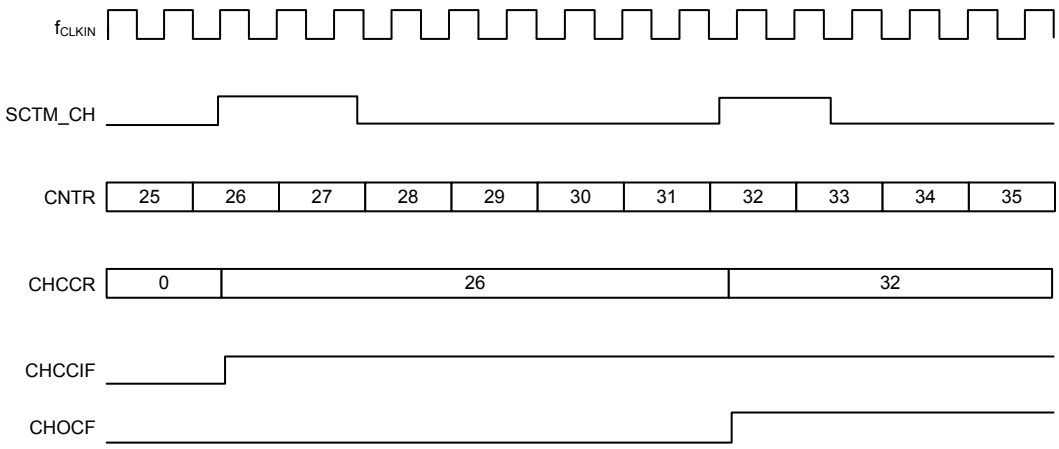


Figure 72. Input Capture Mode

Input Stage

The input stage consists of a digital filter, a channel polarity selection, edge detection and a channel prescaler. The channel input signal (TI) is sampled by a digital filter to generate a filtered input signal TIFP. Then the channel polarity and the edge detection block can generate a TISED signal for the input capture function. The effective input event number can be set by the channel input prescaler register (CHPSC).

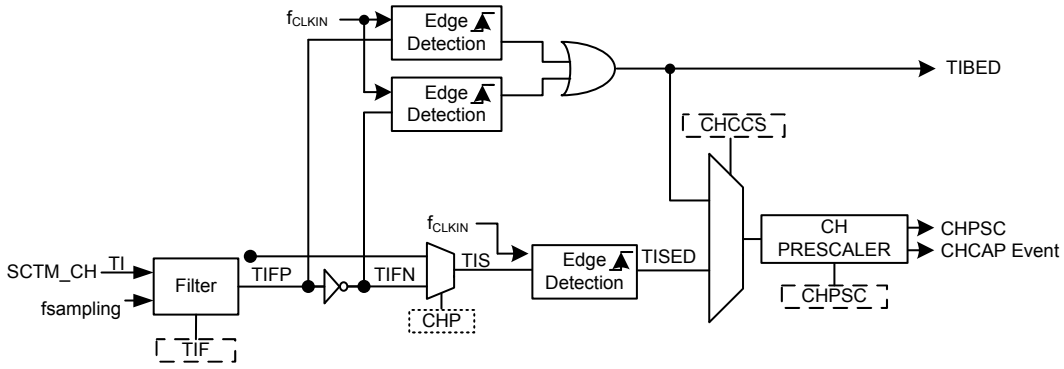


Figure 73. Channel Input Stages

Digital Filter

The digital filters are embedded in the channel input stage. The digital filter in the SCTM is an N-event counter where N refers to how many valid transitions are necessary to output a filtered signal. The N value can be 0, 2, 4, 5, 6 or 8 according to the user selection for each filter.

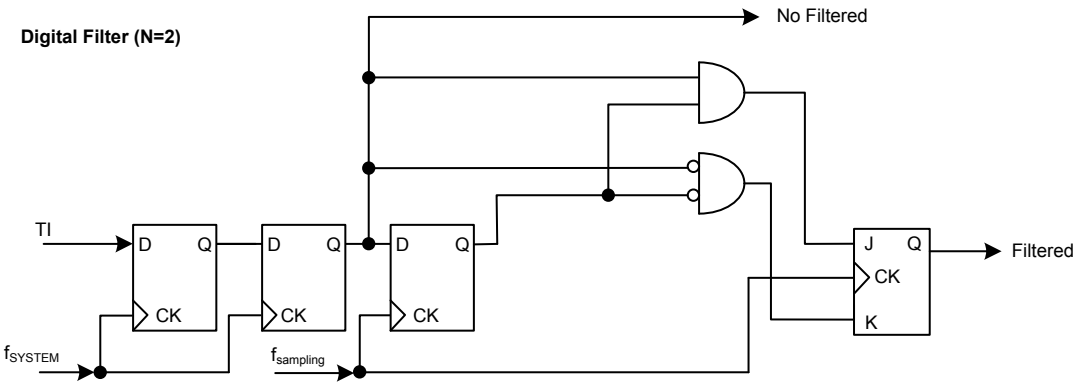


Figure 74. TI Digital Filter Diagram with N = 2

Output Stage

The SCTM output has functions for compare match, single pulse or PWM output. The channel output SCTM_CHO is controlled by the CHOM, CHP and CHE bits in the corresponding CHOCFR, CHPOLR and CHCTR registers.

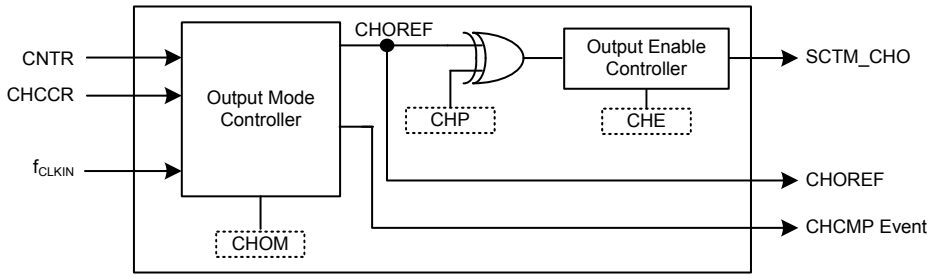


Figure 75. Output Stage Block Diagram

Channel Output Reference Signal

When the SCTM is used in the compare match output mode, the CHOREF signal (Channel Output Reference signal) is defined by the CHOM bit setup. The CHOREF signal has several types of output function which defines what happens to the output when the counter value matches the contents of the CHCCR register. In addition to the low, high and toggle CHOREF output types, there are also PWM mode 1 and PWM mode 2 outputs. In these modes, the CHOREF signal level is changed according to the relationship between the counter value and the CHCCR content. There are also two modes which will force the output into an inactive or active state irrespective of the CHCCR content or counter values. With regard to a more detailed description refer to the relative bit definition. The accompanying Table 34 shows a summary of the output type setup.

Table 34. Compare Match Output Setup

CHOM value	Compare Match Level
0x00	No change
0x01	Clear Output to 0
0x02	Set Output to 1
0x03	Toggle Output
0x04	Force Inactive Level
0x05	Force Active Level
0x06	PWM Mode 1
0x07	PWM Mode 2

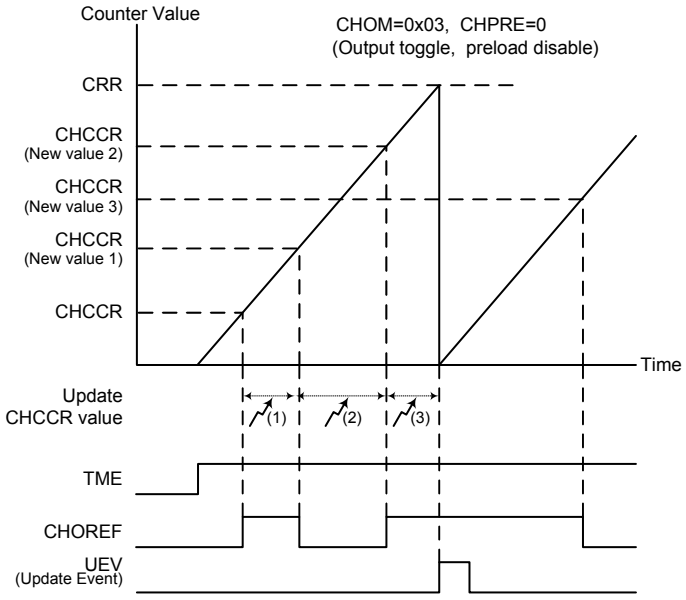


Figure 76. Toggle Mode Channel Output Reference Signal – CHPRE = 0

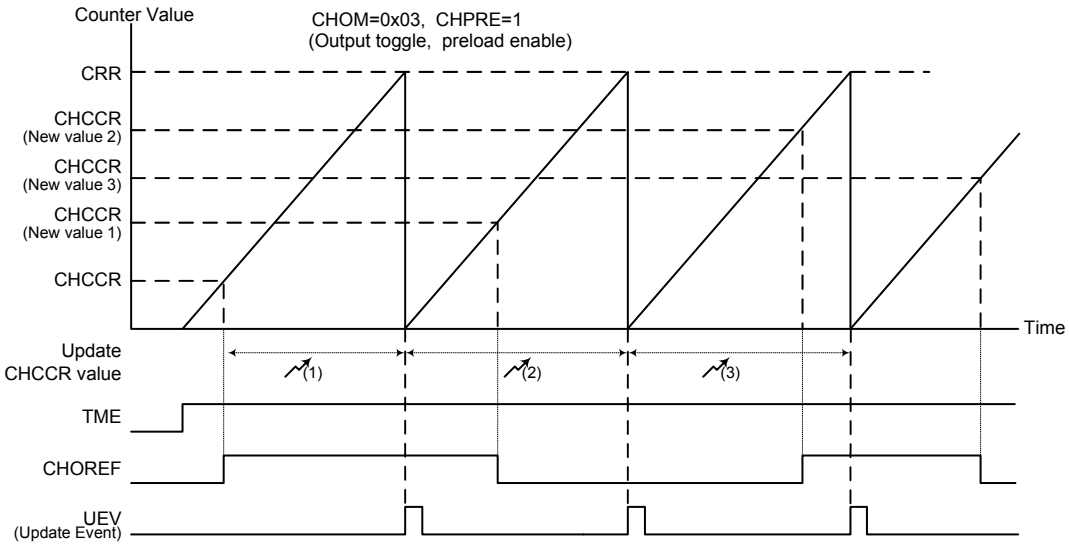


Figure 77. Toggle Mode Channel Output Reference Signal – CHPRE = 1

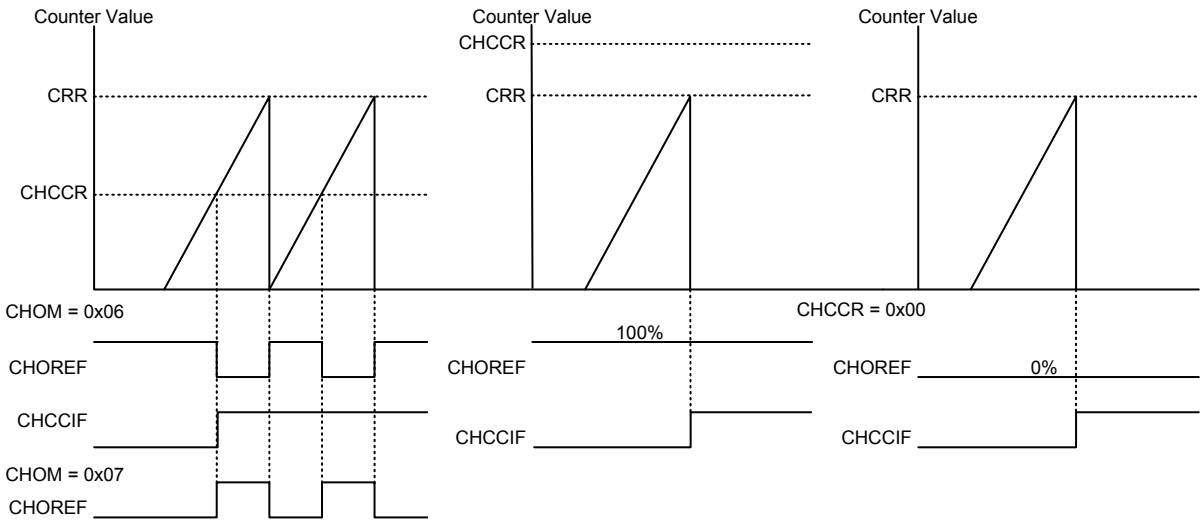


Figure 78. PWM Mode Channel Output Reference Signal

Update Management

The Update event is used to update the CRR, PSCR and CHCCR values from the actual registers to the corresponding shadow registers. An update event will occur when the counter overflows, the software update control bit is triggered or an update event from the slave controller is generated.

The UEVDIS bit in the CNTCFR register can determine whether the update event occurs or not. When the update event occurs, the corresponding update event interrupt will be generated depending upon whether the update event interrupt generation function is enabled or not by configuring the UGDIS bit in the CNTCFR register. For more detailed description, refer to the UEVDIS and UGDIS bit definition in the CNTCFR register.

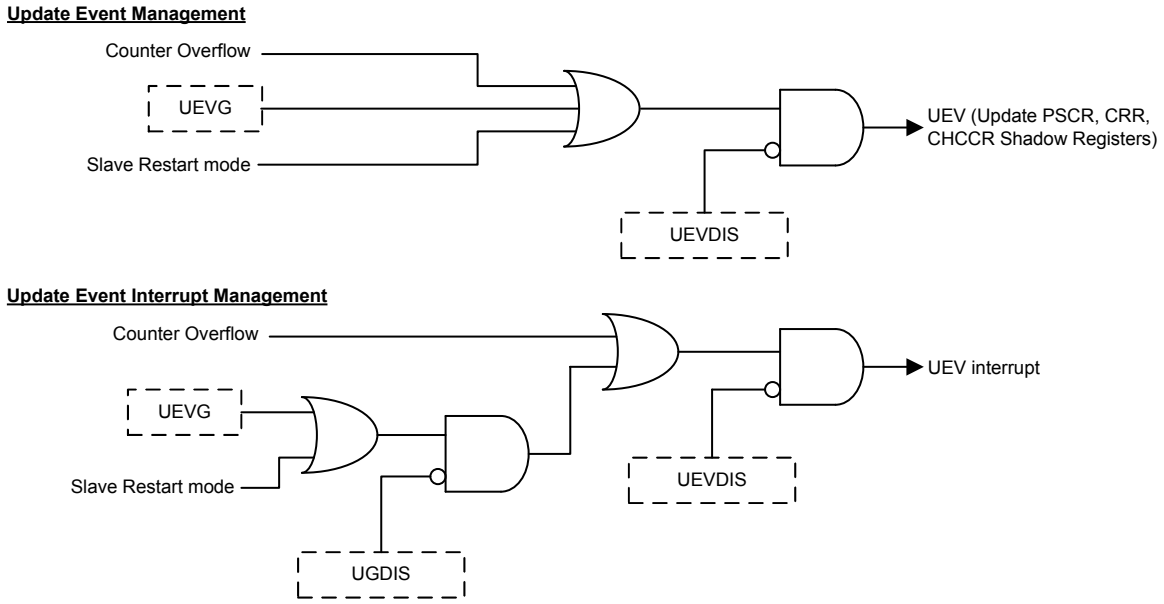


Figure 79. Update Event Setting Diagram

Register Map

The following table shows the SCTM registers and reset values.

Table 35. SCTM Register Map

Register	Offset	Description	Reset Value
CNTCFR	0x000	Timer Counter Configuration Register	0x0000_0000
MDCFR	0x004	Timer Mode Configuration Register	0x0000_0000
TRCFR	0x008	Timer Trigger Configuration Register	0x0000_0000
CTR	0x010	Timer Control Register	0x0000_0000
CHICFR	0x020	Channel Input Configuration Register	0x0000_0000
CHOCFR	0x040	Channel Output Configuration Register	0x0000_0000
CHCTR	0x050	Channel Control Register	0x0000_0000
CHPOLR	0x054	Channel Polarity Configuration Register	0x0000_0000
DICTR	0x074	Timer Interrupt Control Register	0x0000_0000
EVGR	0x078	Timer Event Generator Register	0x0000_0000
INTSR	0x07C	Timer Interrupt Status Register	0x0000_0000
CNTR	0x080	Timer Counter Register	0x0000_0000
PSCR	0x084	Timer Prescaler Register	0x0000_0000
CRR	0x088	Timer Counter Reload Register	0x0000_FFFF
CHCCR	0x090	Channel Capture/Compare Register	0x0000_0000

Register Descriptions

Timer Counter Configuration Register – CNTCFR

This register specifies the SCTM counter configuration.

Offset: 0x000

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved						CKDIV	
Type/Reset							RW 0	RW 0
	7	6	5	4	3	2	1	0
	Reserved						UGDIS	UEVDIS
Type/Reset							RW 0	RW 0

Bits	Field	Descriptions
[9:8]	CKDIV	Clock Division These two bits define the frequency ratio between the timer clock (f_{CLKIN}) and the dead-time clock (f_{DTS}). The dead-time clock is also used for digital filter sampling clock. 00: $f_{DTS} = f_{CLKIN}$ 01: $f_{DTS} = f_{CLKIN} / 2$ 10: $f_{DTS} = f_{CLKIN} / 4$ 11: Reserved
[1]	UGDIS	Update event interrupt generation disable control 0: Any of the following events will generate an update interrupt - Counter overflow - Setting the UEVG bit - Update generation through the slave mode 1: Only counter overflow generates an update interrupt
[0]	UEVDIS	Update event Disable control 0: Enable the update event request by one of following events: - Counter overflow - Setting the UEVG bit - Update generation through the slave mode 1: Disable the update event (However the counter and the prescaler are reinitialized if the UEVG bit is set or if a hardware restart is received from the slave mode)

Timer Mode Configuration Register – MDCFR

This register specifies the SCTM slave mode selection.

Offset: 0x004

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved					SMSEL		
Type/Reset						RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	Reserved							
Type/Reset								

Bits	Field	Descriptions
[10:8]	SMSEL	Slave Mode Selection

SMSEL [2:0]	Mode	Descriptions
000	Disable mode	The prescaler is clocked directly by the internal clock.
100	Restart Mode	The counter value restarts from 0 or the CRR shadow register value depending upon the counter mode on the rising edge of the STI signal. The registers will also be updated.
101	Pause Mode	The counter starts to count when the selected trigger input STI is high. The counter stops counting on the instant, not being reset, when the STI signal changes its state to a low level. Both the counter start and stop control are determined by the STI signal.
110	Trigger Mode	The counter starts to count from the original value in the counter on the rising edge of the selected trigger input STI. Only the counter start control is determined by the STI signal.
111	STIED	The rising edge of the selected trigger signal STI will clock the counter.
Others	Reserved	—

Timer Trigger Configuration Register – TRCFR

This register specifies the SCTM trigger source selection.

Offset: 0x008

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved				TRSEL			
Type/Reset					RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[3:0]	TRSEL	Trigger Source Selection These bits are used to select the trigger input (STI) for counter synchronizing. 0000: Software Trigger by setting the UEVG bit 0001: Filtered input of channel (TIS) 0011: Reserved 1000: Channel both edge detector (TIBED) Others: Default 0 Note: These bits must be updated only when they are not in use, i.e. the slave mode is disabled by setting the SMSEL field to 0x00.

Timer Counter Register – CTR

This register specifies the timer enable bit (TME), CRR buffer enable bit (CRBE).

Offset: 0x010

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved						CRBE	TME
Type/Reset							RW 0	RW 0

Bits	Field	Descriptions
[1]	CRBE	Counter-Reload register Buffer Enable 0: Counter reload register can be updated immediately 1: Counter reload register cannot be updated until the update event occurs
[0]	TME	Timer Enable bit 0: SCTM off 1: SCTM on – SCTM functions normally When the TME bit is cleared to 0, the counter will be stopped and the SCTM will consume no power in any operation mode except for the single pulse mode and the slave trigger mode. In these two modes the TME bit can automatically be set to 1 by hardware which permits all the SCTM registers to function normally.

Channel Input Configuration Register – CHICFR

This register specifies the channel input mode configuration.

Offset: 0x020

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved				CHPSC		CHCCS	
Type/Reset					RW 0	RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved				TIF			
Type/Reset					RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[19:18]	CHPSC	Channel Capture Input Source Prescaler Setting These bits define the effective events of the channel capture input. Note that the prescaler is reset once the Channel Capture/Compare Enable bit, CHE, in the Channel Control register named CHCTR is cleared to 0. 00: No prescaler, channel capture input signal is chosen for each active event 01: Channel Capture input signal is chosen for every 2 events 10: Channel Capture input signal is chosen for every 4 events 11: Channel Capture input signal is chosen for every 8 events
[17:16]	CHCCS	Channel Capture/Compare Selection. 00: Channel is configured as an output 01: Channel is configured as an input derived from the TI signal 10: Reserved 11: Channel is configured as an input which comes from the TIBED signal Note: The CHCCS field can be accessed only when the CHE bit is cleared to 0.

Bits	Field	Descriptions
[3:0]	TIF	Channel Input Source TI Filter Setting These bits define the frequency divided ratio used to sample the TI signal. The Digital filter in the SCTM is an N-event counter where N is defined as how many valid transitions are necessary to output a filtered signal. 0000: No filter, the sampling clock is f_{SYSTEM} 0001: $f_{SAMPLING} = f_{CLKIN}$, N = 2 0010: $f_{SAMPLING} = f_{CLKIN}$, N = 4 0011: $f_{SAMPLING} = f_{CLKIN}$, N = 8 0100: $f_{SAMPLING} = f_{DTS} / 2$, N = 6 0101: $f_{SAMPLING} = f_{DTS} / 2$, N = 8 0110: $f_{SAMPLING} = f_{DTS} / 4$, N = 6 0111: $f_{SAMPLING} = f_{DTS} / 4$, N = 8 1000: $f_{SAMPLING} = f_{DTS} / 8$, N = 6 1001: $f_{SAMPLING} = f_{DTS} / 8$, N = 8 1010: $f_{SAMPLING} = f_{DTS} / 16$, N = 5 1011: $f_{SAMPLING} = f_{DTS} / 16$, N = 6 1100: $f_{SAMPLING} = f_{DTS} / 16$, N = 8 1101: $f_{SAMPLING} = f_{DTS} / 32$, N = 5 1110: $f_{SAMPLING} = f_{DTS} / 32$, N = 6 1111: $f_{SAMPLING} = f_{DTS} / 32$, N = 8

Channel Output Configuration Register – CHOCFR

This register specifies the channel output mode configuration.

Offset: 0x040

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved			CHPRE	Reserved	CHOM[2:0]		
Type/Reset				RW 0		RW 0	RW 0	RW 0

Bits	Field	Descriptions
[4]	CHPRE	Channel Capture/Compare Register (CHCCR) Preload Enable 0: CHCCR preload function is disabled The CHCCR register can be immediately assigned a new value when the CHPRE bit is cleared to 0 and the updated CHCCR value is used immediately. 1: CHCCR preload function is enabled The new CHCCR value will not be transferred to its shadow register until the update event occurs.
[2:0]	CHOM[2:0]	Channel Output Mode Setting These bits define the functional types of the output reference signal CHOREF. 000: No Change 001: Output 0 on compare match 010: Output 1 on compare match 011: Output toggles on compare match 100: Force inactive – CHOREF is forced to 0 101: Force active – CHOREF is forced to 1 110: PWM mode 1 - During up-counting, channel has an active level when CNTR < CHCCR or otherwise has an inactive level. 111: PWM mode 2 - During up-counting, channel has an inactive level when CNTR < CHCCR or otherwise has an active level.

Channel Control Register – CHCTR

This register contains the channel capture input or compare output function enable control bit.

Offset: 0x050

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved							CHE
Type/Reset								RW 0

Bits	Field	Descriptions
[0]	CHE	Channel Capture/Compare Enable - Channel is configured as an input (CHCCS = 0x01/0x03) 0: Input Capture Mode is disabled 1: Input Capture Mode is enabled - Channel is configured as an output (CHCCS = 0x00) 0: Off – Channel output signal CHO is not active 1: On – Channel output signal CHO generated on the corresponding output pin

Channel Polarity Configuration Register – CHPOLR

This register contains the channel capture input or compare output polarity control bit.

Offset: 0x054

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved							CHP
Type/Reset								RW 0

Bits	Field	Descriptions
[0]	CHP	Channel Capture/Compare Polarity - When Channel is configured as an input 0: capture event occurs on a Channel rising edge 1: capture event occurs on a Channel falling edge - When Channel is configured as an output (CHCCS = 0x00) 0: Channel Output is active high 1: Channel Output is active low

Timer Interrupt Control Register – DICTR

This register contains the timer interrupt enable control bits.

Offset: 0x074

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved					TEVIE	Reserved	UEVIE
Type/Reset						RW 0		RW 0
	7	6	5	4	3	2	1	0
	Reserved							CHCCIE
Type/Reset								RW 0

Bits	Field	Descriptions
[10]	TEVIE	Trigger event Interrupt Enable 0: Trigger event interrupt is disabled 1: Trigger event interrupt is enabled
[8]	UEVIE	Update event Interrupt Enable 0: Update event interrupt is disabled 1: Update event interrupt is enabled
[0]	CHCCIE	Channel Capture/Compare Interrupt Enable 0: Channel interrupt is disabled 1: Channel interrupt is enabled

Timer Event Generator Register – EVGR

This register contains the software event generation bits.

Offset: 0x078

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved					TEVG	Reserved	UEVG
Type/Reset						WO 0		WO 0
	7	6	5	4	3	2	1	0
	Reserved							CHCCG
Type/Reset								WO 0

Bits	Field	Descriptions
[10]	TEVG	Trigger Event Generation The trigger event TEV can be generated by setting this bit. It is cleared by hardware automatically. 0: No action 1: TEVIF flag is set
[8]	UEVG	Update Event Generation The update event UEV can be generated by setting this bit. It is cleared by hardware automatically. 0: No action 1: Reinitialize the counter The counter value returns to 0 or the CRR preload value, depending on the counter mode in which the current timer is being used. An update operation of any related registers will also be performed. For more detail descriptions, refer to the corresponding section.
[0]	CHCCG	Channel Capture/Compare Generation A Channel capture/compare event can be generated by setting this bit. It is cleared by hardware automatically. 0: No action 1: Capture/compare event is generated on channel. If Channel is configured as an input, the counter value is captured into the CHCCR register and then the CHCCIF bit is set. If Channel is configured as an output, the CHCCIF bit is set.

Timer Interrupt Status Register – INTSR

This register stores the timer interrupt status.

Offset: 0x07C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved					TEVIF	Reserved	UEVIF
Type/Reset						W0C 0		W0C 0
	7	6	5	4	3	2	1	0
	Reserved			CHOCF	Reserved			CHCCIF
Type/Reset				W0C 0				W0C 0

Bits	Field	Descriptions
[10]	TEVIF	Trigger Event Interrupt Flag This flag is set by hardware on a trigger event and is cleared by software. 0: No trigger event occurs 1: Trigger event occurs
[8]	UEVIF	Update Event Interrupt Flag. This bit is set by hardware on an update event and is cleared by software. 0: No update event occurs 1: Update event occurs Note: The update event is derived from the following conditions: - The counter overflows - The UEVG bit is asserted - A restart trigger event occurs from the slave trigger input
[4]	CHOCF	Channel Over-Capture Flag This flag is set by hardware and cleared by software. 0: No over-capture event is detected 1: Capture event occurs again when the CHCCIF bit is already set and it is not yet cleared by software.
[0]	CHCCIF	Channel Capture/Compare Interrupt Flag - Channel is configured as an output: 0: No match event occurs 1: The contents of the counter CNTR have matched the content of the CHCCR register This flag is set by hardware when the counter value matches the CHCCR value. It is cleared by software. - Channel is configured as an input: 0: No input capture occurs 1: Input capture occurs This bit is set by hardware on a capture event. It is cleared by software or by reading the CHCCR register.

Timer Counter Register – CNTR

This register stores the timer counter value.

Offset: 0x080

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	CNTV							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	CNTV							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	CNTV	Counter Value.

Timer Prescaler Register – PSCR

This register specifies the timer prescaler value to generate the counter clock.

Offset: 0x084

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	PSCV							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	PSCV							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	PSCV	Prescaler Value These bits are used to specify the prescaler value to generate the counter clock frequency f_{CK_CNT}. $f_{CK\_CNT} = \frac{f_{CK\_PSC}}{PSCV[15:0] + 1}$, where the f_{CK_PSC} is the prescaler clock source.

Timer Counter Reload Register – CRR

This register specifies the timer counter reload value.

Offset: 0x088

Reset value: 0x0000_FFFF

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	CRV							
Type/Reset	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1
	7	6	5	4	3	2	1	0
	CRV							
Type/Reset	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1

Bits	Field	Descriptions
[15:0]	CRV	Counter Reload Value The CRV is the reload value which is loaded into the actual counter register.

Channel Capture/Compare Register – CHCCR

This register specifies the timer channel capture/compare value.

Offset: 0x090

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	CHCCV							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	CHCCV							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	CHCCV	Channel Capture/Compare Value - When Channel is configured as an output The CHCCR value is compared with the counter value and the comparison result is used to trigger the CHOREF output signal. - When Channel is configured as an input The CHCCR register stores the counter value captured by the last channel capture event.

16 Watchdog Timer (WDT)

Introduction

The Watchdog timer is a hardware timing circuitry that can be used to detect a system lock-up due to software trapped in a deadlock. The Watchdog timer can operate in a reset mode. The Watchdog timer will generate a reset when the counter counts down to a zero value. Therefore, the software should reload the counter value before a Watchdog timer underflow occurs. In addition, a reset will also be generated if the software reloads the counter before it reaches a delta value. That means that the Watchdog timer prevents a software deadlock that continuously triggers the Watchdog, the reload must occur when the Watchdog timer value has a value within a limited window of 0 and WDTD. The Watchdog timer counter can be stopped when the processor is in the debug or sleep mode. The register write protection function can be enabled to prevent an unexpected change in the Watchdog timer configuration.

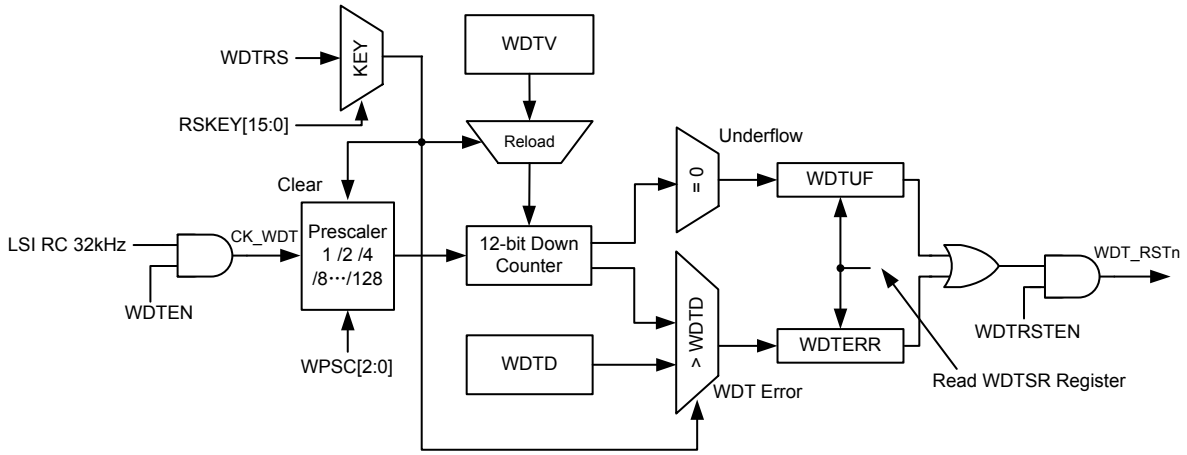


Figure 80. Watchdog Timer Block Diagram

Features

- Clock source from internal 32 kHz RC oscillator – LSI
- Can be independently setup to keep running or to stop when entering the sleep or deep sleep mode 1
- 12-bit down counter with 3-bit prescaler structure
- Provides reset to the system
- Limited reload window setup function for custom Watchdog timer reload times
- Watchdog Timer may be stopped when the processor is in the debug mode
- Reload lock key to prevent unexpected operation
- Configuration register write protection function for counter value, reset enable, delta value, and prescaler

Functional Description

The Watchdog timer is formed from a 12-bit count-down counter and a fixed 3-bit prescaler. The largest time-out period is 16 seconds, using the LSI clock and a 1/128 maximum prescaler value.

The Watchdog timer configuration setup includes a programmable counter reload value, reset enable, window value and prescaler value. These configurations are setup using the WDTMR0 and WDTMR1 registers which must be properly programmed before the Watchdog timer starts counting. In order to prevent unexpected write operations to those configurations, a register write protection function can be enabled by writing any value, other than 0x35CA to PROTECT[15:0], in the WDTPR register. A value of 0x35CA can be written to PROTECT[15:0] to disable the register write protection function before accessing any configuration register. A read operation on PROTECT[0] can obtain the enable/disable status of the register write protection function.

During normal operation, the Watchdog timer counter should be reloaded before it underflows to prevent the generation of a Watchdog reset. The 12-bit count-down counter can be reloaded with the required Watchdog Timer Counter Value (WDTV) by first setting the WDTRS bit to1 with the correct key, which is 0x5FA0 in the WDTCR register.

If a software deadlock occurs during a Watchdog timer reload routine, the reload operation will still go ahead and therefore the software deadlock cannot be detected. To prevent this situation from occurring, the reload operation must be executed in such a way that the value of the Watchdog timer counter is limited to within a delta value (WDTD). If the Watchdog timer counter value is greater than the delta value and a reload operation is executed, a Watchdog Timer error will occur. The Watchdog timer error will generate a Watchdog reset if the related functional control is enabled. Additionally, the above features can be disabled by programming a WDTD value greater than or equal to the WDTV value.

The WDTUF and WDTERR flags in the WDTSR register will be set respectively when the Watchdog timer underflows or when a Watchdog timer error occurs. A system reset or written one operation on the WDTSR register clears the WDTERR and WDTUF flags.

The watchdog timer uses two clocks: PCLK and CK_WDT. The PCLK clock is used for APB access to the watchdog registers. The CK_WDT clock is used for the Watchdog timer functionality and counting. There is some synchronization logic between these two clock domains.

When the system enters the Sleep or Deep sleep mode 1, the Watchdog timer counter will either continue to count or stop depending on the WDTSHLT bits in the WDTMR0 register. The Watchdog stops counting when the WDTSHLT bits are set in the Sleep mode. The count value is retained so that it continues counting after the system is woken up from the Sleep mode. A Watchdog reset will occur any time when the Watchdog timer is running and when it has an operating clock source. When the system enters the debug mode, the Watchdog timer counter will either continue to count or stop depending on the DB_WDT bit (in the MCUDBGCR register) in the Clock Control Unit.

The Watchdog timer should be used in the following manners:

- Set the Watchdog timer reload value (WDTV) and reset in the WDTMR0 register.
- Set the Watchdog timer delta value (WDTD) and prescaler in the WDTMR1 register.
- Start the Watchdog timer by writing to the WDTCR register with WDTRS = 1 and RSKEY = 0x5FA0.
- Write to the WDTPR register to lock all the Watchdog timer registers except for WDTCR and WDTPR.
- The Watchdog timer counter should be reloaded again within the delta value (WDTD).

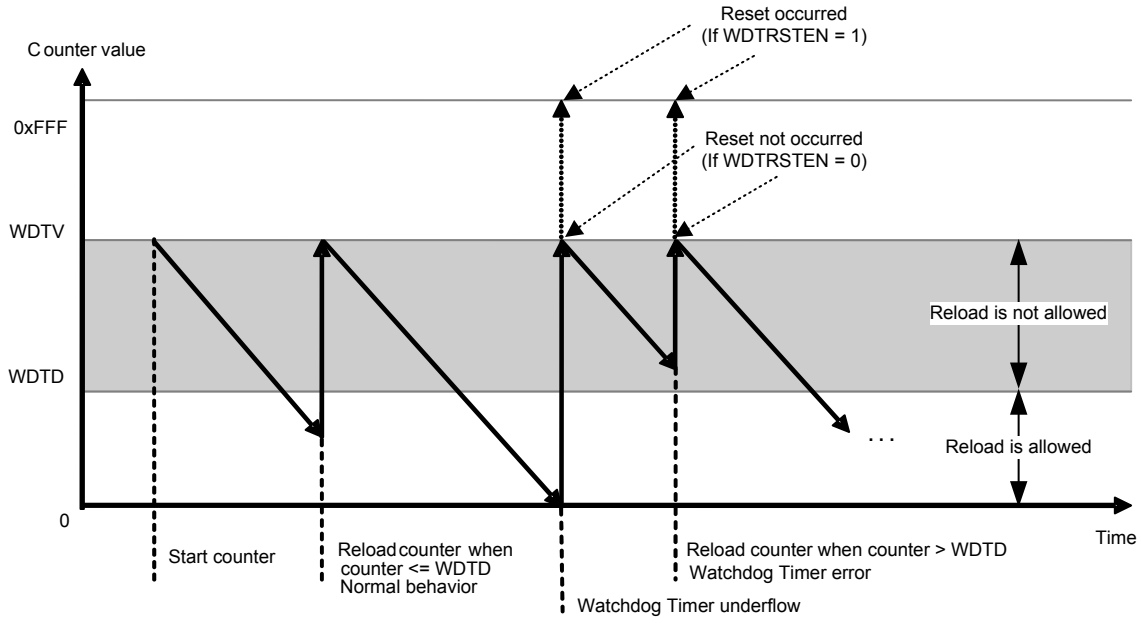


Figure 81. Watchdog Timer Behavior

Register Map

The following table shows the Watchdog Timer registers and reset values.

Table 36. Watchdog Timer Register Map

Register	Offset	Description	Reset Value
WDTCR	0x000	Watchdog Timer Control Register	0x0000_0000
WDTMR0	0x004	Watchdog Timer Mode Register 0	0x0000_0FFF
WDTMR1	0x008	Watchdog Timer Mode Register 1	0x0000_7FFF
WDTSR	0x00C	Watchdog Timer Status Register	0x0000_0000
WDTPR	0x010	Watchdog Timer Protection Register	0x0000_0000
WDTCSR	0x018	Watchdog Timer Clock Selection Register	0x0000_0000

Register Descriptions

Watchdog Timer Control Register – WDTCR

This register is used to reload the Watchdog timer.

Offset: 0x000

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	RSKEY							
Type/Reset	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	RSKEY							
Type/Reset	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0	WO 0
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	Reserved							
Type/Reset								
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	Reserved							WDTRS
Type/Reset								WO 0

Bits	Field	Descriptions
[31:16]	RSKEY	Watchdog Timer Reload Lock Key The RSKEY [15:0] bits should be written with a 0x5FA0 value to enable the WDT reload operation function. Writing any other value except 0x5FA0 in this field will abort the write operation.
[0]	WDTRS	Watchdog Timer Reload 0: No effect 1: Reload Watchdog Timer This bit is used to reload the Watchdog timer counter as a WDTV value which is stored in the WDTMR0 register. It is set to 1 by software and cleared to 0 by hardware automatically.

Watchdog Timer Mode Register 0 – WDTMR0

This register specifies the Watchdog timer counter reload value and reset enable control.

Offset: 0x004

Reset value: 0x0000_0FFF

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							WDTEN
Type/Reset								RW 0
	15	14	13	12	11	10	9	8
		WDTSHLT	WDTRSTEN	Reserved	WDTV			
Type/Reset	RW 0	RW 0	RW 0		RW 1	RW 1	RW 1	RW 1
	7	6	5	4	3	2	1	0
	WDTV							
Type/Reset	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1

Bits	Field	Descriptions
[16]	WDTEN	Watchdog Timer Running Enable 0: Watchdog timer is disabled 1: Watchdog timer is enabled to run. When the Watchdog timer is disabled, the counter will be reset to its hardware default condition. When the WDTEN bit is set, the Watchdog timer will be reloaded with the WDTV value and count down.
[15:14]	WDTSHLT	Watchdog Timer Sleep Halt 00: The Watchdog runs when the system is in the Sleep mode or Deep Sleep mode 1 01: The Watchdog runs when the system is in the Sleep mode and halts in Deep Sleep mode 1 10 or 11: The Watchdog halts when the system is in the Sleep mode and Deep Sleep mode 1 Note that the Watchdog timer always halts when the system is in Deep Sleep mode 2. If a Watchdog interrupt occurs in Sleep or Deep Sleep mode 1, it will wake up the device. The Watchdog stops counting when the WDTSHLT bits are set in the Sleep mode. The count value is retained so that it continues counting after the system wakes up from the Sleep mode.
[13]	WDTRSTEN	Watchdog Timer Reset Enable 0: A Watchdog Timer underflow or error has no effect on the reset of system. 1: A Watchdog Timer underflow or error triggers a Watchdog timer system reset.
[11:0]	WDTV	Watchdog Timer Counter Value The WDTV field defines the value loaded into the 12-bit Watchdog down counter.

Watchdog Timer Mode Register 1 – WDTMR1

This register specifies the Watchdog delta value and the prescaler selection.

Offset: 0x008

Reset value: 0x0000_7FFF

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved	WPSC			WDTD			
Type/Reset		RW 1	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1
	7	6	5	4	3	2	1	0
	WDTD							
Type/Reset	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1	RW 1

Bits	Field	Descriptions
[14:12]	WPSC	Watchdog Timer Prescaler Selection 000: 1/1 001: 1/2 010: 1/4 011: 1/8 100: 1/16 101: 1/32 110: 1/64 111: 1/128
[11:0]	WDTD	Watchdog Timer Delta Value Define the permitted range to reload the Watchdog timer. If the Watchdog timer counter value is less than or equal to the WDTD value, writing to the WDTCR register with WDTRS = 1 and RSKEY = 0x5FA0 will reload the timer. If the Watchdog Timer value is greater than the WDTD value, then writing WDTCR with WDTRS = 1 and RSKEY = 0x5FA0 will cause a Watchdog Timer error. This feature can be disabled by programming a WDTD value greater than or equal to the WDTV value.

Watchdog Timer Status Register – WDTSR

This register specifies the Watchdog timer status.

Offset: 0x00C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved						WDTERR	WDTUF
Type/Reset							WC 0	WC 0

Bits	Field	Descriptions
[1]	WDTERR	Watchdog Timer Error 0: No Watchdog timer error has occurred since the last read of this register 1: A Watchdog timer error has occurred since the last read of this register Note: A reload operation when the Watchdog timer counter value is larger than the WDTD value causes a Watchdog timer error. Note that this bit is a write-one clear flag.
[0]	WDTUF	Watchdog timer Underflow 0: No Watchdog timer underflow since the last read of this register 1: A Watchdog timer underflow has occurred since the last read of this register Note that this bit is a write-one clear flag.

Watchdog Timer Protection Register – WDTPR

This register specifies the Watchdog timer protect key configuration.

Offset: 0x010

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	PROTECT							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	PROTECT							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	PROTECT	Watchdog Timer Register Protection For write operation: 0x35CA: Disable the Watchdog timer register write protection Others: Enable the Watchdog timer register write protection For read operation: 0x0000: Watchdog timer register write protection is disabled 0x0001: Watchdog timer register write protection is enabled This register is used to enable/disable the Watchdog timer configuration register write protection function. All configuration registers become read only except for the WDTCR and WDTPR registers when the register write protection is enabled. Additionally, the read operation of PROTECT[0] can obtain the enable/disable status of the register write protection function.

Watchdog Timer Clock Selection Register – WDTCSR

This register specifies the Watchdog timer clock source selection and lock configuration.

Offset: 0x018

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved			WDTLOCK	Reserved			
Type/Reset				RW				
				0				

Bits	Field	Descriptions
[4]	WDTLOCK	Watchdog Timer Lock Mode 0: This bit is only set to 0 on any reset. It cannot be cleared by software. 1: This bit is set once only by software and locks the Watchdog timer function. Software can set this bit to 1 at any time. Once the WDTLOCK bit is set, the function and registers of the Watchdog timer cannot be modified or disabled, including the Watchdog timer clock source, and only waits for a system reset to disable the lock mode.

17 Inter-Integrated Circuit (I²C)

Introduction

The I²C Module is an internal circuit allowing communication with an external I²C interface which is an industry standard two line serial interface used for connection to external hardware. These two serial lines are known as a serial data line, SDA, and a serial clock line, SCL. The I²C module provides three data transfer rates: (1) 100 kHz in the Standard mode, (2) 400 kHz in the Fast mode and (3) 1MHz in the Fast-mode plus. The SCL period generation register is used to setup different kinds of duty cycle implementation for the SCL pulse.

The SDA line which is connected to the whole I²C bus is a bi-directional data line between the master and slave devices used for the transmission and reception of data. The I²C module also has an arbitration detection function to prevent the situation where more than one master attempts to transmit data on the I²C bus at the same time.

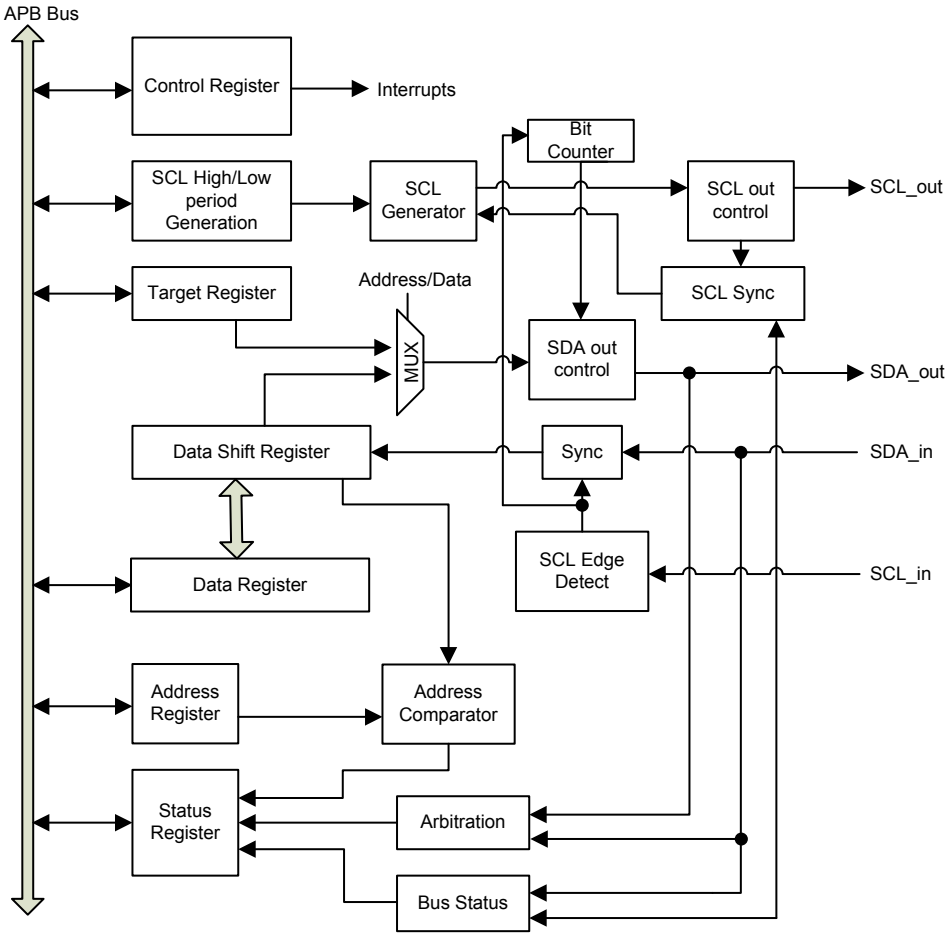


Figure 82. I²C Module Block Diagram

Features

- Two-wire I²C serial interface
  - Serial data line (SDA) and serial clock (SCL)
- Multiple speed modes
  - Standard mode – 100 kHz
  - Fast mode – 400 kHz
  - Fast mode plus – 1 MHz
- Bi-directional data transfer between master and slave
- Multi-master bus – no central master
  - The same interface can act as Master or Slave
- Arbitration among simultaneously transmitting masters without corrupting of serial data on the bus.
- Clock synchronization
  - Allow devices with different bit rates to communicate via one serial bus
- Supports 7-bit and 10-bit addressing mode and general call addressing.
- Multiple slave addresses using address mask function
- Time-out function

Functional Descriptions

Two Wire Serial Interface

The I²C module has two external lines, the serial data SDA and serial clock SCL lines, to carry information between the interconnected devices connected to the bus. The SCL and SDA lines are both bidirectional and must be connected to a pull-high resistor. When the I²C bus is in the free or idle state, both pins are at a high level to perform the required wired-AND function for multiple connected devices.

START and STOP Conditions

A master device can initialize a transfer by sending a START signal and terminate the transfer with a STOP signal. A START signal is usually referred to as the “S” bit, which is defined as a High to Low transition on the SDA line while the SCL line is high. A STOP signal is usually referred to as the “P” bit, which is defined as a Low to High transition on the SDA line while SCL is high.

A repeated START, which is denoted as the “Sr” bit, is functionally identical to the normal START condition. A repeated START signal allows the I²C interface to communicate with another slave device or with the same device but in a different transfer direction without releasing the I²C bus control.

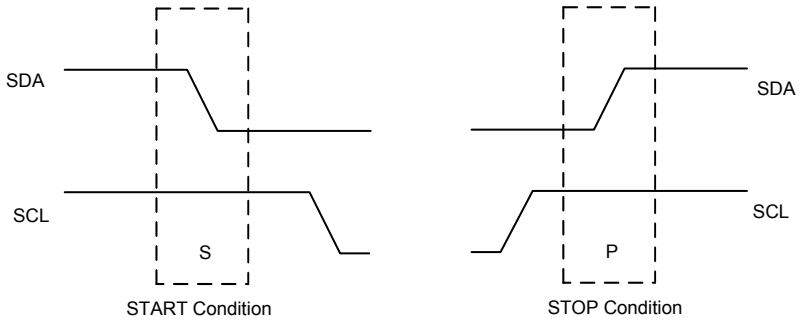


Figure 83. START and STOP Condition

Data Validity

The data on the SDA line must be stable during the high period of the SCL clock. The SDA data state can only be changed when the clock signal on the SCL line is in a low state.

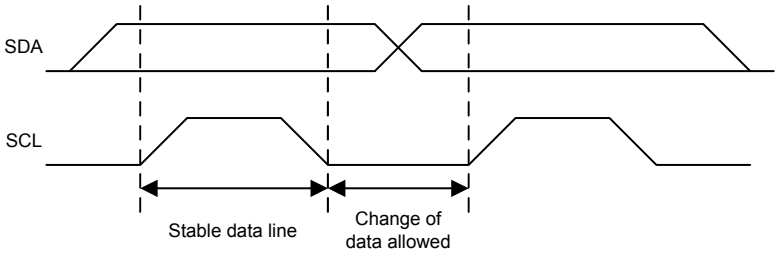


Figure 84. Data Validity

Addressing Format

The I²C interface starts to transfer data after the master device has sent the address to confirm the targeted slave device. The address frame is sent just after the START signal by master device. The addressing mode selection bit named ADRM in the I2CCR register should be defined to choose either the 7-bit or 10-bit addressing mode.

7-bits Address Format

The 7-bit address format is composed of the seven-bit length slave address, which the master device wants to communicate with a R/$\overline{W}$ bit and an ACK bit. The R/$\overline{W}$ bit defines the direction of the data transfer.

R/$\overline{W}$=0 (Write): The master transmits data to the addressed slave.

R/$\overline{W}$=1 (Read): The master receives data from the addressed slave.

The slave address can be assigned through the ADDR field in the I2CADDR register. The slave device sends back the acknowledge bit (ACK) if its slave address matches the transmitted address sent by master.

Note that it is forbidden to own the same address for two slave devices.

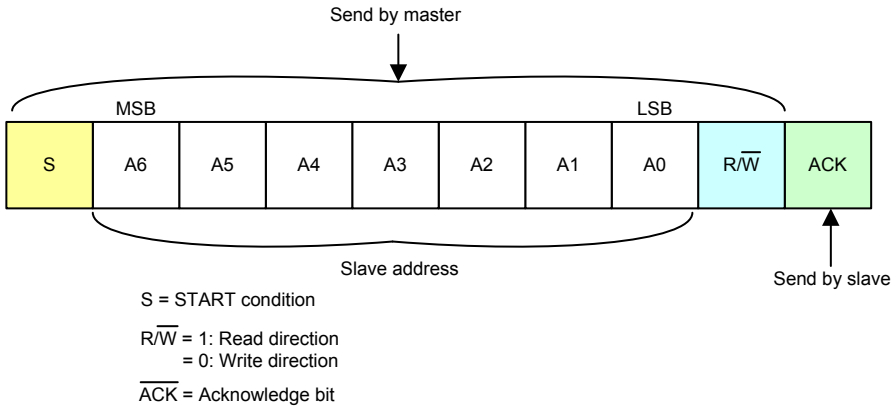


Figure 85. 7-bit Addressing Mode

10-bits Address Format

In order to prevent address clashes, due to the limited range of the 7-bit addresses, a new 10-bit address scheme has been introduced. This enhancement can be mixed with the 7-bit addressing mode which increases the available address range about ten times. For the 10-bit addressing mode, the first two bytes after a START signal include a header byte and an address byte that usually determines which slave will be selected by the master. The header byte is composed of a leading "11110", 10th and 9th bits of the slave address. The second byte is the remaining 8 bit address of the slave device.

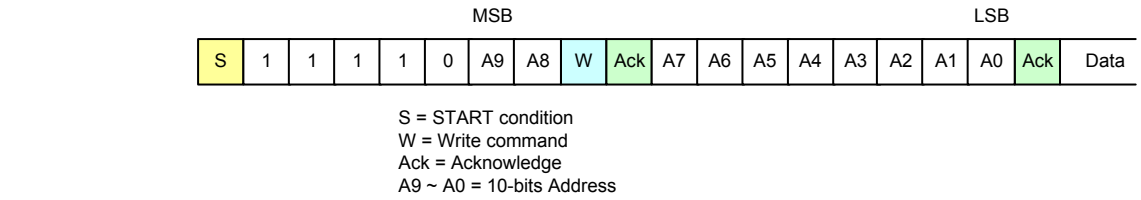


Figure 86. 10-bit Addressing Write Transmit Mode

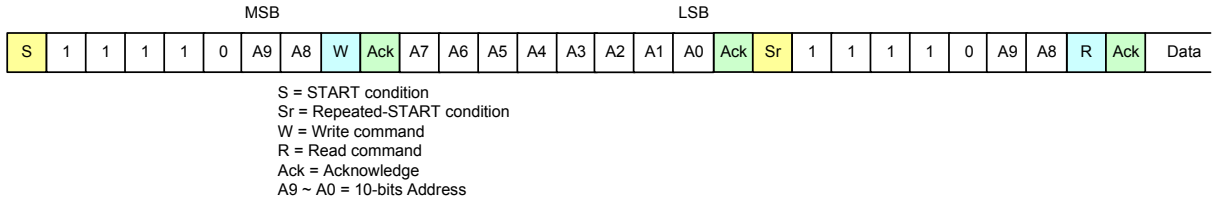


Figure 87. 10-bits Addressing Read Receive Mode

Data Transfer and Acknowledge

Once the slave device address has been matched, the data can be transmitted to or received from the slave device according to the transfer direction specified by the R/$\overline{W}$ bit. Each byte is followed by an acknowledge bit on the 9th SCL clock.

If the slave device returns a Not Acknowledge (NACK) signal to the master device, the master device can generate a STOP signal to terminate the data transfer or generate a repeated START signal to restart the transfer.

If the master device sends a Not Acknowledge (NACK) signal to the slave device, the slave device should release the SDA line for the master device to generate a STOP signal to terminate the transfer.

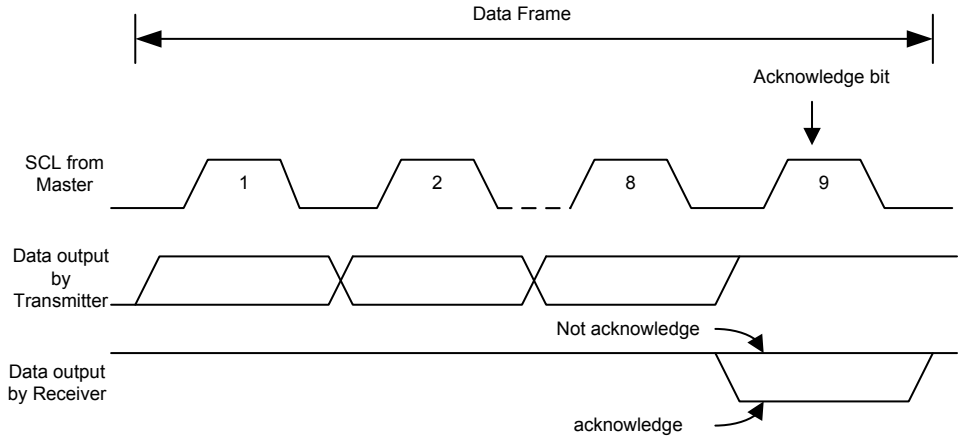


Figure 88. I²C Bus Acknowledge

Clock Synchronization

Only one master device can generate the SCL clock under normal operation. However when there is more than one master trying to generate the SCL clock, the clock should be synchronized so that the data output can be compared. Clock synchronization is performed using the wired-AND connection of the I²C interface to the SCL line.

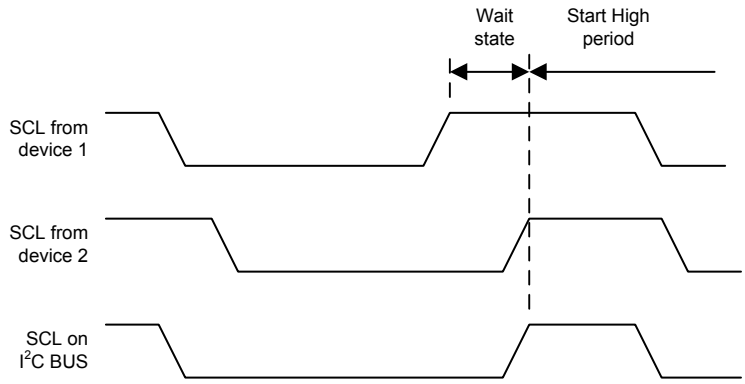


Figure 89. Clock Synchronization during Arbitration

Arbitration

A master may start a transfer only if the I²C bus line is in the free or idle mode. If two or more masters generate a START signal at approximately the same time, an arbitration procedure will occur.

Arbitration takes place on the SDA line and can continue for many bits. The arbitration procedure gives a higher priority to the device that transmits serial data with a binary low bit (logic low). Other master devices which want to transmit binary high bits (logic high) will lose the arbitration. As soon as a master loses the arbitration, the I²C module will set the ARBLOS bit in the I2CSR register and generate an interrupt if the interrupt enable bit, ARBLSIEN, in the I2CIER register is set to 1. Meanwhile, it stops sending data and listens to the bus in order to detect an I²C stop signal. When the stop signal is detected, the master which has lost the arbitration may try to access the bus again.

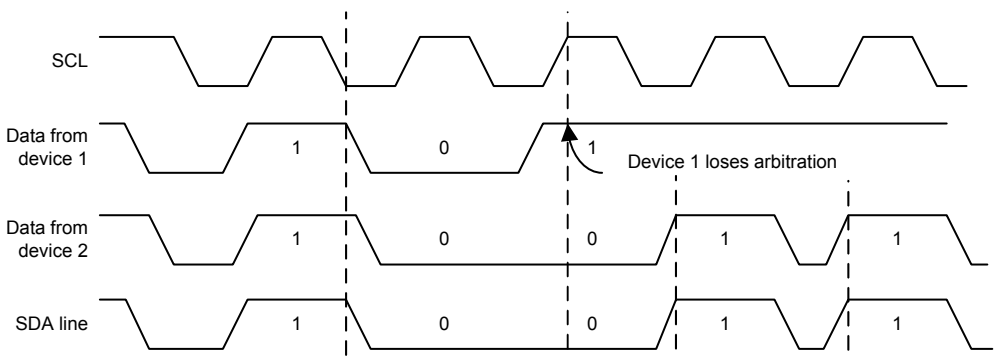


Figure 90. Two Master Arbitration Procedure

General Call Addressing

The general call addressing function can be used to address all the devices connected to the I²C bus. The master device can activate the general call function by writing a value "00" into the TAR and setting the RWD bit to 0 in the I2CTAR register on the addressing frame.

The device can support the general call addressing function by setting the corresponding enable control bit GCEN to 1. If the GCEN bit is set to 1 to support the general call addressing, the AA bit in the I2CCR register should also be set to 1 to send an acknowledge signal back when the device receives an address frame with a value of 00H. When this condition occurs, the general call flag, GCS, will be set to 1, but the ADRS flag will not be set.

Bus Error

If an unpredictable START or STOP condition occurs when the data is being transferred on the I²C bus, it will be considered as a bus error and the transferring data will be aborted. When a bus error event occurs, the relevant bus error flag BUSERR in the I2CSR register will set to 1 and both the SDA and SCL lines are released. The BUSERR flag should be cleared by writing a 1 to it to initiate the I²C module to an idle state.

Address Mask Enable

The I²C module provides address mask function for user to decide which address bit can be ignored during the comparison with the address frame sent from the master. The ADRS flag will be asserted when the unmasked address bits and the address frame sent from the master are matched. Note that this function is only available in the slave mode.

For instance, the user sets a data transfer with 7-bit addressing mode together with the I2CADDMR register value as 0x05h and the I2CADDR register value as 0x55h, this means if an address which is sent by an I²C master on the bus is equal to 0x50h, 0x51h, 0x54h or 0x55h, the I²C slave address will all be considered to be matched and the ADRS flag in the I2CSR register will be asserted after the address frame.

Address Snoop

The Address Snoop register, I2CADDSR, is used to monitor the calling address on the I²C bus during the whole data transfer operation no matter if the I²C module operates as a master or a slave device. Note that the I2CADDSR register is a read only register and each calling address on the I²C bus will be stored in the I2CADDSR register automatically even if the I²C device is not addressed.

Operation Mode

The I²C module can operate in one of the following modes:

- Master Transmitter
- Master Receiver
- Slave Transmitter
- Slave Receiver

The I²C module operates in the slave mode by default. The interface will switch to the master mode automatically after generating a START signal.

Master Transmitter Mode

Start condition

Users write the target slave device address and communication direction into the I2CTAR register after setting the I2CEN bit in the I2CCR register. The STA flag in the I2CSR register is set by hardware after a start condition occurs. In order to send the following address frame, the STA flag must be cleared to 0 if it has been set to 1. The STA flag is cleared by reading the I2CSR register.

Address Frame

The ADRS flag in the I2CSR register will be set after the address frame is sent by the master device and the acknowledge signal from the address matched slave device is received. In order to send the following data frame, the ADRS flag must be cleared to 0 if it has been set to 1. The ADRS bit is cleared by reading the I2CSR register.

Data Frame

The data to be transmitted to the slave device must be transferred to the I2CDR register.

The TXDE bit in the I2CSR register is set to indicate that the I2CDR register is empty, which results in the SCL line being held at a logic low state. New data must then be transferred to the I2CDR register to continue the data transfer process. Writing a data into the I2CDR register will clear the TXDE flag.

Close / Continue Transmission

After transmitting the last data byte, the STOP bit in the I2CCR register can be set to terminate the transmission or re-assign another slave device by configuring the I2CTAR register to restart a new transfer.

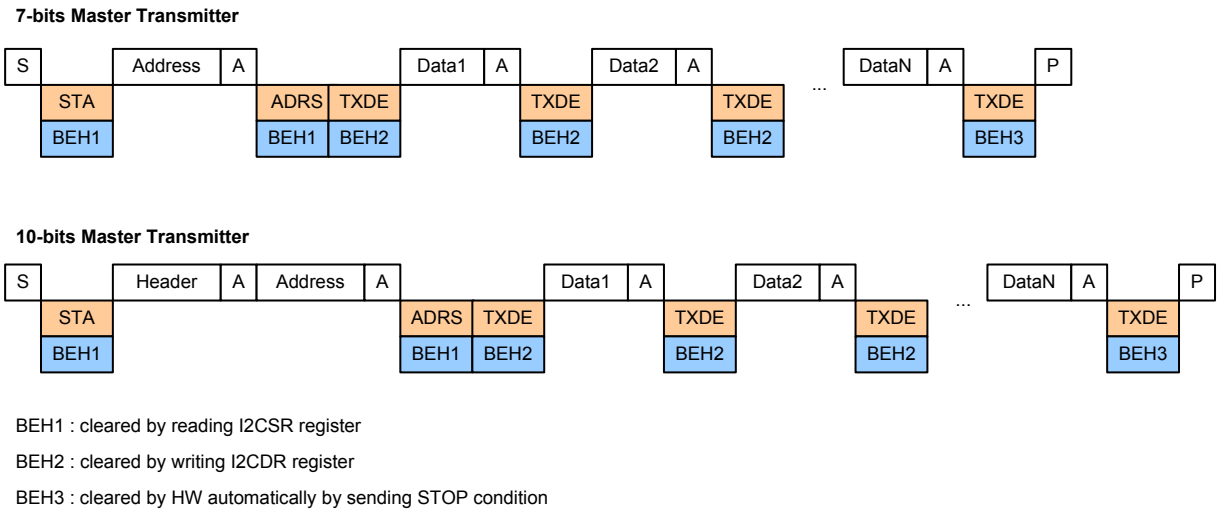


Figure 91. Master Transmitter Timing Diagram

Master Receiver Mode

Start condition

The target slave device address and communication direction must be written into the I2CTAR register. The STA flag in the I2CSR register is set by hardware after a start condition occurs. In order to send the following address frame, the STA flag must be cleared to 0 if it has been set to 1.The STA flag is cleared by reading the I2CSR register.

Address Frame

In the 7-bit addressing mode: The ADRS flag is set after the address frame is sent by the master device and the acknowledge signal from the address matched slave device is received. In order to receive the following data frame, the ADRS bit must be cleared to 0 if it has been set to 1. The ADRS bit is cleared after reading the I2CSR register.

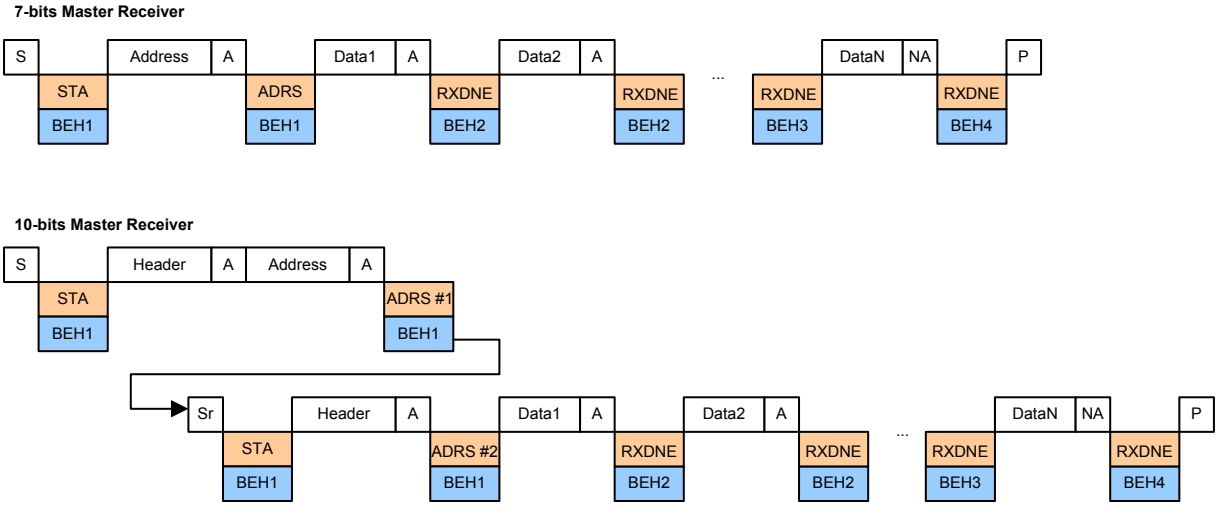
In the 10-bit addressing mode: The ADRS bit in the I2CSR register will be set twice in the 10-bit addressing mode. The first time the ADRS bit is set is when the 10-bit address is sent and the acknowledge signal from the slave device is received. The second time the ADRS bit is set is when the header byte is sent and the slave acknowledge signal is received. In order to receive the following data frame, the ADRS bit must be cleared to 0 if it has been set to 1. The ADRS bit is cleared after reading the I2CSR register. The detailed master receiver mode timing diagram is shown in the following figure.

Data Frame

In the master receiver mode, data is transmitted from the slave device. Once a data is received by the master device, the RXDNE flag in the I2CSR register is set but it will not hold the SCL line. However, if the device receives a complete new data byte and the RXDNE flag has already been set to 1, the RXBF bit in the I2CSR register will be set to 1 and the SCL line will be held at a logic low state. When this situation occurs, data from the I2CDR register should be read to continue the data transfer process. The RXDNE flag can be cleared after reading the I2CDR register.

Close / Continue Transmission

The master device needs to reset the AA bit in the I2CCR register to send a NACK signal to the slave device before the last data byte transfer has been completed. After the last data byte has been received from the slave device, the master device will hold the SCL line at a logic low state following after a NACK signal sent by the master device to the slave device. The STOP bit can be set to terminate the data transfer process or re-assign the I2CTAR register to restart a new transfer.



BEH1 : cleared by reading I2CSR register

BEH2 : cleared by reading I2CDR register

BEH3 : cleared by reading I2CDR register, set AA=0 to send NACK signal

BEH4 : cleared by reading I2CDR register, set STOP=1 to send STOP signal

Figure 92. Master Receiver Timing Diagram

Slave Transmitter Mode

Address Frame

In the 7-bit addressing mode, the ADRS bit in the I2CSR register is set after the slave device receives the calling address which matches with the slave device address. In the 10-bit addressing mode, the ADRS bit is set when the first header byte is matched and the second address byte is matched respectively. After the ADRS bit has been set to 1, it must be cleared to 0 to continue the data transfer process. The ADRS bit is cleared after reading the I2CSR register.

Data Frame

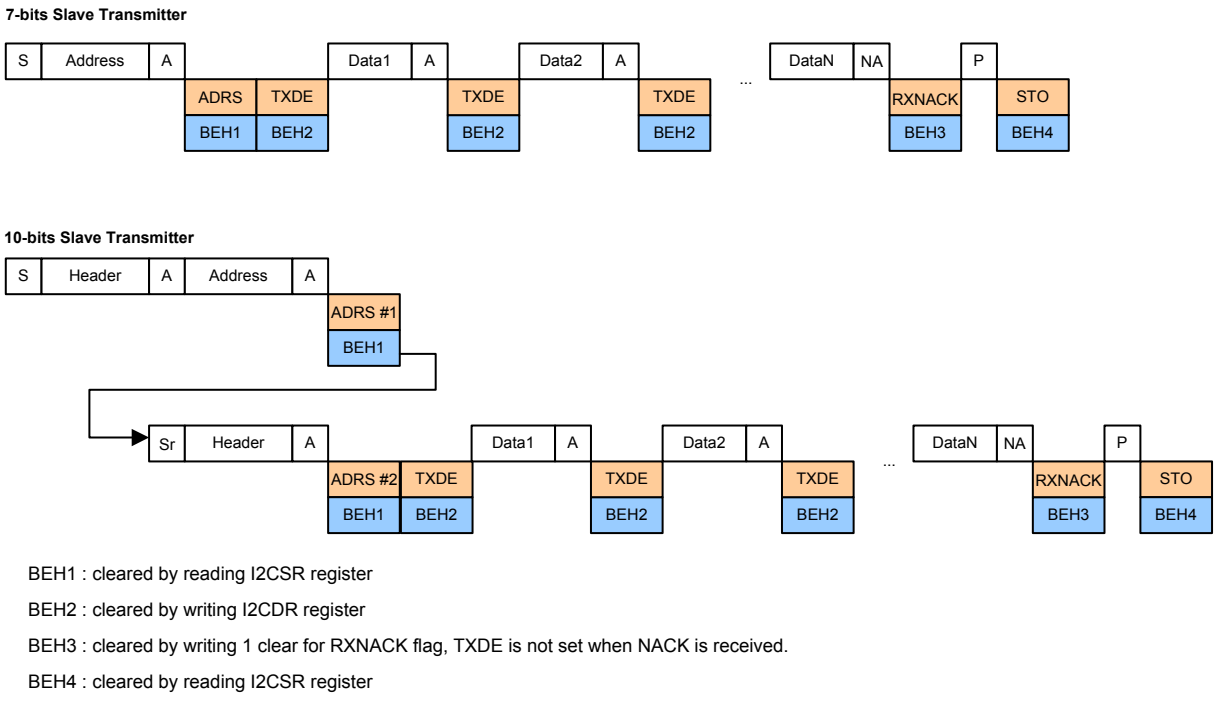
In the Slave transmitter mode, the TXDE bit is set to indicate that the I2CDR is empty, which results in the SCL line being held at a logic low state. New transmission data must then be written into the I2CDR register to continue the data transfer process. Writing a data into the I2CDR register will clear the TXDE bit.

Receive Not-Acknowledge

When the slave device receives a Not-Acknowledge signal, the RXNACK bit in the I2CSR Register is set but it will not hold the SCL line. Writing "1" to RXNACK will clear the RXNACK flag.

STOP Condition

When the slave device detects a STOP condition, the STO bit in the I2CSR register is set to indicate that the I^2C interface transmission is terminated. Reading the I2CSR register can clear the STO flag.



BEH1 : cleared by reading I2CSR register

BEH2 : cleared by writing I2CDR register

BEH3 : cleared by writing 1 clear for RXNACK flag, TXDE is not set when NACK is received.

BEH4 : cleared by reading I2CSR register

Figure 93. Slave Transmitter Timing Diagram

Slave Receiver Mode

Address Frame

The ADRS bit in the I2CSR register is set after the slave device receives the calling address which matches with the slave device address. After the ADRS bit has been set to 1, it must be cleared to 0 to continue the data transfer process. The ADRS flag is cleared after reading the I2CSR register.

Data Frame

In the slave receiver mode, the data is transmitted from the master device. Once a data byte is received by the slave device, the RXDNE flag in the I2CSR register is set but it will not hold the SCL line. However, if the device receives a complete new data byte and the RXDNE bit has been set to 1, the RXBF bit in the I2CSR register will be set to 1 and the SCL line will be held at a logic low state. When this situation occurs, data from the I2CDR register should be read to continue the data transfer process. The RXDNE flag bit can be cleared after reading the I2CDR register.

STOP condition

When the slave device detects a STOP condition, the STO flag bit in the I2CSR register is set to indicate that the I²C interface transmission is terminated. Reading the I2CSR register can clear the STO flag bit.

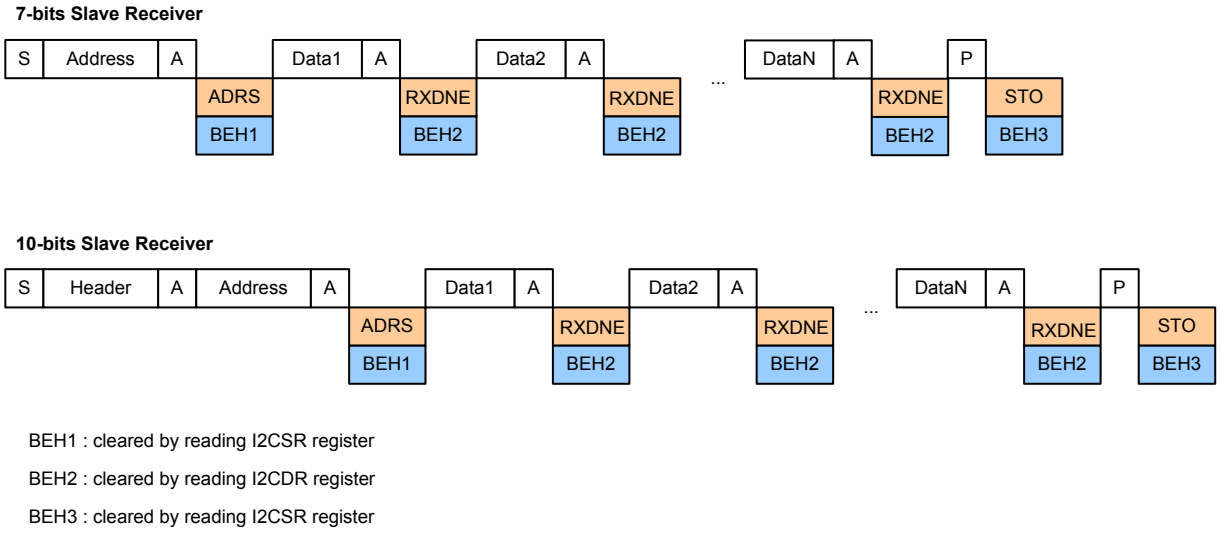


Figure 94. Slave Receiver Timing Diagram

Conditions of Holding SCL Line

The following conditions will cause the SCL line to be held at a logic low state by hardware resulting in all the I²C transfers being stopped. Data transfer will be continued after the creating conditions are eliminated.

Table 37. Conditions of Holding SCL line

Type	Condition	Description	Eliminated
Flag	TXDE	I²C is used in transmitted mode and I2CDR register needs to have data to transmit. (Note: TXDE won't be assert after receiving a NACK)	Master case: Writing data to I2CDR register Set TAR Set STOP Slave case: Writing data to I2CDR register
	GCS	I²C is addressed as slave through general call	Reading I2CSR register
	ADRS	Master: I²C is sent over address frame and is returned an ACK from slave (Note: Reference Fig.95 and Fig.96) Slave: I²C is addressed as slave device (Note: Reference Fig.97 and Fig.98)	Reading I2CSR register
	STA	Master send START signal	Reading I2CSR register
	RXBF	Received a complete new data and meanwhile the RXDNE flag has been set already before.	Reading I2CDR register
Event	Master receives NACK	No matter in address or data frame, once received a NACK signal will hold SCL line in master mode.	Set TAR Set STOP
	Master sends NACK used in received mode	Occurred when receiving the last data byte in Master received mode (Note: Reference Fig.95, and RXNACK flag won't be assert at this case)	Set TAR Set STOP

I²C Timeout Function

In order to reduce the occurrence of I²C lockup problem due to the reception of erroneous clock source, a timeout function is provided. If the I²C bus clock source is not received for a certain timeout period, then a corresponding I²C timeout flag will be asserted. This timeout period is determined by a 16-bit down-counting counter with a programmable preload value. The timeout counter is driven by the I²C timeout clock, f_{I2CTO}, which is specified by the timeout prescaler field in the I2CTOUT register. The TOUT field in the I2CTOUT register is used to define the timeout counter preload value. The timeout function is enabled by setting the ENTOUT bit in the I2CCR register. The timeout counter will start to count down from the preloaded value if the ENTOUT bit is set to 1 and one of the following conditions occurs:

- The I²C master module sends a START signal.
- The I²C slave module detects a START signal.
- The RXBF, TXDE, RXDNE, RXNACK, GCS or ADRS flags are asserted.

The timeout counter will stop counting when the ENTOUT bit is cleared. However, the counter will also stop counting when the conditions, listed as follows occur:

- The I²C slave module is not addressed.
- The I²C slave module detects a STOP signal.
- The I²C master module sends a STOP signal.
- The ARBLOS or BUSERR flags in the I2CSR register are asserted.

If the timeout counter underflows, the corresponding timeout flag, TOUTF, in the I2CSR register will be set to 1 and a timeout interrupt will be generated if the relevant interrupt is enabled.

Register Map

The following table shows the I²C registers and reset values.

Table 38. I²C Register Map

Register	Offset	Description	Reset Value
I2CCR	0x000	I²C Control Register	0x0000_2000
I2CIER	0x004	I²C Interrupt Enable Register	0x0000_0000
I2CADDR	0x008	I²C Address Register	0x0000_0000
I2CSR	0x00C	I²C Status Register	0x0000_0000
I2CSHPGR	0x010	I²C SCL High Period Generation Register	0x0000_0000
I2CSLPGR	0x014	I²C SCL Low Period Generation Register	0x0000_0000
I2CDR	0x018	I²C Data Register	0x0000_0000
I2CTAR	0x01C	I²C Target Register	0x0000_0000
I2CADDMR	0x020	I²C Address Mask Register	0x0000_0000
I2CADDSR	0x024	I²C Address Snoop Register	0x0000_0000
I2CTOUT	0x028	I²C Timeout Register	0x0000_0000

Register Descriptions

I²C Control Register – I2CCR

This register specifies the corresponding I²C function enable control.

Offset: 0x000 (0)
Reset value: 0x0000_2000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	SEQFILTER		COMBFILTEREn	ENTOUT	Reserved			
Type/Reset	RW	0 RW 0	RW	1 RW 0				
	7	6	5	4	3	2	1	0
	ADRM	Reserved			I2CEN	GCEN	STOP	AA
Type/Reset	RW	0			RW	0 RW 0	RW	0 RW 0

Bits	Field	Descriptions
[15:14]	SEQFILTER	SDA or SCL Input Sequential Filter Configuration Bits 00: Sequential filter disable 01: 1 PCLK glitch filter 1x: 2 PCLK glitch filter Note: This setting would affect the frequency of SCL. Detail is described in I2CSLPGR register.
[13]	COMBFILTEREn	SDA or SCL Input Combinational Filter Enable Bit 0: Combinational filter Disable 1: Combinational filter Enable
[12]	ENTOUT	I²C Timeout Function Enable Control 0: Timeout Function disabled 1: Timeout Function enabled This bit is used to enable or disable the I²C timeout function. When the I2CEN bit is cleared to 0, the ENTOUT bit will be automatically cleared to 0 by hardware. It is recommended that users have to properly configure the PSC and TOUT fields in the I2CTOUT register before the timeout counter starts to count by setting the ENOUT bit to 1.
[7]	ADRM	Addressing Mode 0: 7-bit addressing mode 1: 10-bit addressing mode When the I²C master/slave module operates in the 7-bit addressing mode, it can only send out and respond to a 7-bit address and vice versa. When the I2CEN bit is disabled, the ADRM bit is automatically cleared to 0 by hardware.
[3]	I2CEN	I²C Interface Enable 0: I²C interface disabled 1: I²C interface enabled

Bits	Field	Descriptions
[2]	GCEN	General Call Enable 0: General call disabled 1: General call enabled When the device receives the calling address with a value of 0x00 and if both the GCEN and the AA bits are set to 1, then the I²C interface is addressed as a slave and the GCS bit in the I2CSR register is set to 1. When the I2CEN bit is cleared to 0, the GCEN bit is automatically cleared to 0 by hardware.
[1]	STOP	STOP Condition Control 0: No action 1: Send a STOP condition in master mode This bit is set to 1 by software to generate a STOP condition and automatically cleared to 0 by hardware. The STOP bit is only available for the master device.
[0]	AA	Acknowledge Bit 0: Send a Not Acknowledge (NACK) signal after a byte is received 1: Send an Acknowledge (ACK) signal after a byte is received When the I2CEN bit is cleared to 0, the AA bit is automatically cleared to 0 by hardware.

I²C Interrupt Enable Register – I2CIER

This register specifies the corresponding I²C interrupt enable bits.

Offset: 0x004

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved					RXBFIE	TXDEIE	RXDNEIE
Type/Reset						RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
	Reserved				TOUTIE	BUSERRIE	RXNACKIE	ARBLOSIE
Type/Reset					RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	Reserved				GCSIE	ADRSIE	STOIE	STAIE
Type/Reset					RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[18]	RXBFIE	RX Buffer Full Interrupt Enable Bit 0: Interrupt disabled 1: Interrupt enabled When the I2CEN bit in the I2CCR register is cleared to 0, this bit is cleared to 0 by hardware.
[17]	TXDEIE	Data Register Empty Interrupt Enable Bit in Transmitter Mode 0: Interrupt disabled 1: Interrupt enabled When the I2CEN bit in the I2CCR register is cleared to 0, this bit is cleared to 0 by hardware.

Bits	Field	Descriptions
[16]	RXDNEIE	Data Register Not Empty Interrupt Enable Bit in Received Mode 0: Interrupt disabled 1: Interrupt enabled When the I2CEN bit in the I2CCR register is cleared to 0, this bit is cleared to 0 by hardware.
[11]	TOUTIE	Timeout Interrupt Enable Bit 0: Interrupt disabled 1: Interrupt enabled When the I2CEN bit in the I2CCR register is cleared to 0, this bit is cleared to 0 by hardware.
[10]	BUSERRIE	Bus Error Interrupt Enable Bit 0: Interrupt disabled 1: Interrupt enabled When the I2CEN bit in the I2CCR register is cleared to 0, this bit is cleared to 0 by hardware.
[9]	RXNACKIE	Received Not Acknowledge Interrupt Enable Bit 0: Interrupt disabled 1: Interrupt enabled When the I2CEN bit in the I2CCR register is cleared to 0, this bit is cleared to 0 by hardware.
[8]	ARBLOSIE	Arbitration Loss Interrupt Enable Bit in the I^2C multi-master mode 0: Interrupt disabled 1: Interrupt enabled When the I2CEN bit in the I2CCR register is cleared to 0, this bit is cleared to 0 by hardware.
[3]	GCSIE	General Call Slave Interrupt Enable Bit 0: Interrupt disabled 1: Interrupt enabled When the I2CEN bit in the I2CCR register is cleared to 0, this bit is cleared to 0 by hardware.
[2]	ADRSIE	Slave Address Match Interrupt Enable Bit 0: Interrupt disabled 1: Interrupt enabled When the I2CEN bit in the I2CCR register is cleared to 0, this bit is cleared to 0 by hardware.
[1]	STOIE	STOP Condition Detected Interrupt Enable Bit 0: Interrupt disabled 1: Interrupt enabled When the I2CEN bit in the I2CCR register is cleared to 0, this bit is cleared to 0 by hardware. The bit is used for the I^2C slave mode only.
[0]	STAIE	START Condition Transmit Interrupt Enable Bit 0: Interrupt disabled 1: Interrupt enabled When the I2CEN bit in the I2CCR register is cleared to 0, this bit is cleared to 0 by hardware. The bit is used for the I^2C master mode only.

I²C Address Register – I2CADDR

This register specifies the I²C device address.

Offset: 0x008

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved						ADDR	
Type/Reset							RW 0	RW 0
	7	6	5	4	3	2	1	0
	ADDR							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[9:0]	ADDR	Device Address The register indicates the I²C device address. When the I²C device is used in the 7-bit addressing mode, only the ADDR[6:0] bits will be compared with the received address sent from the I²C master device.

I²C Status Register – I2CSR

This register contains the I²C operation status.

Offset: 0x00C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
		Reserved	TXNRX	MASTER	BUSBUSY	RXBF	TXDE	RXDNE
Type/Reset			RO 0	RO 0	RO 0	RO 0	RO 0	RO 0
	15	14	13	12	11	10	9	8
	Reserved				TOUTF	BUSERR	RXNACK	ARBLOS
Type/Reset					WC 0	WC 0	WC 0	WC 0
	7	6	5	4	3	2	1	0
	Reserved				GCS	ADRS	STO	STA
Type/Reset					RC 0	RC 0	RC 0	RC 0

Bits	Field	Descriptions
[21]	TXNRX	Transmitter / Receiver Mode 0: Receiver mode 1: Transmitter mode Read only bit.
[20]	MASTER	Master Mode 0: I²C is in the slave mode or idle 1: I²C is in the master mode The I²C interface is switched as a master device on the I²C bus when the I2CTAR register is assigned and the I²C bus is idle. The MASTER bit is cleared by hardware when software disables the I²C bus by clearing the I2CEN bit to 0 or sends a STOP condition to the I²C bus or the bus error is detected. This bit is set and cleared by hardware and is a read only bit.
[19]	BUSBUSY	Bus Busy 0: I²C bus is idle 1: I²C bus is busy The I²C interface hardware starts to detect the I²C bus status if the interface is enabled by setting the I2CEN bit to 1. It is set to 1 when the SDA or SCL signal is detected to have a logic low state and cleared when a STOP condition is detected.
[18]	RXBF	Buffer Full Flag in Receiver Mode 0: Data buffer is not full 1: Data buffer is full This bit is set when the data register I2CDR has already stored a data byte and meanwhile the data shift register also has been received a complete new data byte. The RXBF bit is cleared by software reading the I2CDR register.

Bits	Field	Descriptions
[17]	TXDE	Data Register Empty Using in Transmitter Mode 0: Data register I2CDR not empty 1: Data register I2CDR empty This bit is set when the I2CDR register is empty in the Transmitter mode. Note that the TXDE bit will be set after the address frame is being transmitted to inform that the data to be transmitted should be loaded into the I2CDR register. The TXDE bit is cleared by software writing data to the I2CDR register in both the master and slave mode or cleared automatically by hardware after setting the STOP signal to terminate the data transfer or setting the I2CTAR register to restart a new data transfer in the master mode.
[16]	RXDNE	Data Register Not Empty in Receiver Mode 0: Data register I2CDR empty 1: Data register I2CDR not empty This bit is set when the I2CDR register is not empty in the receiver mode. The RXDNE bit is cleared by software reading the data byte from the I2CDR register.
[11]	TOUTF	Timeout Counter Underflow Flag 0: No timeout counter underflow occurred 1: Timeout counter underflow occurred Writing “1” to this bit will clear the TOUTF flag.
[10]	BUSERR	Bus Error Flag 0: No bus error has occurs 1: Bus error has occurred This bit is set by hardware when the I^2C interface detects a misplaced START or STOP condition in a transfer process. Writing a “1” to this bit will clear the BUSERR flag. In Master Mode: Once the Bus Error event occurs, both the SDA and SCL lines are released by hardware and the BUSERR flag is asserted. The application software has to clear the BUSERR flag before the next address byte is transmitted. In Slave Mode: Once a misplaced START or STOP condition has been detected by the slave device, the software must clear the BUSERR flag before the next address byte is received.
[9]	RXNACK	Received Not Acknowledge Flag 0: Acknowledge is returned from receiver 1: Not Acknowledge is returned from receiver The RXNACK bit indicates that the not Acknowledge signal is received in master or slave transmitter mode. Writing “1” to this bit will clear the RXNACK flag.
[8]	ARBLOS	Arbitration Loss Flag 0: No arbitration loss is detected 1: Bit arbitration loss is detected This bit is set by hardware on the current clock which the I^2C interface loses the bus arbitration to another master during the address or data frame transmission. Writing “1” to this bit will clear the ARBLOS flag. Once the ARBLOS flag is asserted by hardware, the ARBLOS flag must be cleared before the next transmission.
[3]	GCS	General Call Slave Flag 0: No general call slave occurs 1: I^2C interface is addressed by a general call command When the I^2C interface receives an address with a value of 0x00 or 0x000 in the 7-bit or 10-bit addressing mode, if both the GCEN and the AA bit are set to 1, then it is switched as a general call slave. This flag is cleared automatically after being read.

Bits	Field	Descriptions
[2]	ADRS	Address Transmit (master mode) / Address Receive (slave mode) Flag Address Sent in Master Mode 0: Address frame has not been transmitted 1: Address frame has been transmitted For the 7-bit addressing mode, this bit is set after the master device receives the address frame acknowledge bit sent from the slave device. For the 10-bit addressing mode, this bit is set after receiving the acknowledge bit of the first header byte and the second address. Address Matched in Slave Mode 0: I^2C interface is not addressed 1: I^2C interface is addressed as slave When the I^2C interface has received the calling address that matches the address defined in the I2CADDR register together with the AA bit being set to 1 in the I2CCR register, it will be switched to a slave mode. This flag is cleared automatically after the I2CSR register has been read.
[1]	STO	STOP Condition Detected Flag 0: No STOP condition detected 1: STOP condition detected in slave mode This bit is only available for the slave mode and is cleared automatically after the I2CSR register is read.
[0]	STA	START Condition Transmit 0: No START condition detected 1: START condition is transmitted in master mode This bit is only available for the master mode and is cleared automatically after the I2CSR register is read.

I²C SCL High Period Generation Register – I2CSHPGR

This register specifies the I²C SCL clock high period interval.

Offset: 0x010

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	SHPG							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	SHPG							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	SHPG	SCL Clock High Period Generation High period duration setting $SCL_{HIGH} = T_{PCLK} \times (SHPG + d)$ where T_{PCLK} is the APB bus peripheral clock (PCLK) period of the I²C, and d value depends on the setting of the SEQFILTER in the I²C Control Register (I2CCR). If SEQFILTER=00, d=6 If SEQFILTER=01, d=8 If SEQFILTER=10 or 11, d=9

I²C SCL Low Period Generation Register – I2CSLPGR

This register specifies the I²C SCL clock low period interval.

Offset: 0x014

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	SLPG							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	SLPG							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	SLPG	SCL Clock Low Period Generation Low period duration setting SCL_{LOW} = T_{PCLK} × (SLPG + d) where T_{PCLK} is the APB bus peripheral clock (PCLK) period of I²C, and d value depends on the setting of the SEQFILTER in the I²C Control Register (I2CCR). If SEQFILTER=00, d=6 If SEQFILTER=01, d=8 If SEQFILTER=10 or 11, d=9

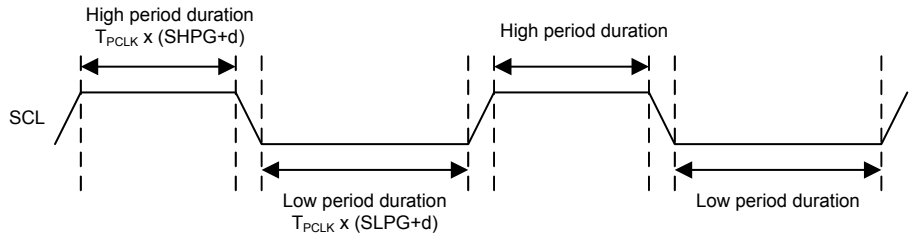


Figure 95. SCL Timing Diagram

Table 39. I²C Clock Setting Example

I²C Clock	$T_{SCL} = T_{PCLK} \times [(SHPG + d) + (SLPG + d)]$ (where d = 6) SHPG + SLPG value at PCLK			
	8 MHz	20 MHz	24 MHz	40 MHz
100 kHz (Standard Mode)	68	188	228	388
400 kHz (Fast Mode)	8	38	48	88
1 MHz (Fast Mode Plus)	N/A	8	12	28

I²C Data Register – I2CDR

This register specifies the data to be transmitted or received by the I²C module.

Offset: 0x018

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	DATA							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[7:0]	DATA	I²C Data Register For the transmitter mode, a data byte which is transmitted to a slave device can be assigned to these bits. The TXDE flag is cleared if the application software assigns new data to the I2CDR register. For the receiver mode, a data byte is received bit by bit from MSB to LSB through the I²C interface and stored in the data shift register. Once the acknowledge bit is given, the data shift register value is delivered into the I2CDR register if the RXDNE flag is equal to 0.

I²C Target Register – I2CTAR

This register specifies the target device address to be communicated.

Offset: 0x01C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved					RWD	TAR	
Type/Reset						RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	TAR							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[10]	RWD	Read or Write Direction 0: Write direction to target slave address 1: Read direction from target slave address If this bit is set to 1 in the 10-bit master receiver mode, the I²C interface will initiate a byte with a value of 11110XX0b in the first header frame and then continue to deliver a byte with a value of 11110XX1b in the second header frame by hardware automatically.
[9:0]	TAR	Target Slave Address The I²C interface will assign a START signal and send a target slave address automatically once the data is written to this register. When the system wants to send a repeated START signal to the I²C bus, the timing is suggested to set the I2CTAR register after a byte transfer is completed. It is not allowed to set TAR in the address frame. I2CTAR[9:7] is not available under the 7-bit addressing mode.

I²C Address Mask Register – I2CADDMR

This register specifies which bit of the I²C address is masked and not compared with corresponding bit of the received address frame.

Offset: 0x020

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved						ADDMR	
Type/Reset							RW 0	RW 0
	7	6	5	4	3	2	1	0
	ADDMR							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[9:0]	ADDMR	Address Mask Control Bit The ADDMR[i] is used to specify whether the i^{th} bit of the ADDMR in the I2CADDMR register is masked and is compared with the received address frame or not on the I²C bus. The register is only used for the I²C slave mode only. 0: i^{th} bit of the ADDMR is compared with the address frame on the I²C bus. 1: i^{th} bit of the ADDMR is masked and not compared with the address frame on the I²C bus.

I²C Address Snoop Register – I2CADDSR

This register is used to indicate the address frame value appeared on the I²C bus.

Offset: 0x024

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved						ADDSR	
Type/Reset							RO 0	RO 0
	7	6	5	4	3	2	1	0
	ADDSR							
Type/Reset	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0	RO 0

Bits	Field	Descriptions
[9:0]	ADDSR	Address Snoop Once the I2CEN bit is enabled, the calling address value on the I²C bus will automatically be loaded into this ADDSR field.

I²C Timeout Register – I2CTOUT

This register specifies the I²C Timeout counter preload value and clock prescaler ratio.

Offset: 0x028

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved					PSC		
Type/Reset						RW 0	RW 0	RW 0
	15	14	13	12	11	10	9	8
	TOUT							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	TOUT							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[18:16]	PSC	I²C Time-out Counter Prescaler Selection This PSC field is used to specify the I²C time-out counter clock frequency, f_{I2CTO}. The time-out clock frequency is obtained using the formula. $f_{I2CTO} = \frac{f_{PCLK}}{2^{PSC}}$ PSC=0 → $f_{I2CTO} = f_{PCLK} / 2^0 = f_{PCLK}$ PSC=1 → $f_{I2CTO} = f_{PCLK} / 2^1 = f_{PCLK} / 2$ PSC=2 → $f_{I2CTO} = f_{PCLK} / 2^2 = f_{PCLK} / 4$ … PSC=7 → $f_{I2CTO} = f_{PCLK} / 2^7 = f_{PCLK} / 128$
[15:0]	TOUT	I²C Timeout Counter Preload Value The TOUT field is used to define the counter preloaded value The counter value is reloaded as the following conditions occur: 1. The RXBF, TXDE, RXDNE, RXNACK, GCS or ADRS flag in the I2CSR register is asserted. 2. The I²C master module sends a START signal. 3. The I²C slave module detects a START signal. The counter stops counting as the following conditions occur: 1. The I²C slave device is not addressed. 2. The I²C master module sends a STOP signal. 3. The I²C slave module detects a STOP signal. 4. The ARBLOS or BUSERR flag in the I2CSR register is asserted.

18 Serial Peripheral Interface (SPI)

Introduction

The Serial Peripheral Interface, SPI, provides an SPI protocol data transmit and receive functions in both master or slave mode. The SPI interface uses 4 pins, among which are serial data input and output lines MISO and MOSI, the clock line SCK, and the slave select line SEL. One SPI device acts as a master who controls the data flow using the SEL and SCK signals to indicate the start of the data communication and the data sampling rate. To receive the data bits, the streamlined data bits which range from 1 bit to 16 bits specified by the DFL field in the SPICR1 register are latched in a specific clock edge and stored in the data register or in the RX FIFO. Data transmission is carried in a similar way but with the reverse sequence. The mode fault detection provides a capability for multi-master applications.

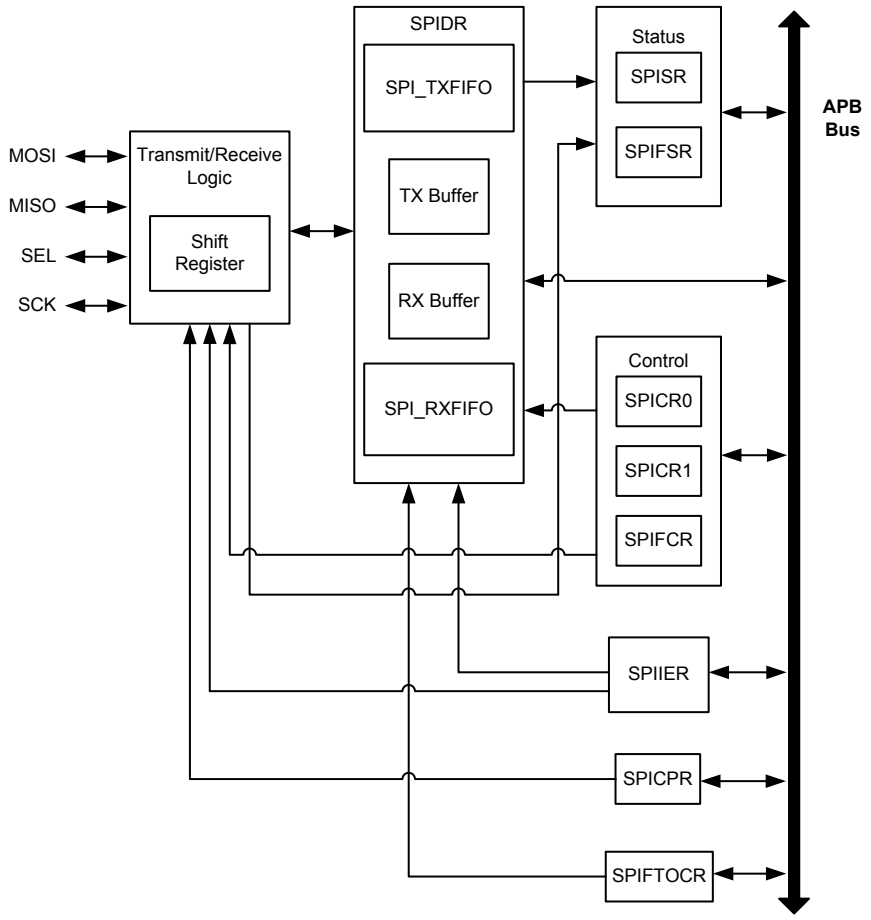


Figure 96. SPI Block Diagram

Features

- Master or slave mode
- Master mode speed up to $f_{PCLK}/2$
- Slave mode speed up to $f_{PCLK}/3$
- Programmable data frame length up to 16 bits
- FIFO Depth: 8 levels
- MSB or LSB first shift selection
- Programmable slave select high or low active polarity
- Multi-master and multi-slave operation
- Master mode supports the dual output read mode of SPI NOR Flash
- Four error flags with individual interrupt
  - Read overrun
  - Write collision
  - Mode fault
  - Slave abort

Function Descriptions

Master Mode

Each data frame can range from 1 to 16 bits in data length. The first bit of the transmitted data can be either an MSB or LSB determined by the FIRSTBIT bit in the SPICR1 register. The SPI module is configured as a master or a slave by setting the MODE bit in the SPICR1 register. When the MODE bit is set, the SPI module is configured as a master and will generate the serial clock on the SCK pin. The data stream will transmit data in the shift register to the MOSI pin on the serial clock edge. The SEL pin is active during the full data transmission. When the SELAP bit in the SPICR1 register is set, the SEL pin is active high during the complete data transactions. When the SELM bit in the SPICR1 register is set, the SEL pin will be driven by the hardware automatically and the time interval between the active SEL edge and the first edge of SCK is equal to half an SCK period.

Slave Mode

In the slave mode, the SCK pin acts as an input pin and the serial clock will be derived from the external master device. The SEL pin also acts as an input. When the SELAP bit is cleared to 0, the SEL signal is active low during the full data stream reception. When the SELAP bit is set to 1, the SEL signal will be active high during the full data stream byte reception.

Note: For the slave mode, the APB clock, known as f_{PCLK}, must be at least 3 times faster than the external SCK clock input frequency.

SPI Serial Frame Format

The SPI interface format is base on the Clock Polarity, CPOL, and the Clock Phase, CPHA, configurations.

- Clock Polarity Bit – CPOL
  When the Clock Polarity bit is cleared to 0, the SCK line idle state is LOW. When the Clock Polarity bit is set to 1, the SCK line idle state is HIGH.
- Clock Phase Bit – CPHA
  When the Clock Phase bit is cleared to 0, the data is sampled on the first SCK clock transition. When the Clock Phase bit is set to1, the data is sampled on the second SCK clock transition.

There are four formats contained in the SPI interface. Table 40 shows how to configure these formats by setting the FORMAT field in the SPICR1 register.

Table 40. SPI Interface Format Setup

FORMAT [2:0]	CPOL	CPHA
001	0	0
010	0	1
110	1	0
101	1	1
Others	Reserved	

CPOL = 0, CPHA = 0

In this format, the received data is sampled on the SCK line rising edge while the transmitted data is changed on the SCK line falling edge. In the master mode, the first bit is driven when data is written into the SPIDR Register. In the slave mode, the first bit is driven when the SEL signal goes to an active level. Figure 100 shows the single byte data transfer timing of this format.

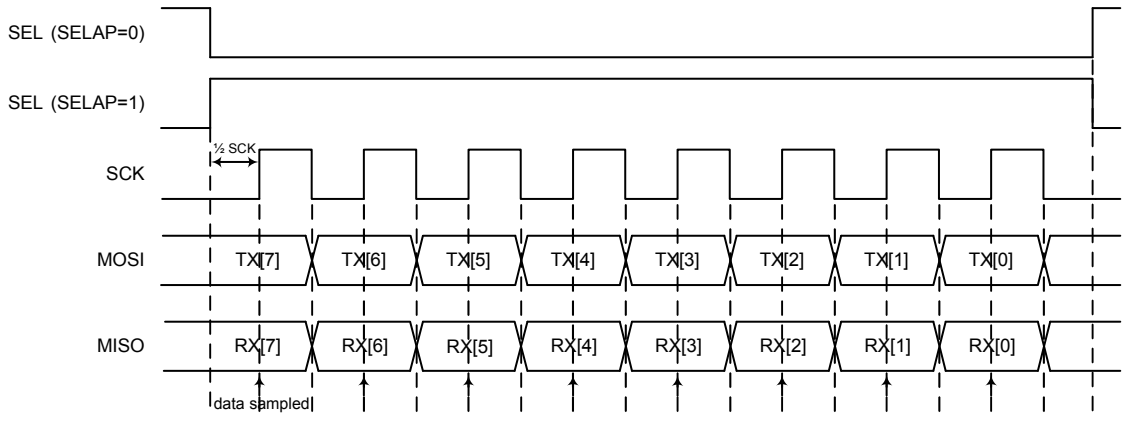


Figure 97. SPI Single Byte Transfer Timing Diagram – CPOL = 0, CPHA = 0

Figure 101 shows the continuous data transfer timing diagram of this format. Note that the SEL signal must change to an inactive level between each data frame.

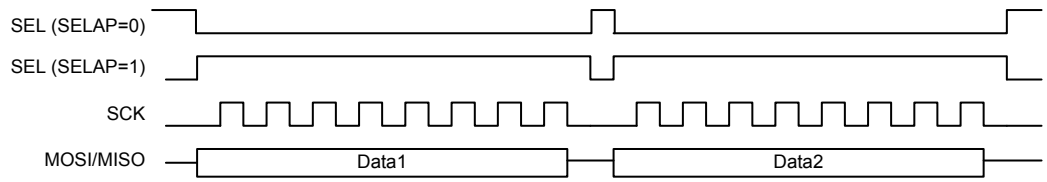


Figure 98. SPI Continuous Data Transfer Timing Diagram – CPOL = 0, CPHA = 0

CPOL = 0, CPHA = 1

In this format, the received data is sampled on the SCK line falling edge while the transmitted data is changed on the SCK line rising edge. In the master mode, the first bit is driven when data is written into the SPIDR register. In the slave mode, the first bit is driven at the first SCK clock rising edge. Figure 102 shows the single data byte transfer timing.

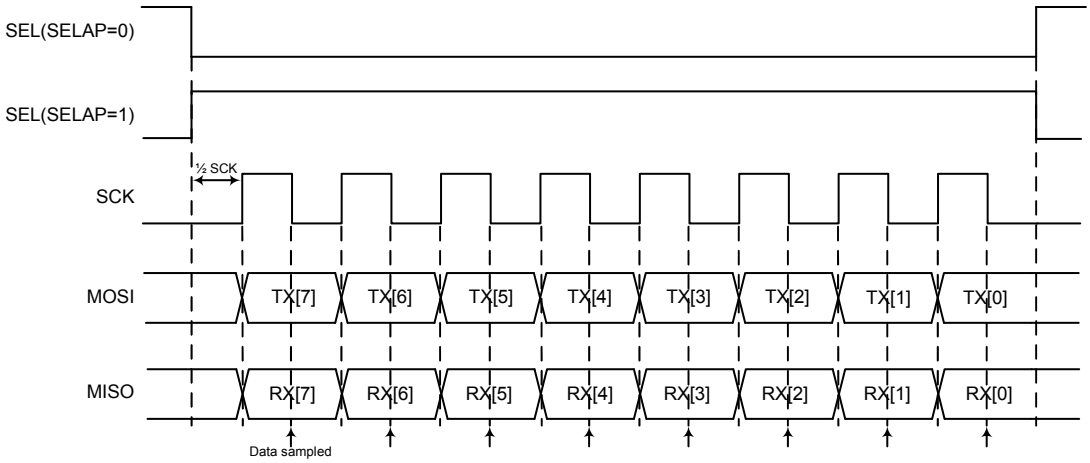


Figure 99. SPI Single Byte Transfer Timing Diagram – CPOL = 0, CPHA = 1

Figure 103 shows the continuous data transfer diagram timing. Note that the SEL signal must remain active until the last data transfer has completed.

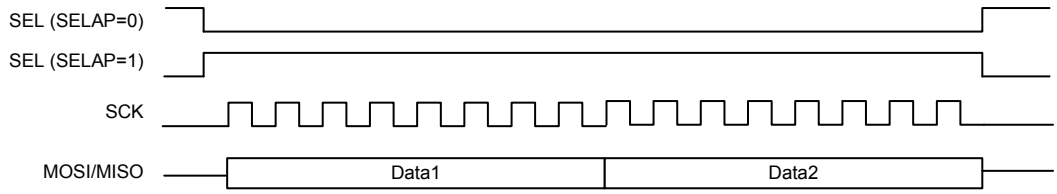


Figure 100. SPI Continuous Transfer Timing Diagram – CPOL = 0, CPHA = 1

CPOL = 1, CPHA = 0

In this format, the received data is sampled on the SCK line falling edge while the transmitted data is changed on the SCK line rising edge. In the master mode, the first bit is driven when data is written into the SPIDR register. In the slave mode, the first bit is driven when the SEL signal changes to an active level. Figure 104 shows the single byte transfer timing of this format.

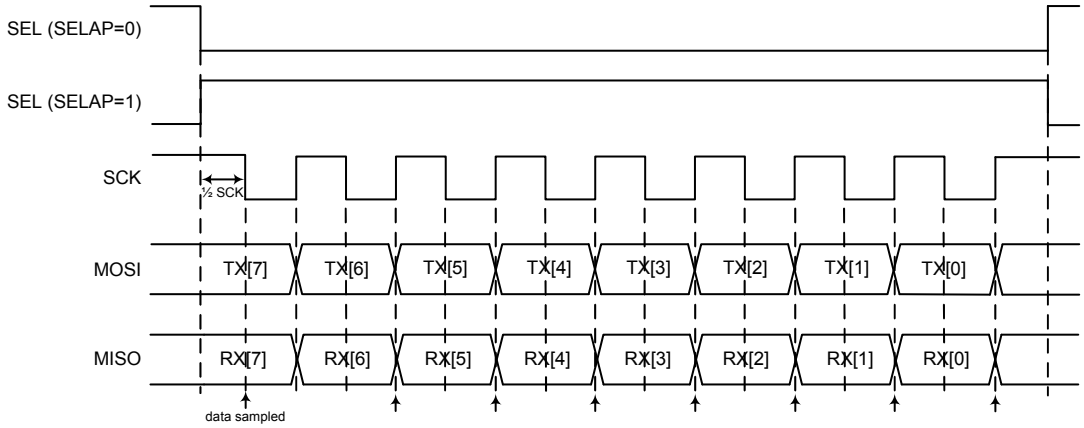


Figure 101. SPI Single Byte Transfer Timing Diagram – CPOL = 1, CPHA = 0

Figure 105 shows the continuous data transfer timing of this format. Note that the SEL signal must change to an inactive level between each data frame.

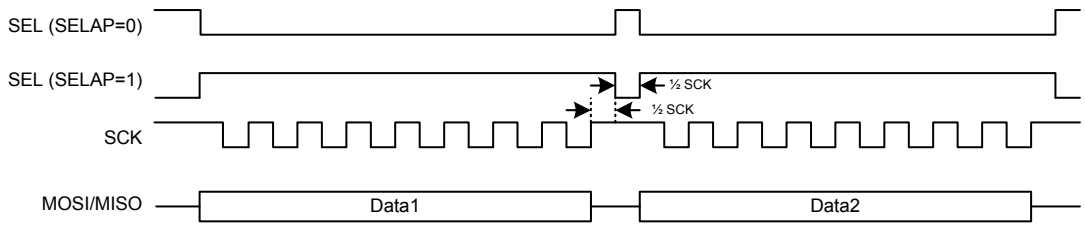


Figure 102. SPI Continuous Transfer Timing Diagram – CPOL = 1, CPHA = 0

CPOL = 1, CPHA = 1

In this format, the received data is sampled on the SCK line rising edge while the transmitted data is changed on the SCK line falling edge. In the master mode, the first bit is driven when data is written into the SPIDR register. In the slave mode, the first bit is driven at the first SCK falling edge. Figure 106 shows the single byte transfer timing of this format.

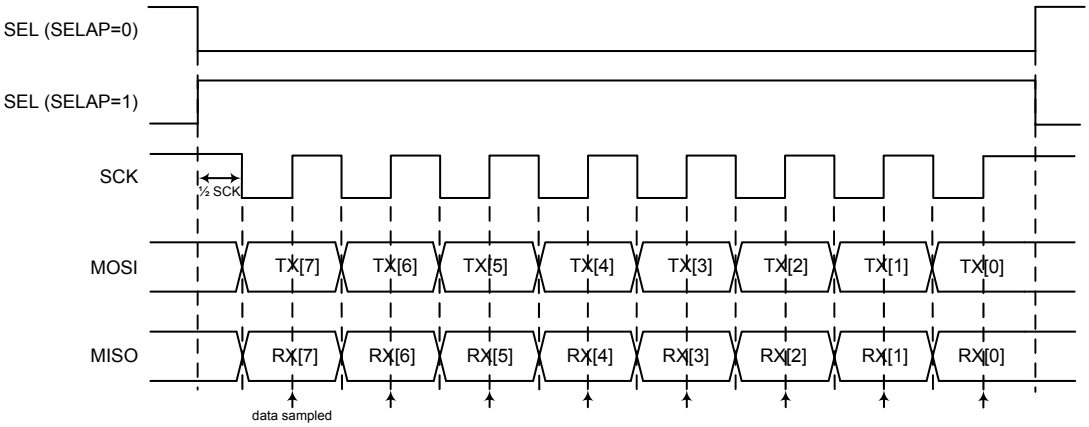


Figure 103. SPI Single Byte Transfer Timing Diagram – CPOL = 1, CPHA = 1

Figure 107 shows the continuous data transfer timing of this format. Note that the SEL signal must remain active until the last data transfer has completed.

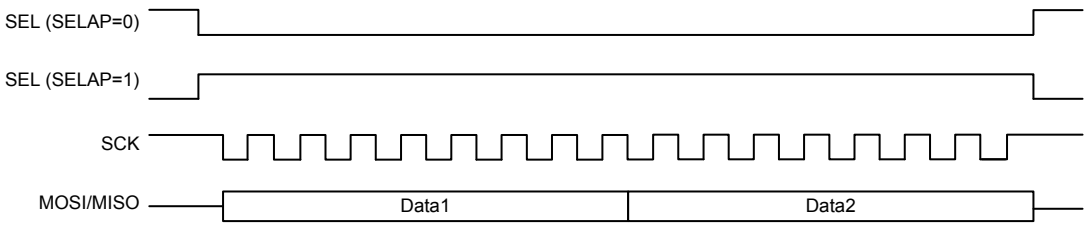


Figure 104. SPI Continuous Transfer Timing Diagram – CPOL = 1, CPHA = 1

Status Flags

TX Buffer Empty – TXBE

This TXBE flag is set when the TX buffer is empty in the non-FIFO mode or when the TX FIFO data length is equal to or less than the TX FIFO threshold level as defined by the TXFTLS field in the SPIFCR register in the FIFO mode. The following data to be transmitted can then be loaded into the buffer again. After this, the TXBE flag will be reset when the TX buffer already contains new data in the non-FIFO mode or the TX FIFO data length is greater than the TX FIFO threshold level determined by the TXFTLS bits in FIFO mode.

Transmission Register Empty – TXE

This TXE flag is set when both the TX buffer and the TX shift registers are empty. It will be reset when the TX buffer or the TX shift register contains new transmitted data.

RX Buffer Not Empty – RXBNE

This RXBNE flag is set when there is a valid received data in the RX Buffer in the non-FIFO mode or the RX FIFO data length is equal to or greater than the RX FIFO threshold level as defined by the RXFTLS field in the SPIFCR register in the SPI FIFO mode. This flag will be automatically cleared by hardware when the received data has been read out from the RX buffer totally in the non-FIFO mode or when the RX FIFO data length is less than the RX FIFO threshold level set in the RXFTLS field.

Time Out Flag – TO

The time out function is only available in the SPI FIFO mode and is disabled by loading a zero value into the TOC field in the Time Out Counter register. The time out counter will start counting if the SPI RX FIFO is not empty, once data is read from the SPIDR register or new data is received, the time out counter will be reset to 0 and count again. When the time out counter value is equal to the value specified by the TOC field in the SPIFTOCR register, the TO flag will be set. The flag is cleared by writing 1 to this bit.

Mode Fault – MF

The mode fault flag can be used to detect SPI bus usage in the SPI multi-master mode. For the multi-master mode, the SPI module is configured as a master device and the SEL signal is setup as an input signal. The mode fault flag is set when the SPI SEL pin is suddenly changed to an active level by another SPI master. This means that another SPI master is requesting to use the SPI bus. Therefore, when an SPI mode fault occurs, it will force the SPI module to operate in the slave mode and also disable all the SPI interface signals to avoid SPI bus signal collisions. For the same reason, if the SPI master wants to transfer data, it also needs to inform other SPI masters by driving its SEL signal to an active state. The detailed configuration diagram for the SPI multi-master mode is shown in the following figure.

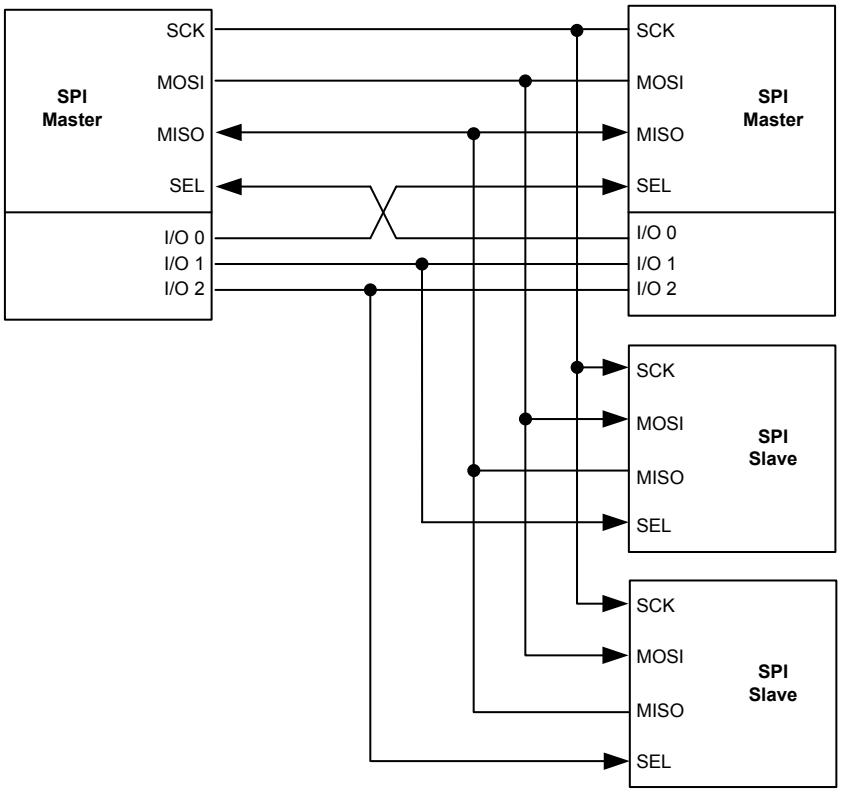


Figure 105. SPI Multi-Master Slave Environment

Table 41. SPI Mode Fault Trigger Conditions

Mode fault	Descriptions
Trigger condition	1. SPI Master mode. 2. SELOEN = 0 in the SPICR0 register – SEL pin is configured to be the input mode. 3. SEL signal changes to an active level when driven by the external SPI master.
SPI behavior	1. Mode fault flag is set. 2. The SPIEN bit in the SPICR0 register is reset. This disables the SPI interface and blocks all output signals from the device. 3. The MODE bit in the SPICR1 register is reset. This forces the device into slave mode.

Table 42. SPI Master Mode SEL Pin Status

	SEL as Input – SELOEN = 0		SEL as Output – SELOEN = 1	
Multi-master	Support		Not support	
SPI SEL control signal	Use Another GPIO to replace the SEL pin function		SEL pin in hardware or software mode - using SELM setting	
Continuous transfer	Case 1	Case 2	Case 1	Case 2
	Not supported	Supported	Using hardware control	Hardware or software control

Case 1: SEL signal must be inactive between each data transfer.
Case 2: SEL signal will not to be active until the last data frame has finished.
Note: When the SPI is in the slave mode, the SEL signal is always an input and not affected by the SELOEN bit in the SPICR0 register.

Write Collision – WC

The following conditions will assert the Write Collision Flag.

- The FIFOEN bit in the SPIFCR register is cleared.
  The write collision flag is asserted when new data is written into the SPIDR register while both the TX buffer and the shift register are already full. Any new data written into the TX buffer will be lost.
- The FIFOEN bit in the SPIFCR register is set.
  The write collision flag is asserted to indicate that new data is written into the SPIDR register while both the TX FIFO and the TX shift register are already full. Any new data written into the TX FIFO will be lost.

Read Overrun – RO

- The FIFOEN bit in the SPIFCR register is cleared.
  The read overrun flag is asserted to indicate that both the RX shift register and the RX buffer are already full, if one more data is received. This will result in the newly received data not being shifted into the SPI shift register. As a result the latest received data will be lost.
- The FIFOEN bit in the SPIFCR register is set.
  The read overrun flag is set to indicate that the RX shift register and the RX FIFO are both full if one more data is received. This means that the latest received data can not be shifted into the SPI shift register. As a result the latest received data will be lost.

Slave Abort – SA

In the SPI slave mode, the slave abort flag is set to indicate that the SEL pin suddenly changed to an inactive state during the reception of a data frame transfer. The data frame length is set by the DFL field in the SPICR1 register.

Register Map

The following table shows the SPI registers and their reset values.

Table 43. SPI Register Map

Register	Offset	Description	Reset Value
SPICR0	0x000	SPI Control Register 0	0x0000_0000
SPICR1	0x004	SPI Control Register 1	0x0000_0000
SPIIER	0x008	SPI Interrupt Enable Register	0x0000_0000
SPICPR	0x00C	SPI Clock Prescaler Register	0x0000_0000
SPIDR	0x010	SPI Data Register	0x0000_0000
SPISR	0x014	SPI Status Register	0x0000_0003
SPIFCR	0x018	SPI FIFO Control Register	0x0000_0000
SPIFSR	0x01C	SPI FIFO Status Register	0x0000_0000
SPIFTOCR	0x020	SPI FIFO Time Out Counter Register	0x0000_0000

Register Descriptions

SPI Control Register 0 – SPICR0

This register specifies the SEL control and the SPI enable bits.

offset: 0x000

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	SELHT				GUADT			
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	GUADTEN	DUALEN	Reserved	SSELC	SELOEN	Reserved		SPIEN
Type/Reset	RW 0	RW 0		RW 0	RW 0			RW 0

Bits	Field	Descriptions
[15:12]	SELHT	Chip Select Hold Time 0x0: 1/2 SCK 0x1: 1 SCK 0x2: 3/2 SCK 0x3: 2 SCK .... Note that SELHT is for master mode only.
[11:8]	GUADT	Guard Time GUADTEN=1 0x0: 1 SCK 0x1: 2 SCK 0x2: 3 SCK ... Note that GUADT is for master mode only.
[7]	GUADTEN	Guard Time Enable 0: Guard Time is 1/2 SCK 1: When set this bit, Guard time can be controlled by GUADT Note that GUADTEN is for master mode only.
[6]	DUALEN	Dual Port Enable 0: Dual port is disabled 1: Dual port is enabled The control bit is used to support the dual output read mode of the serial SPI NOR Flash. When this bit is set and the MOSI signal will change the direction from output to input and receive the serial data stream. That means the DUALEN control bit is only for master mode.

Bits	Field	Descriptions
[4]	SSELC	Software Slave Select Control 0: Set the SEL output to an inactive state 1: Set the SEL output to an active state The application Software can setup the SEL output to an active or inactive state by configuring the SSELC bit. The active level is configured by the SELAP bit in the SPICR1 register. Note that the SSELC bit is only available when the SELOEN bit is set to 1 for enabling the SEL output meanwhile the SELM bit is cleared to 0 for controlling the SEL signal by software. Otherwise, the SSELC bit has no effect.
[3]	SELOEN	Slave Select Output Enable 0: Set the SEL signal to the input mode for Multi-master mode 1: Set the SEL signal to the output mode for slave select The SELOEN is only available in the master mode to setup the SEL signal as an input or output signal. When the SEL signal is configured to operate in the output mode, it is used as a slave select signal in either the hardware or software mode according to the SELM bit setting in the SPICR1 register. The SEL signal is used for mode fault detection in the multi-master environment when it is configured to operate in the input mode.
[0]	SPIEN	SPI Enable 0: SPI interface is disabled 1: SPI interface is enabled

SPI Control Register 1 – SPICR1

This register specifies the SPI parameters including the data length, the transfer format, the SEL active polarity/mode, the LSB/MSB control, and the master/slave mode.

Offset: 0x004

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved	MODE	SELM	FIRSTBIT	SELAP	FORMAT		
Type/Reset		RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	Reserved				DFL			
Type/Reset					RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[14]	MODE	Master or Slave Mode 0: Slave mode 1: Master mode

Bits	Field	Descriptions
[13]	SELM	Slave Select Mode 0: SEL signal is controlled by software – asserted or de-asserted by the SSELC bit 1: SEL signal is controlled by hardware – generated automatically by the SPI hardware Note that SELM bit is available for master mode only – MODE = 1
[12]	FIRSTBIT	LSB or MSB Transmitted First 0: MSB transmitted first 1: LSB transmitted first
[11]	SELAP	Slave Select Active Polarity 0: SEL signal is active low 1: SEL signal is active high
[10:8]	FORMAT	SPI Data Transfer Format These three bits are used to determine the data transfer format of the SPI interface.

FORMAT [2:0]	CPOL	CPHA
001	0	0
010	0	1
110	1	0
101	1	1
Others	Reserved	

CPOL: Clock Polarity
0: SCK Idle state is low
1: SCK Idle state is high
CPHA: Clock Phase
0: Data is captured on the first SCK clock edge
1: Data is captured on the second SCK clock edge

[3:0]	DFL	Data Frame Length Selects the data transfer frame from 1 bit to 16 bits. 0x1: 1 bit 0x2: 2 bits … 0xF: 15 bits 0x0: 16 bits

SPI Interrupt Enable Register – SPIIER

This register contains the corresponding SPI interrupt enable control bit.

Offset: 0x008

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	TOIEN	SAIEN	MFIEN	ROIEN	WCIEN	RXBNEIEN	TXEIEN	TXBEIEN
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[7]	TOIEN	Time Out Interrupt Enable 0: Disable 1: Enable
[6]	SAIEN	Slave Abort Interrupt Enable 0: Disable 1: Enable
[5]	MFIEN	Mode Fault Interrupt Enable 0: Disable 1: Enable
[4]	ROIEN	Read Overrun Interrupt Enable 0: Disable 1: Enable
[3]	WCIEN	Write Collision Interrupt Enable 0: Disable 1: Enable
[2]	RXBNEIEN	RX Buffer Not Empty Interrupt Enable 0: Disable 1: Enable Generates an interrupt request when the RXBNE flag is set and when the RXBNEIEN bit is set. In the FIFO mode, the interrupt request being generated depends upon the RX FIFO trigger level setting.
[1]	TXEIEN	TX Empty Interrupt Enable 0: Disable 1: Enable The TX register empty interrupt request will be generated when the TXE flag and the TXEIEN bit are set.

Bits	Field	Descriptions
[0]	TXBEIEN	TX Buffer Empty Interrupt Enable 0: Disable 1: Enable The TX buffer empty interrupt request will be generated when the TXBE flag and the TXBEIEN bit are set. In the FIFO mode, the interrupt request being generated depends upon the TX FIFO trigger level setting.

SPI Clock Prescaler Register – SPICPR

This register specifies the SPI clock prescaler ratio.

Offset: 0x00C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	CP							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	CP							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	CP	SPI Clock Prescaler The SPI clock (SCK) is determined by the following equation: $f_{SCK} = f_{PCLK} / (2 \times (CP + 1))$, where the CP ranges is from 0 to 65535 Note: For the SPI slave mode, the system clock (f_{PCLK}) must be at least 3 times faster than the external SPI SCK input.

SPI Data Register – SPIDR

This register stores the SPI received or transmitted Data.

Offset: 0x010

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	DR							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	DR							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	DR	Data Register The SPI data register is used to store the serial bus transmitted or received data. In the non-FIFO mode, writing data into the SPI data register will also load the data into the data transmission buffer, known as the TX buffer. Reading data from the SPI data register will return the data held in the data received buffer, named RX buffer.

SPI Status Register – SPISR

This register contains the relevant SPI status.

Offset: 0x014

Reset value: 0x0000_0003

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							BUSY
Type/Reset								RO 0
	7	6	5	4	3	2	1	0
	TO	SA	MF	RO	WC	RXBNE	TXE	TXBE
Type/Reset	WC 0	WC 0	WC 0	WC 0	WC 0	RO 0	RO 1	RO 1

Bits	Field	Descriptions
[8]	BUSY	SPI Busy flag 0: SPI not busy 1: SPI busy In the master mode, this flag is reset when the TX buffer and TX shift register are both empty and is set when the TX buffer or the TX shift register are not empty. In the slave mode, this flag is set when SEL changes to an active level and is reset when SEL changes to an inactive level.
[7]	TO	Time Out flag 0: No RX FIFO time out 1: RX FIFO time out has occurred. Write 1 to clear it. Once the time out counter value is equal to the TOC field setting in the SPIFTOCR register, the time out flag will be set and an interrupt will be generated if the TOIEN bit in the SPIIER register is enabled. This bit is cleared by writing 1. Note: This Time Out flag function is only available in the SPI FIFO mode.
[6]	SA	Slave Abort flag 0: No slave abort 1: Slave abort has occurred. This bit is set by hardware and cleared by writing 1.
[5]	MF	Mode Fault flag 0: No mode fault 1: Mode fault has occurred This bit is set by hardware and cleared by writing 1.
[4]	RO	Read Overrun flag 0: No read overrun 1: Read overrun has occurred. This bit is set by hardware and cleared by writing 1.
[3]	WC	Write Collision flag 0: No write collision 1: Write collision has occurred. This bit is set by hardware and cleared by writing 1.
[2]	RXBNE	Receive Buffer Not Empty flag 0: RX buffer empty 1: RX buffer not empty This bit indicates the RX buffer status in the non-FIFO mode. It is also used to indicate if the RX FIFO trigger level has been reached in the FIFO mode. This bit will be cleared when the SPI RX buffer is empty in the non-FIFO mode or if the number of data contained in RX FIFO is less than the trigger level which is specified by the RXFTLS field in the SPIFCR register in the SPI FIFO mode.
[1]	TXE	Transmission Register Empty flag 0: TX buffer or TX shift register is not empty 1: TX buffer and TX shift register both are empty
[0]	TXBE	Transmit Buffer Empty flag 0: TX buffer not empty 1: TX buffer empty In the FIFO mode, this bit indicates that the number of data contained in TX FIFO is equal to or less than the trigger level specified by the TXFTLS field in the SPIFCR register.

SPI FIFO Control Register – SPIFCR

This register contains the related SPI FIFO control including the FIFO enable control and the FIFO trigger level selections.

Offset: 0x018

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved					FIFOEN		Reserved
Type/Reset						RW 0		
	7	6	5	4	3	2	1	0
	RXFTLS				TXFTLS			
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[10]	FIFOEN	FIFO Enable 0: FIFO disable 1: FIFO enable This bit cannot be set or reset when the SPI interface is in transmitting.
[7:4]	RXFTLS	RX FIFO Trigger Level Select 0000: Trigger level is 0 0001: Trigger level is 1 ... 1000: Trigger level is 8 Others: Reserved The RXFTLS field is used to specify the RX FIFO trigger level. When the number of data contained in the RX FIFO is equal to or greater than the trigger level defined by the RXFTLS field, the RXBNE flag will be set.
[3:0]	TXFTLS	TX FIFO Trigger Level Select 0000: Trigger level is 0 0001: Trigger level is 1 ... 1000: Trigger level is 8 Others: Reserved The TXFTLS field is used to specify the TX FIFO trigger level. When the number of data contained in the TX FIFO is equal to or less than the trigger level defined by the TXFTLS field, the TXBE flag will be set.

SPI FIFO Status Register – SPIFSR

This register contains the relevant SPI FIFO status.

Offset: 0x01C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	RXFS				TXFS			
Type/Reset	RO	RO	RO	RO	RO	RO	RO	RO
	0	0	0	0	0	0	0	0

Bits	Field	Descriptions
[7:4]	RXFS	RX FIFO Status 0000: RX FIFO empty 0001: RX FIFO contains 1 data ... 1000: RX FIFO contains 8 data Others: Reserved
[3:0]	TXFS	TX FIFO Status 0000: TX FIFO empty 0001: TX FIFO contains 1 data … 1000: TX FIFO contains 8 data Others: Reserved

SPI FIFO Time Out Counter Register – SPIFTOCR

This register stores the SPI RX FIFO time out counter value.

Offset: 0x020

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	TOC							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	TOC							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	TOC	Time Out Counter The time out counter starts to count from 0 after the SPI RX FIFO receives a data, and reset the counter value once the data is read from the SPIDR register by software or another new data is received. If the FIFO does not receive new data or the software does not read data from the SPIDR register the time out counter value will continuously increase. When the time out counter value is equal to the TOC setting value, the TO flag in the SPISR register will be set and an interrupt will be generated if the TOIEN bit in the SPIIEN register is set. The time out counter will be stopped when the RX FIFO is empty. The SPI FIFO time out function can be disabled by setting the TOC field to zero. The time out counter is driven by the system APB clock, named f_{PCLK}.

19 Universal Synchronous Asynchronous Receiver Transmitter (USART)

Introduction

The Universal Synchronous Asynchronous Receiver Transceiver, USART, provides a flexible full duplex data exchange using synchronous or asynchronous transfer. The USART is used to translate data between parallel and serial interfaces, and is also commonly used for RS232 standard communication. The USART peripheral function supports a variety of interrupts.

The USART module includes an 8-byte transmit FIFO, TX FIFO, and a 8-byte receive FIFO, RX FIFO. Software can detect a USART error status by reading USART Status & Interrupt Flag Register, USRSIFR. The status includes the condition of the transfer operations as well as several error conditions resulting from Parity, Overrun, Framing and Break events.

The USART includes a programmable baud rate generator which is capable of dividing the USART clock of the CK_APB (CK_USART) to produce a baud rate clock for the USART transmitter and receiver.

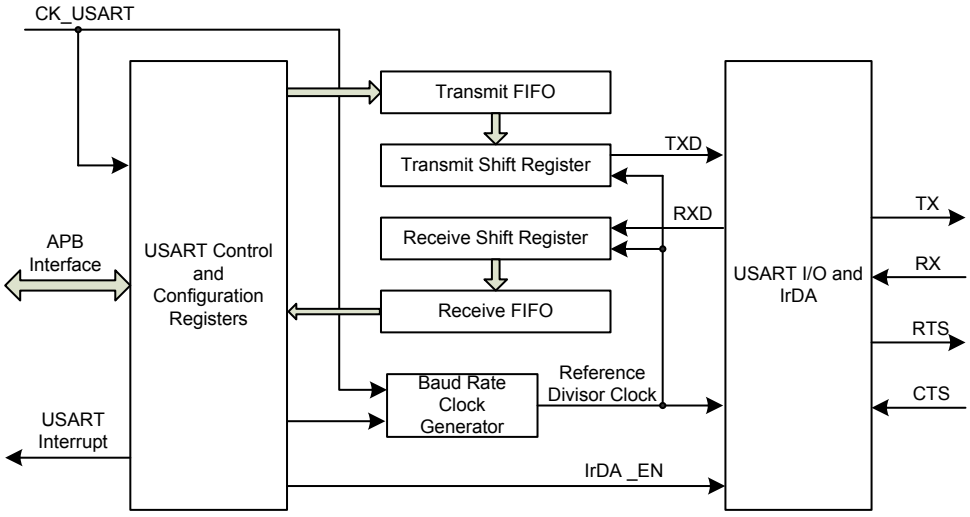


Figure 106. USART Block Diagram

Features

- Supports both asynchronous and clocked synchronous serial communication modes
- Full Duplex Communication Capability
- Programming baud rate up to 3 Mbit/s for asynchronous mode and 6 Mbit/s for synchronous mode
- IrDA SIR encoder and decoder
  - Support of normal 3/16 bit duration and low-power (1.41 ~ 2.23 μs) durations
- Supports RS485 mode with output enable
- Auto hardware flow control mode – RTS, CTS
- Fully programmable serial communication functions including:
  - Word length: 7, 8, or 9-bit character
  - Parity: Even, odd, or no-parity bit generation and detection
  - Stop bit: 1 or 2 stop bit generation
  - Bit order: LSB-first or MSB-first transfer
- Error detection: Parity, overrun, and frame error
- FIFO:
  - Receive FIFO: 8 × 9 bits (max 9 data bits)
  - Transmit FIFO: 8 × 9 bits (max 9 data bits)

Function Descriptions

Serial Data Format

The USART module performs a parallel-to-serial conversion on data that is written to the transmit FIFO registers and then sends the data with the following format: Start bit, 7 ~ 9 LSB first data bits, optional Parity bit and finally 1 ~ 2 Stop bits. The Start bit has the opposite polarity of the data line idle state. The Stop bit is the same as the data line idle state and provides a delay before the next start situation. The both Start and Stop bits are used for data synchronization during the asynchronous data transmission.

The USART module also performs a serial-to-parallel conversion on the data that is read from the receive FIFO registers. It will first check the Parity bit and will then look for a Stop bit. If the Stop bit is not found, the USART module will consider the entire word transmission to have failed and respond with a Framing Error.

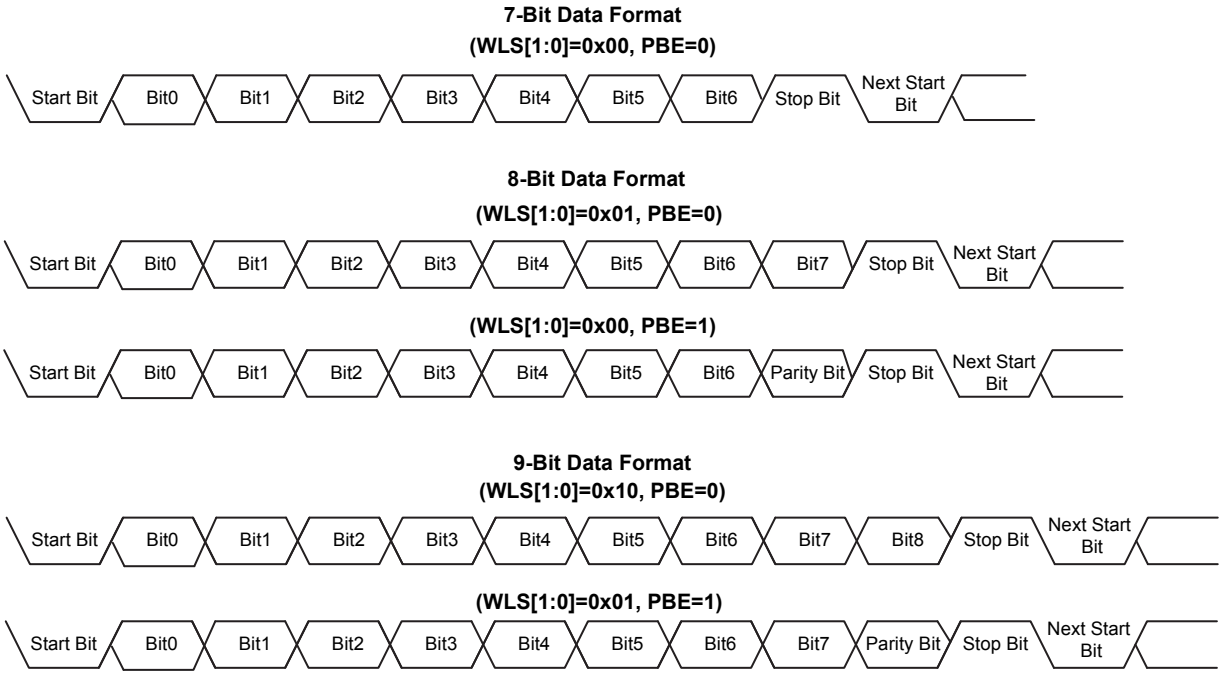


Figure 107. USART Serial Data Format

Baud Rate Generation

The baud rate for the USART receiver and transmitter are both set with the same values. The baud-rate divisor, BRD, has the following relationship with the USART clock which is known as CK_USART.

Baud Rate Clock = CK_USART / BRD

Where CK_USART clock is the APB clock connected to the USART while the BRD range is from 16 to 65535 for asynchronous mode and 8 to 65535 for synchronous mode.

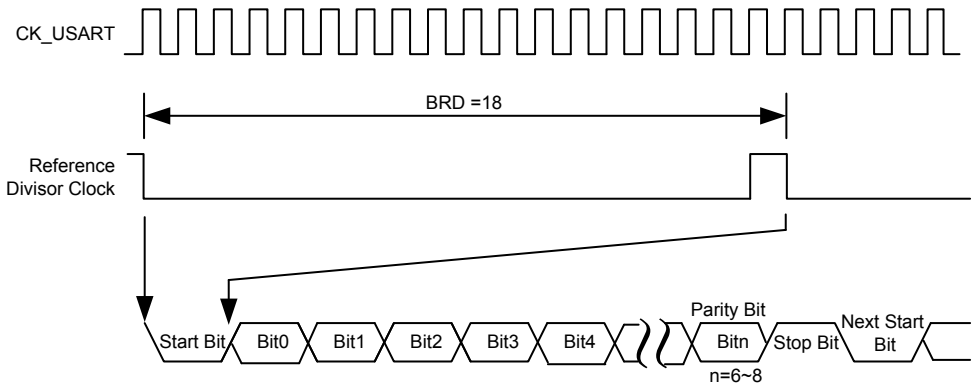


Figure 108. USART Clock CK_USART and Data Frame Timing

Table 44. Baud Rate Deviation Error Calculation – CK_USART = 8 MHz

Baud rate		CK_USART = 8 MHz		
No	Kbps	Actual	BRD	Deviation Error rate
1	2.4	2.4	3333	0.01%
2	9.6	9.6	833	0.04%
3	19.2	19.2	417	-0.08%
4	57.6	57.6	139	-0.08%
5	115.2	115.9	69	0.64%
6	230.4	228.6	35	-0.79%
7	460.8	470.6	17	2.12%
8	921.6	888.9	9	-3.55%
9	2250	N/A	N/A	N/A
10	3000	N/A	N/A	N/A

Table 45. Baud Rate Deviation Error Calculation – CK_USART = 20 MHz

Baud rate		CK_USART = 20 MHz		
No	Kbps	Actual	BRD	Deviation Error rate
1	2.4	2.4	8333	0.00%
2	9.6	9.6	2083	0.02%
3	19.2	19.2	1042	-0.03%
4	57.6	57.6	347	0.06%
5	115.2	114.9	174	-0.22%
6	230.4	229.9	87	-0.22%
7	460.8	461.5	43	0.94%
8	921.6	909.1	22	-1.36%
9	2250	2222.2	9	-1.23%
10	3000	2857.1	7	-4.76%

Table 46. Baud Rate Deviation Error Calculation – CK_USART = 24 MHz

Baud rate		CK_USART = 24 MHz		
No	Kbps	Actual	BRD	Deviation Error rate
1	2.4	2.4	10000	0.00%
2	9.6	9.6	2500	0.00%
3	19.2	19.2	1250	0.00%
4	57.6	57.6	417	-0.08%
5	115.2	115.4	208	0.16%
6	230.4	230.8	104	0.16%
7	460.8	461.5	52	0.16%
8	921.6	923.1	26	0.16%
9	2250	2181.8	11	-3.03%
10	3000	3000	8	0.00%

Table 47. Baud Rate Deviation Error Calculation – CK_USART = 40 MHz

Baud rate		CK_USART = 40 MHz		
No	Kbps	Actual	BRD	Deviation Error rate
1	2.4	2.4	16667	0.00%
2	9.6	9.6	4167	-0.01%
3	19.2	19.2	2083	0.02%
4	57.6	57.6	694	0.06%
5	115.2	115.3	347	0.06%
6	230.4	229.9	174	-0.22%
7	460.8	459.8	87	-0.22%
8	921.6	930.2	43	0.94%
9	2250	2222.2	18	-1.23%
10	3000	3076.9	13	2.56%

Hardware Flow Control

The USART supports the hardware flow control function which is enabled by setting the HFCEN bit in the USRCR register to 1. It is possible to control the serial data flow between 2 USART devices by using the CTS input and the RTS output. The Figure 112 shows the connection diagram in this mode. The hardware flow control function is categorized into to types. One is the RTS flow control function and the other is the CTS flow control function.

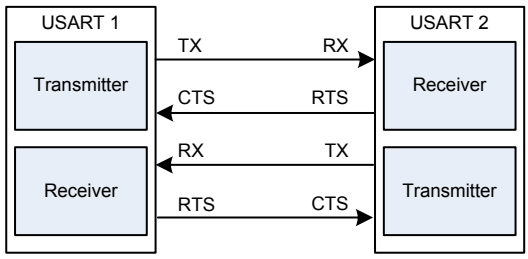


Figure 109. Hardware Flow Control between 2 USARTs

RTS Flow Control

In the RTS flow control, the USART RTS pin is active with a logic low state when the receive data register is empty. It means that the receiver is ready to receive a new data. When the RX FIFO reaches the trigger level which is specified by configuring the RXTL field in the USRFCR register, the USART RTS pin is inactive with a logic high state. Figure 113 shows the example of the RTS flow control.

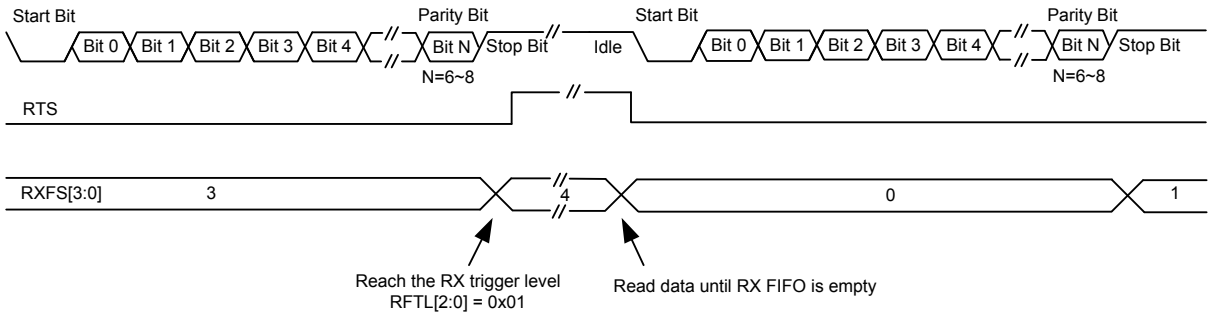


Figure 110. USART RTS Flow Control

CTS Flow Control

If the hard flow control function is enabled, the URTXEN bit in the USRCR register will be controlled by the USART CTS input signal. If the USART CTS pin is forced to a logic low state, the URTXEN bit will automatically be set to 1 to enable the data transmission. However, if the USART CTS pin is forced to a logic high state, the URTXEN bit will be cleared to 0 and then the data transmission will also be disabled.

When the USART CTS pin is forced to a logic high state during a data transmission period, the current data transmission will be continued until the stop bit is completed. The Figure 114 shows an example of the communication with CTS flow control.

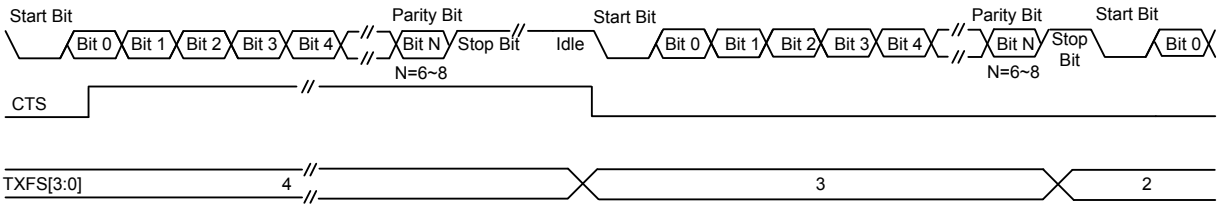


Figure 111. USART CTS Flow Control

IrDA

The USART IrDA mode is provided as a half-duplex point-to-point wireless communication interface.

The USART module includes an integrated modulator and demodulator which allow a wireless communication using infrared transceivers. The transmitter specifies a logic data '0' as a 'high' pulse and a logic data '1' as a 'low' level while the Receiver specifies a logic data '0' as a 'low' pulse and a logic data '1' as 'high' level in the IrDA mode.

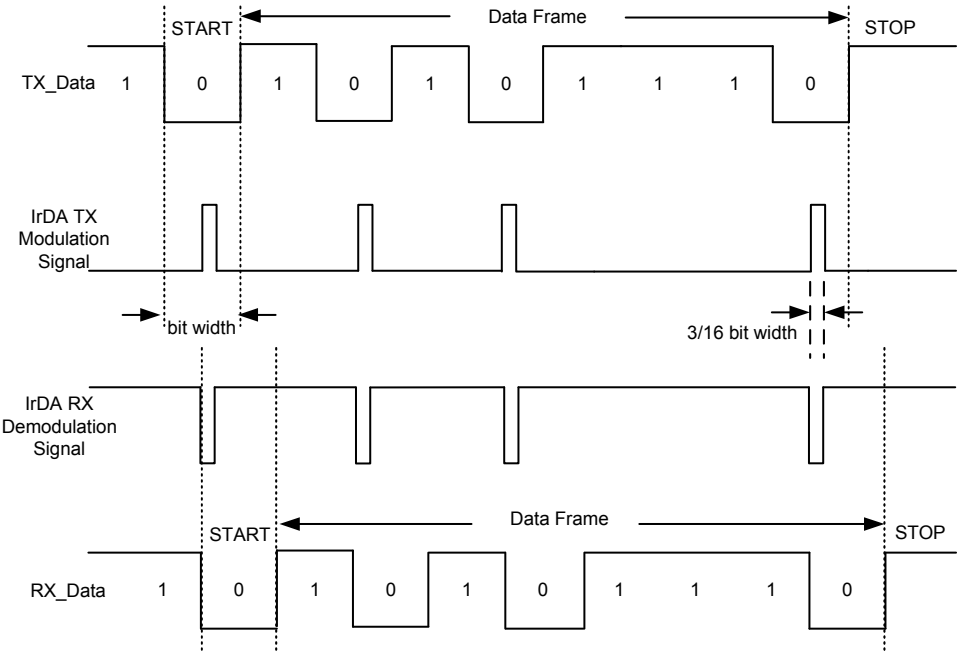


Figure 112. IrDA Modulation and Demodulation

The IrDA mode provides two operation modes, one is the normal mode and the other is the low-power mode.

IrDA Normal Mode

For the IrDA normal mode, the width of each transmitted pulse generated by the transmitter modulator is specified as 3/16 of the baud rate clock period. The receiver pulse width for the IrDA receiver demodulator is based on the IrDA receive debounce filter which is implemented using an 8-bit down-counting counter. The debounce filter counter value is specified by the IrDAPSC field in the IrDACR register. When a falling edge is detected on the receiver pin, the debounce filter counter starts to count down, driven by the CK_USART clock. If a rising edge is detected on the receiver pin, the counter stops counting and is reloaded with the IrDAPSC value. When a low pulse falling edge on the receiver pin is detected and then before the debounce filter has counted down to zero, a rising edge is also detected, then this low pulse will be considered as glitch noise and will be discarded. If a low pulse falling edge appears on the receiver pin but no rising edge is detected before the debounce counter reaches 0, then the input is regarded as a valid data "0" for this bit duration. The IrDAPSC value must be set to be greater than or equal to 0x01, then the IrDA receiver demodulation operation can function properly. The IrDAPSC value can be adjusted to meet the USART baud rate setting to filter the IrDA received glitch noise of which the width is smaller than the prescaler setting duration.

IrDA Low-Power Mode

In the IrDA low-power mode, the transmitted IrDA pulse width generated by the transmitter modulator is not kept at 3/16 of the baud rate clock period. Instead, the pulse width is fixed and is calculated by the following formula. The transmitted pulse width can be adjusted by the IrDAPSC field to meet the minimum pulse width specification of the external IrDA Receiver device.

$$T_{IrDA\_L} = 3 \times IrDAPSC / CK\_USART$$

Note: 1. T_{IrDA_L} is transmitted pulse width in the low power mode.

2. The IrDAPSC filed in the IrDA Control Register IrDACR is the IrDACR prescaler value.

The debounce behavior in the IrDA low-power receiving mode is similar to the IrDA normal mode. For glitch detection, the low pulse of which the pulse width is shorter than 1 × (IrDAPSC / CK_USART) should be discarded in the IrDA receiver demodulation. A valid low data is accepted if its low pulse width is greater than 2 × (IrDAPSC / CK_USART) duration.

The IrDA physical layer specification specifies a minimum delay with a value of 10 ms between the transmission and reception switch; and this IrDA receiver set-up time also should be managed by the software.

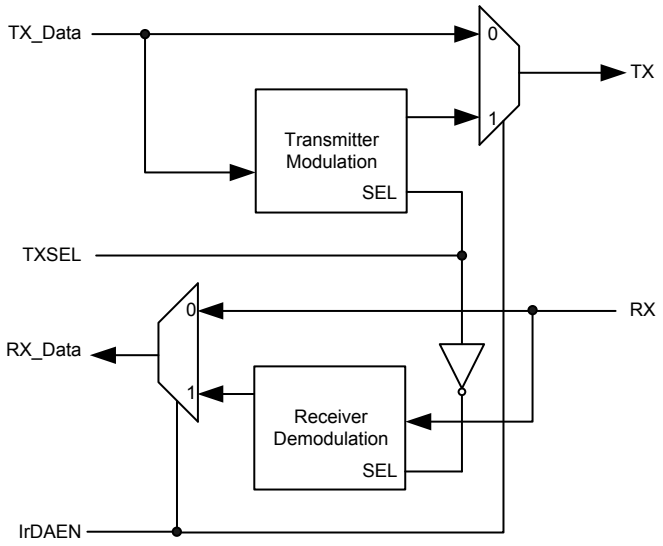


Figure 113. USART I/O and IrDA Block Diagram

RS485 Mode

The RS485 mode of the USART provides the data transmission on the interface transmitted over a 2-wire twisted pair bus. The RS485 transceiver interprets the voltage levels of the differential signals with respect to a third common voltage. Without this common reference, the transceiver may interpret the differential signals incorrectly. This enhances the noise rejection capabilities of the RS485 interface. The USART RTS pin is used to control the external RS485 transceiver whose polarity can be selected by configuring the TXENP bit in the RS485 Control Register, named RS485CR, when the USART operates in the RS485 mode.

RS485 Auto Direction Mode – AUD

When the RS485 mode is configured as a master transmitter, it will operate in the Auto Direction Mode, AUD. In the AUD mode the polarity of the USART RTS pin is configurable according to the TXENP bit in the RS485 Control Register in the RS485 mode. This pin can be used to control the external RS485 transceiver to enable the transmitter.

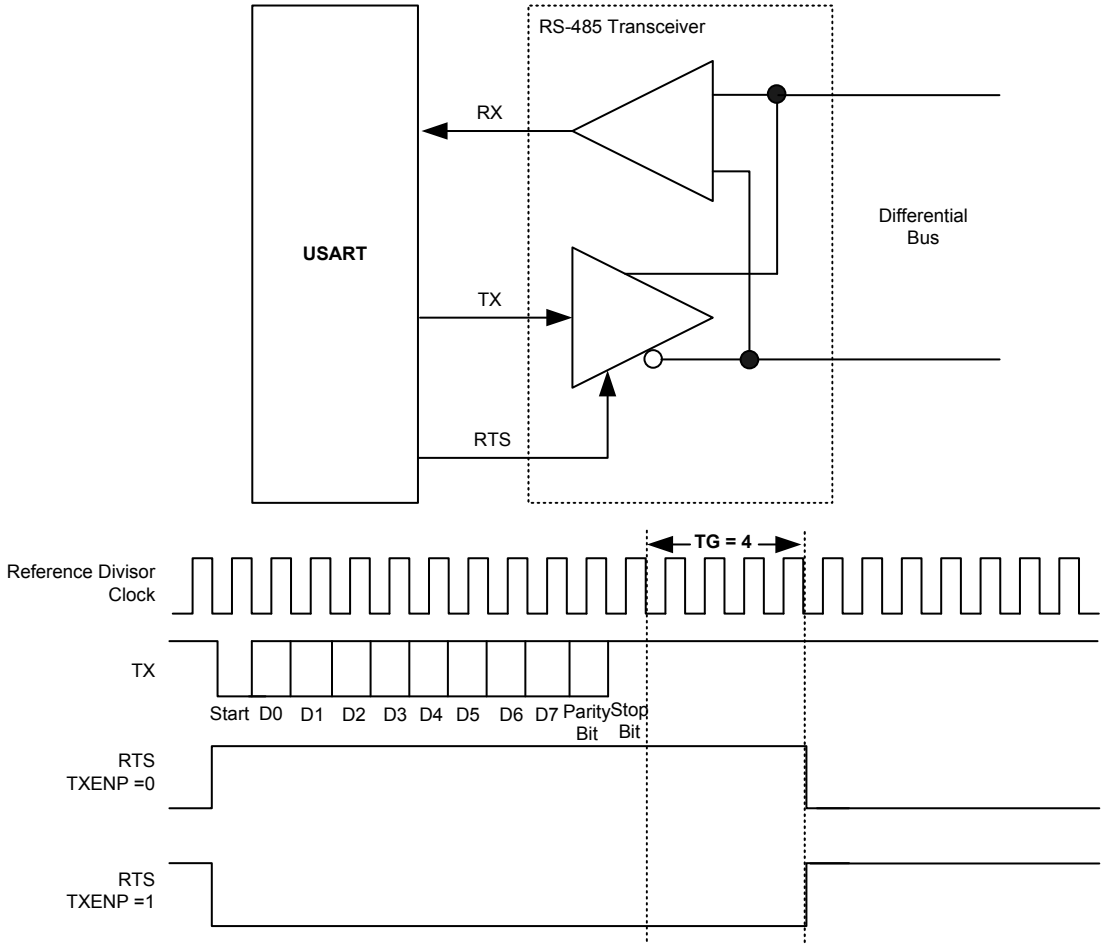


Figure 114. RS485 Interface and Waveform

RS485 Normal Multi-drop Operation Mode – NMM

When the RS485 mode is configured as an addressable slave, it will operate in the Normal Multi-drop Operation Mode, NMM. This mode is enabled when the RSNMM field is set in the RS485CR register. Regardless of the URRXEN value in the USRCR register, all the received data with a parity bit "0" will be ignored until the first address byte is detected with a parity bit "1" and then the received address byte will be stored in the RXFIFO. Once the first address data is detected and stored in the RXFIFO, the RSADD flag in the USRSIFR register will be set and generate an interrupt if the RSADDIE bit in the USRIER register is set to 1. Application software can determine whether the receiver is enabled or disabled to accept the following data by configuring the URRXEN bit. When the receiver is enabled by setting the URRXEN bit to 1, all received data will be stored in the RXFIFO. Otherwise, all received data will be ignored if the receiver is disabled by clearing the URRXEN bit to 0.

RS485 Auto Address Detection Operation Mode – AAD

Except the Normal Multi-drop Operation Mode, the RS485 mode can operate in the Auto Address Detection Operation Mode, AAD, when it is configured as an addressable slave. This mode is enabled by setting the RSAAD filed to 1 in the RS485CR register. The receiver will detect the address frame with a parity bit "1" and then compare the received address data with the ADDMATCH field value which is a programmable 8-bit address value specified in the RS485CR register. If the address data matches the ADDMATCH value, it will be stored in the RXFIFO and the URRXEN bit will be automatically set. When the receiver is enabled, all received data will be stored in the RXFIFO until the next address frame does not match the ADDMATCH value and then the receiver will be automatically disabled. After the receiver is enabled, software can disable the receiver by setting the URRXEN bit to '0'.

Synchronous Master Mode

The data is transmitted in a full-duplex style in the USART Synchronous Master Mode, i.e., data transmission and reception both occur at the same time and only support master mode. The USART CTS pin is the synchronous USART transmitter clock output. In this mode, no clock pulses will be sent to the CTS pin during the start bit, parity bit and stop bit duration. The CPS bit in the Synchronous Control Register SYNCR, can be used to determine whether data is captured on the first or the second clock edge. The CPO bit in the SYNCR can be use to configure the clock polarity in the USART Synchronous Mode idle state. Detailed timing information is shown in Figure 119.

In the USART synchronous Mode, the USART CTS/SCK clock output pin is only used to transmit the data to slave device. If the transmission data register USRDR, is written with valid data, the USART synchronous mode will automatically transmit this data with the corresponding clock output and the USART receiver will also receive data on the RX pin. Otherwise the receiver will not obtain synchronous data if no data is transmitted.

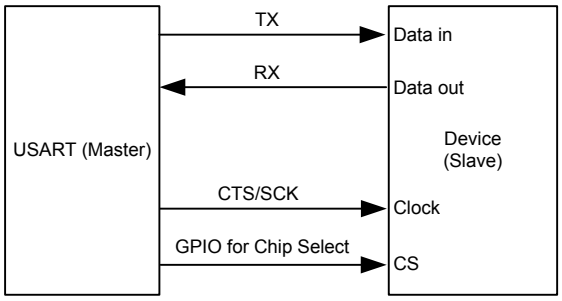


Figure 115. USART Synchronous Transmission Example

Note: The USART supports the synchronous master mode only: it cannot receive or send data related to an input clock. The USART CTS/SCK clock is always an output.

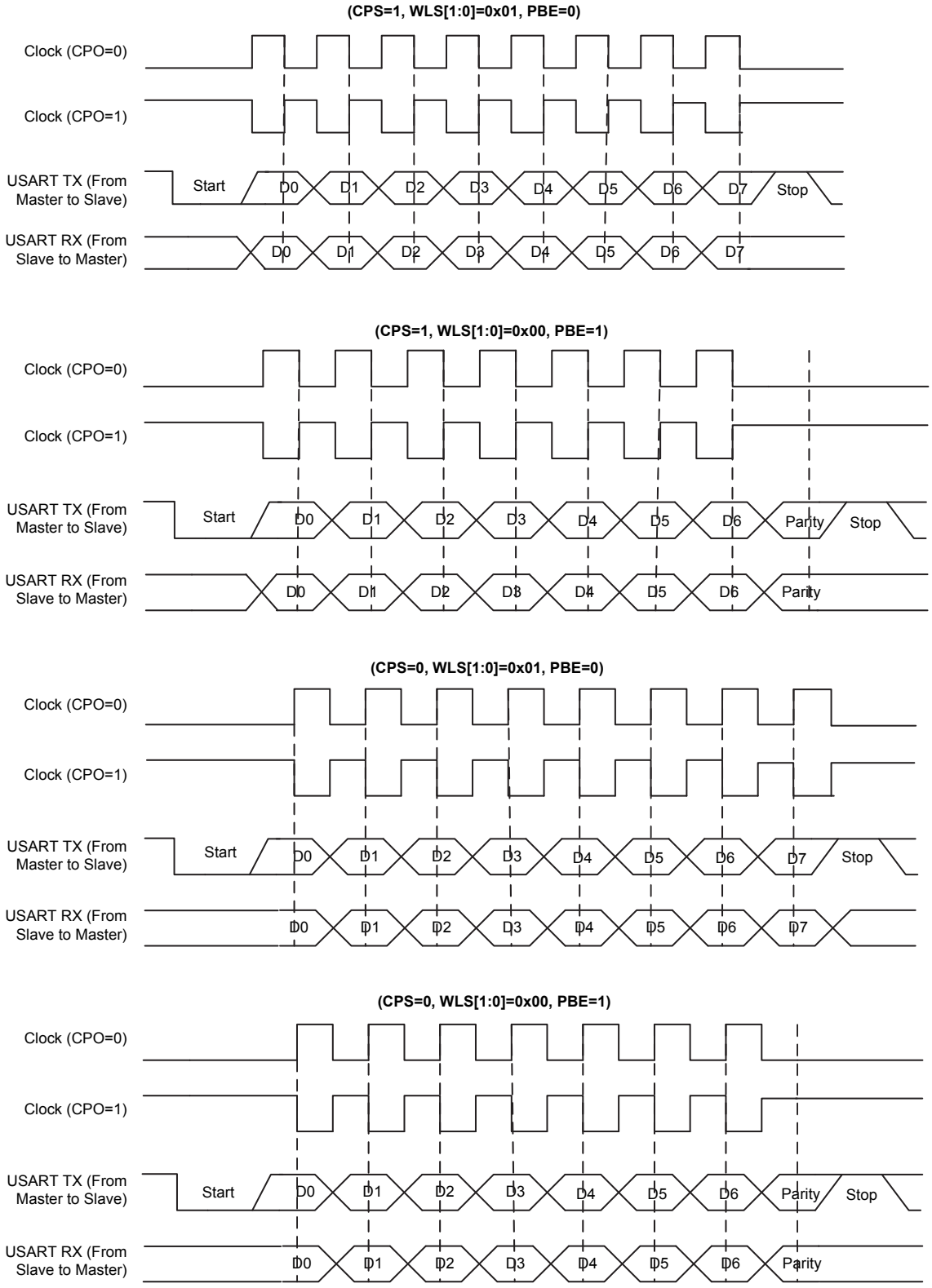


Figure 116. 8-bit Format USART Synchronous Waveform

Interrupts and Status

The UART can generate interrupts when the following event occurs and corresponding interrupt enable bits are set:

- Receive FIFO time-out interrupt: An interrupt will be generated when the USART receive FIFO does not receive a new data packet during the specified time-out interval.
- Receiver line status interrupts: The interrupt will be generated when the USART receiver overrun error, parity error, framing error or break events occurs.
- Transmit FIFO threshold level interrupt: An interrupt will be generated when the data to be transmitted in the USART Transmit FIFO is less than the specified threshold level.
- Transmit complete interrupt: An interrupt will be generated when the Transmit FIFO is empty and the content of the transmit shift register (TSR) is also completely shifted.
- Receive FIFO threshold level interrupt: An interrupt will be generated when the FIFO received data amount has reached the specified threshold level.

Register Map

The following table shows the USART registers and reset values.

Table 48. USART Register Map

Register	Offset	Description	Reset Value
USRDR	0x000	USART Data Register	0x0000_0000
USRCR	0x004	USART Control Register	0x0000_0000
USRFCR	0x008	USART FIFO Control Register	0x0000_0000
USRIER	0x00C	USART Interrupt Enable Register	0x0000_0000
USRSIFR	0x010	USART Status & Interrupt Flag Register	0x0000_0180
USRTPR	0x014	USART Timing Parameter Register	0x0000_0000
IrDACR	0x018	USART IrDA Control Register	0x0000_0000
RS485CR	0x01C	USART RS485 Control Register	0x0000_0000
SYNCR	0x020	USART Synchronous Control Register	0x0000_0000
USRDLR	0x024	USART Divider Latch Register	0x0000_0010
USRTSTR	0x028	USART Test Register	0x0000_0000

Register Descriptions

USART Data Register – USRDR

The register is used to access the USART transmitted and received FIFO data.

Offset: 0x000
Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							DB
Type/Reset								RW 0
	7	6	5	4	3	2	1	0
	DB							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[8:0]	DB	Reading data via this receiver buffer register will return the data from the receive FIFO. The receive FIFO has a capacity of up to 8 × 9 bits. By reading this register, the USART will return a 7, 8 and 9-bit received data. The DB field bit 8 is valid for 9-bit mode only and is fixed at 0 for the 8-bit mode. For the 7-bits mode, the DB[6:0] contains the available bits. Writing data to this buffer register will load data into the Transmit FIFO. The Transmit FIFO has a capacity of up to 8 × 9 bits. By writing to this register, the USART will send out 7, 8 or 9-bit transmitted data. The DB field bit 8 is valid for the 9-bit mode only and will be ignored for the 8-bit mode. For the 7-bit mode, the DB[6:0] contains the available bits.

USART Control Register – USRCR

The register specifies the parameters such as the data length, parity and stop bit for the USART. It also contains the USART enable control bits together with the USART mode and data transfer mode selections.

Offset: 0x004

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	RTS	BCB	SPE	EPE	PBE	NSB		WLS
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
		Reserved	URRXEN	URTXEN	HFCEN	TRSM		MODE
Type/Reset			RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15]	RTS	Request-To-Send Signal 0: Drive USART RTS pin to logic 1 1: Drive USART RTS pin to logic 0 Note that the RTS bit is used to control the USART RTS pin status when the HFCEN bit is reset. When the HFCEN bit is set, this RTS bit indicates the pin status that is controlled by hardware flow control function.
[14]	BCB	Break Control Bit When this bit is set to 1, the serial data output on the USART TX pin will be forced to the Spacing State (logic 0). This bit acts only on the USART TX output pin and has no effect on the transmitter logic.
[13]	SPE	Stick Parity Enable 0: Disable stick parity 1: Stick Parity bit is transmitted This bit is only available when the PBE bit is set to 1. If both the PBE and SPE bits are set to 1 and the EPE bit is cleared to 0, the transmitted parity bit will be stuck to 1. However, when the PBE and SPE bits are set to 1 and also the EPE bit is set to 1, the transmitted parity bit will be stuck to 0.
[12]	EPE	Even Parity Enable 0: Odd number of logic 1's are transmitted or checked in the data word and parity bits. 1: Even number of logic 1's are transmitted or checked in the data word and parity bits. This bit is only available when the PBE bit is set to 1.

Bits	Field	Descriptions
[11]	PBE	Parity Bit Enable 0: Parity bit is not generated (transmitted data) or checked (receive data) during transfer 1: Parity bit is generated or checked during transfer Note: When the WLS field is set to “10” to select the 9-bit data format, writing to the PBE bit has no effect.
[10]	NSB	Number of “STOP bit” 0: One “STOP bit” is generated in the transmitted data 1: Two “STOP bit” is generated when 8- and 9-bit word length is selected
[9:8]	WLS	Word Length Select 00: 7 bits 01: 8 bits 10: 9 bits 11: Reserved
[5]	URRXEN	USART RX Enable 0: Disable 1: Enable
[4]	URTXEN	USART TX Enable 0: Disable 1: Enable
[3]	HFCEN	Hardware Flow Control Function Enable 0: Disable 1: Enable
[2]	TRSM	Transfer Mode Selection This bit is used to select the data transfer protocol. 0: LSB first 1: MSB first
[1:0]	MODE	USART Mode Selection. 00: Normal operation 01: IrDA 10: RS485 11: Synchronous

USART FIFO Control Register – USRFCR

This register specifies the USART FIFO control and configurations including threshold level and reset function together with the USART FIFO status.

Offset: 0x008

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved				RXFS			
Type/Reset					RO 0	RO 0	RO 0	RO 0
	23	22	21	20	19	18	17	16
	Reserved				TXFS			
Type/Reset					RO 0	RO 0	RO 0	RO 0
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	RXTL		TXTL		Reserved		RXR	TXR
Type/Reset	RW 0	RW 0	RW 0	RW 0			WO 0	WO 0

Bits	Field	Descriptions
[27:24]	RXFS	RX FIFO Status The RXFS field shows the current number of data contained in the RX FIFO. 0000: RX FIFO is empty 0001: RX FIFO contains 1 data ... 1000: RX FIFO contains 8 data Others: Reserved
[19:16]	TXFS	TX FIFO Status The TXFS field shows the current number of data contained in the TX FIFO. 0000: TX FIFO is empty 0001: TX FIFO contains 1 data ... 1000: TX FIFO contains 8 data Others: Reserved
[7:6]	RXTL	RX FIFO Threshold Level Setting 00: 1 byte 01: 2 bytes 10: 4 bytes 11: 6 bytes The RXTL field defines the RX FIFO trigger level.
[5:4]	TXTL	TX FIFO Threshold Level Setting 00: 0 byte 01: 2 bytes 10: 4 bytes 11: 6 bytes The TXTL field determines the TX FIFO trigger level.
[1]	RXR	RX FIFO Reset Setting this bit will generate a reset pulse to reset the RX FIFO which will empty the RX FIFO. i.e., the RX FIFO pointer will be reset to 0, after a reset signal. This bit returns to 0 automatically after the reset pulse is generated.

Bits	Field	Descriptions
[0]	TXR	TX FIFO Reset Setting this bit will generate a reset pulse to reset TX FIFO which will empty the TX FIFO. i.e., the TX FIFO pointer will be reset to 0, after a reset signal. This bit returns to 0 automatically after the reset pulse is generated.

USART Interrupt Enable Register – USRIER

This register is used to enable the related USART interrupt function. The USART module generates interrupts to the controller when the corresponding events occur and the corresponding interrupt enable bits are set.

Offset: 0x00C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved						CTSIE	RXTOIE
Type/Reset							RW 0	RW 0
	7	6	5	4	3	2	1	0
	RSADDIE	BIE	FEIE	PEIE	OEIE	TXCIE	TXDEIE	RXDRIE
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[9]	CTSIE	CTS Clear-To-Send Interrupt Enable 0: Disable interrupt 1: Enable interrupt An interrupt will be generated when the CTSC bit is set in the USRSIFR register.
[8]	RXTOIE	Receive FIFO Time-Out Interrupt Enable 0: Disable interrupt 1: Enable interrupt Receive FIFO Time-Out Interrupt means that receive FIFO is not empty and no activities have occurred in the receive FIFO during the time-out duration specified by the RXTOC field.
[7]	RSADDIE	RS485 Address Detection Interrupt Enable 0: Disable interrupt 1: Enable interrupt An interrupt will be generated when the RSADD bit is set in the USRSIFR register.
[6]	BIE	Break Interrupt Enable 0: Disable interrupt 1: Enable interrupt An interrupt will be generated when the BII bit is set in the USRSIFR register.

Bits	Field	Descriptions
[5]	FEIE	Framing Error Interrupt Enable 0: Disable interrupt 1: Enable interrupt An interrupt will be generated when the FEI bit is set in the URSIFR register.
[4]	PEIE	Parity Error Interrupt Enable 0: Disable interrupt 1: Enable interrupt An interrupt will be generated when the PEI bit is set in the USRSIFR register.
[3]	OEIE	Overrun Error Interrupt Enable 0: Disable interrupt 1: Enable interrupt An interrupt will be generated when the OEI bit is set in the USRSIFR register.
[2]	TXCIE	Transmit Complete Interrupt Enable 0: Disable interrupt 1: Enable interrupt An interrupt will be generated when the TXC bit is set in the USRSIFR register.
[1]	TXDEIE	Transmit Data Empty Interrupt Enable 0: Disable interrupt 1: Enable interrupt An interrupt will be generated when the TXDE bit is set in the USRSIFR register.
[0]	RXDRIE	Receive Data Ready Interrupt Enable 0: Disable interrupt 1: Enable interrupt An interrupt will be generated when the RXDR bit is set in the USRSIFR register.

USART Status & Interrupt Flag Register – USRSIFR

This register contains the corresponding USART status.

Offset: 0x010

Reset value: 0x0000_0180

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved				CTSS	CTSC	RSADDE	TXC
Type/Reset					RO 0	WC 0	WC 0	RO 1
	7	6	5	4	3	2	1	0
	TXDE	RXTOF	RXDR	BII	FEI	PEI	OEI	RXDNE
Type/Reset	RO 1	WC 0	RO 0	WC 0	WC 0	WC 0	WC 0	RO 0

Bits	Field	Descriptions
[11]	CTSS	CTS Clear-To-Send Status 0: CTS pin is inactive 1: CTS pin is active and kept at a logic low state

Bits	Field	Descriptions
[10]	CTSC	CTS Status Change Flag This bit will be set whenever the CTS input pin status is changed and an Interrupt will be generated if the CTSC bit is set high and CTSIE = 1 in the USRIER register. Writing 1 to this bit clears the flag.
[9]	RSADD	RS485 Address Detection 0: Address is not detected 1: Address is detected This bit will be set to 1 when the receiver detects the address. An interrupt will be generated if the RSADD bit is set high and RSADDIE = 1 in the USRIER register. Writing 1 to this bit clears the flag. Note: This bit is only used in the RS485 mode by setting the MODE field in the USRCR register.
[8]	TXC	Transmit Complete 0: Either transmit FIFO (TX FIFO) or transmit shift register (TSR) is not empty 1: Both the TX FIFO and TSR register are empty An interrupt will be generated if the TXC bit is set high and TXCIE=1 in the USRIER register. This bit is cleared by a write to the USRDR register with new data.
[7]	TXDE	Transmit Data FIFO Empty 0: TX FIFO level is higher than threshold 1: TX FIFO level is less than threshold The TXDE bit will be set when the transmit FIFO level is less than the transmit FIFO threshold level setting which is set by the TXTL field in the USRFCR register. This bit will be cleared when the new data is written into the USRDR register and the TX FIFO level is higher than the threshold setting.
[6]	RXTOF	Receive FIFO Time-Out Flag 0: RX FIFO Time-Out does not occur 1: RX FIFO Time-Out occurs Writing 1 to this bit clears the flag.
[5]	RXDR	Receive FIFO Ready Flag 0: RX FIFO level is less than threshold 1: RX FIFO level is higher than threshold The RXDR bit will be set when the FIFO received data amount reaches the specified threshold level which is set by the RXTL field in the USRFCR register. This bit will be cleared when the data is read from the USRDR register and the RX FIFO level is less than threshold setting.
[4]	BII	Break Interrupt Indicator This bit will be set to 1 whenever the received data input is held in the “spacing state” (logic 0) for longer than a full word transmission time, which is the total time of “start bit” + data bits + “parity” + “stop bits” duration. Writing 1 to this bit clears the flag.
[3]	FEI	Framing Error Indicator This bit will be set to 1 whenever the received character does not have a valid “stop bit”, which means, the stop bit following the last data bit or parity bit is detected as logic 0. Writing 1 to this bit clears the flag.
[2]	PEI	Parity Error Indicator This bit will be set to 1 whenever the received character does not have a valid “parity bit”. Writing 1 to this bit clears the flag.

Bits	Field	Descriptions
[1]	OEI	Overrun Error Indicator An overrun error will occur only after the RX FIFO is full and when the next character has been completely received in the RX shift register. The character in the shift register is overwritten, when an overrun event occurs. However, the data in the RX shift register will not be transferred to the RX FIFO. The OEI bit is used to indicate the overrun event occurrence as soon as it happens. Writing 1 to this bit clears the flag.
[0]	RXDNE	RX FIFO Data Not Empty 0: RX FIFO is empty 1: RX FIFO contains at least 1 received data word

USART Timing Parameter Register – USRTPR

This register contains the USART timing parameters including the transmitter time guard parameters and the receive FIFO time-out value together with the RX FIFO time-out function enable control.

Offset: 0x014

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	TG							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	RXTOEN	RXTOC						
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:8]	TG	Transmitter Time Guard The transmitter time guard counter is driven by the baud rate clock. When the TX FIFO transmits data, the counter will be reset and then starts to count. Only when the counter content is equal to the TG value, are further word transmission transactions allowed.
[7]	RXTOEN	Receive FIFO Time-Out Counter Enable 0: Receive FIFO Time-Out Counter is disabled 1: Receive FIFO Time-Out Counter is enabled
[6:0]	RXTOC	Receive FIFO Time-Out Counter Compare Value The RX FIFO time-out counter is driven by the baud rate clock. When the RX FIFO receives new data, the counter will be reset and then starts to count. Once the time-out counter content is equal to the time-out counter compare value RXTOC, a receive FIFO time-out interrupt, RXTOI, will be generated if the RXTOIE bit in the USRIER register is set to 1. New received data or the empty RX FIFO after being read will clear the RX FIFO time-out counter.

USART IrDA Control Register – IrDACR

This register is used to control the USART IrDA mode.

Offset: 0x018

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	IrDAPSC							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
		Reserved	RXINV	TXINV	LB	TXSEL	IrDALP	IrDAEN
Type/Reset			RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:8]	IrDAPSC	IrDA Prescaler value This field contains the 8-bit debounce prescaler value. The debounce count-down counter is driven by the USART clock, named as CK_USART. The counting period is specified by the IrDAPSC field. The IrDAPSC field must be set to a value equal to or greater than 0x01 for the normal debounce counter operation. If the pulse width is less than the duration specified by the IrDAPSC field, the pulse will be considered as the glitch noise and discarded. 00000000: Reserved – can not be used 00000001: CK_USART clock divided by 1 00000010: CK_USART clock divided by 2 00000011: CK_USART clock divided by 3 ...
[5]	RXINV	RX Signal Inverse Control 0: No inversion 1: RX input signal is inversed
[4]	TXINV	TX Signal Inverse Control 0: No inversion 1: TX output signal is inversed
[3]	LB	IrDA Loop Back Mode 0: Disable IrDA loop back mode 1: Enable IrDA loop back mode for self testing
[2]	TXSEL	Transmit Select 0: Enable IrDA receiver 1: Enable IrDA transmitter
[1]	IrDALP	IrDA Low Power Mode Select the IrDA operation mode. 0: Normal mode 1: IrDA low power mode

Bits	Field	Descriptions
[0]	IrDAEN	IrDA Enable control 0: Disable IrDA mode 1: Enable IrDA mode

USART RS485 Control Register – RS485CR

This register is used to control the USART RS485 mode.

Offset: 0x01C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	ADDMATCH							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	Reserved					RSAAD	RSNMM	TXENP
Type/Reset						RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:8]	ADDMATCH	RS485 Auto Address Match value The field contains the address match value for the RS485 auto address detection operation mode.
[2]	RSAAD	RS485 Auto Address Detection Operation Mode Control 0: Disable 1: Enable
[1]	RSNMM	RS485 Normal Multi-drop Operation Mode Control 0: Disable 1: Enable
[0]	TXENP	USART RTS/TXE Pin Polarity 0: RTS/TXE is active high in the RS485 transmission mode 1: RTS/TXE is active low in the RS485 transmission mode

USART Synchronous Control Register – SYNCR

This register is used to control the USART synchronous mode.

Offset: 0x020

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved				CPO	CPS	Reserved	CLKEN
Type/Reset					RW 0	RW 0		RW 0

Bits	Field	Descriptions
[3]	CPO	Clock Polarity 0: CTS/SCK pin idle state is low 1: CTS/SCK pin idle state is high Selects the polarity of the clock output on the USART CTS/SCK pin in the synchronous mode. Works in conjunction with the CPS bit to specify the desired clock idle state.
[2]	CPS	Clock Phase 0: Data is captured on the first clock edge 1: Data is captured on the second clock edge This bit allows the user to select the phase of the clock output on the USART CTS/SCK pin in the synchronous mode. Works in conjunction with the CPO bit to determine the data capture edge.
[0]	CLKEN	Clock Enable 0: CTS/SCK pin disabled 1: CTS/SCK pin enabled Enable/disable the USART CTS/SCK pin.

USART Divider Latch Register – USRDLR

The register is used to determine the USART clock divided ratio to generate the appropriate baud rate.

Offset: 0x024

Reset value: 0x0000_0010

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	Reserved							
Type/Reset								
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	BRD							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	BRD							
Type/Reset	RW 0	RW 0	RW 0	RW 1	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	BRD	Baud Rate Divider The 16 bits define the USART clock divider ratio. Baud Rate = CK_USART / BRD Where the CK_USART clock is the clock connected to the USART module. BRD = 16 ~ 65535 for asynchronous mode BRD = 8 ~ 65535 for synchronous mode

USART Test Register – USRTSTR

This register controls the USART debug mode.

Offset: 0x028

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved						LBM	
Type/Reset							RW 0	RW 0

Bits	Field	Descriptions
[1:0]	LBM	Loopback Test Mode Select 00: Normal Operation 01: Reserved 10: Automatic Echo Mode 11: Loopback Mode

20 Universal Asynchronous Receiver Transmitter (UART)

Introduction

The Universal Asynchronous Receiver Transceiver, UART, provides a flexible full duplex data exchange using asynchronous transfer. The UART is used to translate data between parallel and serial interfaces, and is also commonly used for RS232 standard communication. The UART peripheral function supports a variety of interrupts.

The UART module includes a transmit data register TDR and transmit shift register TSR, and a receive data register RDR and receive shift register RSR. Software can detect a UART error status by reading UART Status & Interrupt Flag Register, URSIFR. The status includes the condition of the transfer operations as well as several error conditions resulting from Parity, Overrun, Framing and Break events.

The UART includes a programmable baud rate generator which is capable of dividing the UART clock of the CK_APB (CK_UART) to produce a baud rate clock for the UART transmitter and receiver.

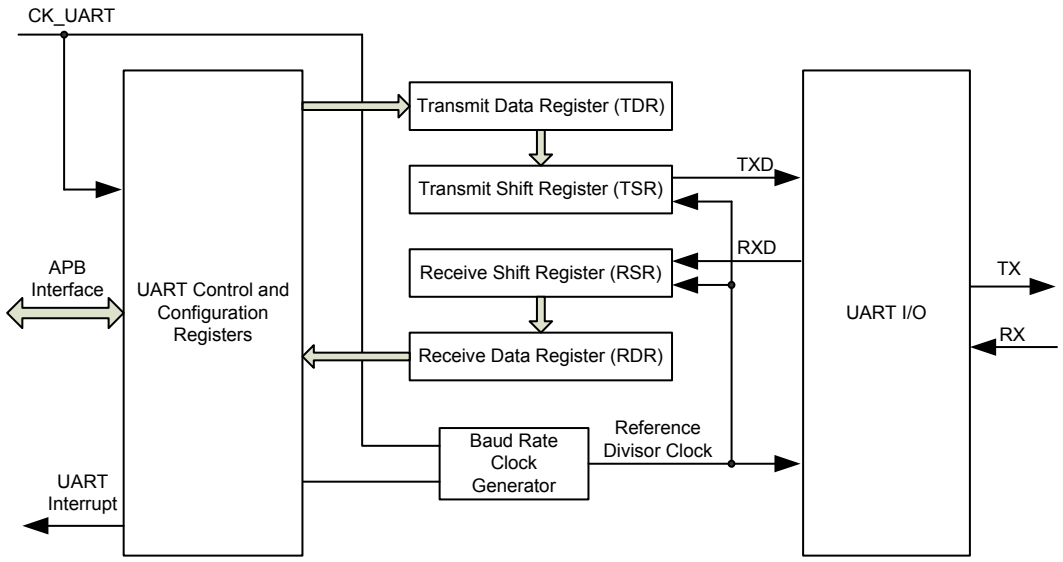


Figure 117. UART Block Diagram

Features

- Supports asynchronous serial communication modes
- Full Duplex Communication Capability
- Programming baud rate up to 3 Mbit/s
- Fully programmable serial communication functions including:
  - Word length: 7, 8, or 9-bit character
  - Parity: Even, odd, or no-parity bit generation and detection
  - Stop bit: 1 or 2 stop bit generation
  - Bit order: LSB-first or MSB-first transfer
- Error detection: Parity, overrun, and frame error

Function Descriptions

Serial Data Format

The UART module performs a parallel-to-serial conversion on data that is written to the transmit data register and then sends the data with the following format: Start bit, 7 ~ 9 LSB first data bits, optional Parity bit and finally 1 ~ 2 Stop bits. The Start bit has the opposite polarity of the data line idle state. The Stop bit is the same as the data line idle state and provides a delay before the next start situation. The both Start and Stop bits are used for data synchronization during the asynchronous data transmission.

The UART module also performs a serial-to-parallel conversion on the data that is read from the receive data register. It will first check the Parity bit and will then look for a Stop bit. If the Stop bit is not found, the UART module will consider the entire word transmission to have failed and respond with a Framing Error.

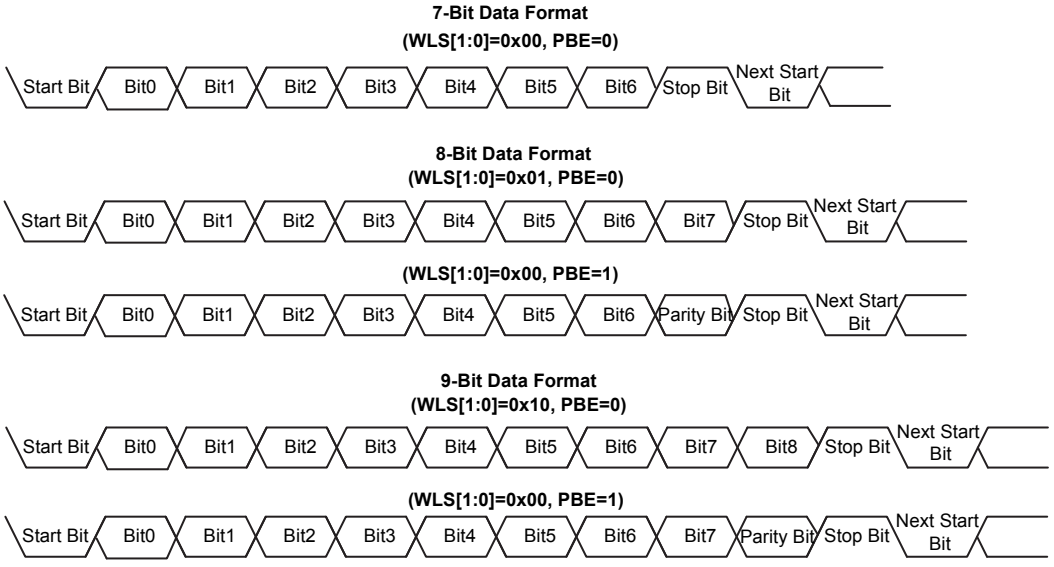


Figure 118. UART Serial Data Format

Baud Rate Generation

The baud rate for the UART receiver and transmitter are both set with the same values. The baud-rate divisor, BRD, has the following relationship with the UART clock which is known as CK_UART.

Baud Rate Clock = CK_UART / BRD

Where CK_UART clock is the APB clock connected to the UART while the BRD range is from 16 to 65535.

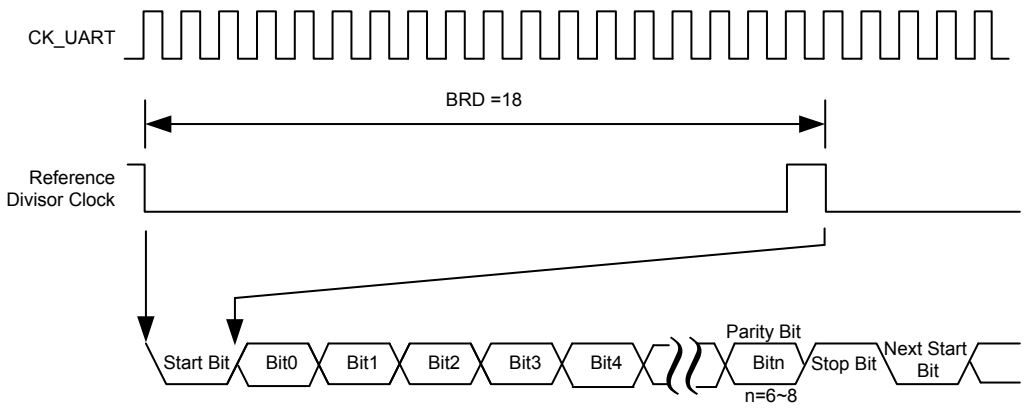


Figure 119. UART Clock CK_UART and Data Frame Timing

Table 49. Baud Rate Deviation Error Calculation – CK_UART = 8 MHz

Baud rate		CK_UART = 8 MHz		
No	Kbps	Actual	BRD	Deviation Error rate
1	2.4	2.4	3333	0.01%
2	9.6	9.6	833	0.04%
3	19.2	19.2	417	-0.08%
4	57.6	57.6	139	-0.08%
5	115.2	115.9	69	0.64%
6	230.4	228.6	35	-0.79%
7	460.8	470.6	17	2.12%
8	921.6	888.9	9	-3.55%
9	2250	N/A	N/A	N/A
10	3000	N/A	N/A	N/A

Table 50. Baud Rate Deviation Error Calculation – CK_UART = 20 MHz

Baud rate		CK_UART = 20 MHz		
No	Kbps	Actual	BRD	Deviation Error rate
1	2.4	2.4	8333	0.00%
2	9.6	9.6	2083	0.02%
3	19.2	19.2	1042	-0.03%
4	57.6	57.6	347	0.06%
5	115.2	114.9	174	-0.22%
6	230.4	229.9	87	-0.22%
7	460.8	461.5	43	0.94%
8	921.6	909.1	22	-1.36%
9	2250	2222.2	9	-1.23%
10	3000	2857.1	7	-4.76%

Table 51. Baud Rate Deviation Error Calculation – CK_UART = 24 MHz

Baud rate		CK_UART = 24 MHz		
No	Kbps	Actual	BRD	Deviation Error rate
1	2.4	2.4	10000	0.00%
2	9.6	9.6	2500	0.00%
3	19.2	19.2	1250	0.00%
4	57.6	57.6	417	-0.08%
5	115.2	115.4	208	0.16%
6	230.4	230.8	104	0.16%
7	460.8	461.5	52	0.16%
8	921.6	923.1	26	0.16%
9	2250	2181.8	11	-3.03%
10	3000	3000	8	0.00%

Table 52. Baud Rate Deviation Error Calculation – CK_UART = 40 MHz

Baud rate		CK_UART = 40 MHz		
No	Kbps	Actual	BRD	Deviation Error rate
1	2.4	2.4	16667	0.00%
2	9.6	9.6	4167	-0.01%
3	19.2	19.2	2083	0.02%
4	57.6	57.6	694	0.06%
5	115.2	115.3	347	0.06%
6	230.4	229.9	174	-0.22%
7	460.8	459.8	87	-0.22%
8	921.6	930.2	43	0.94%
9	2250	2222.2	18	-1.23%
10	3000	3076.9	13	2.56%

Interrupts and Status

The UART can generate interrupts when the following event occurs and corresponding interrupt enable bits are set:

- Receiver line status interrupts: The interrupts are generated when the UART receiver overrun error, parity error, framing error or break events occurs.
- Transmit data register empty interrupt: An interrupt is generated when the content of the transmit data register is transferred to the transmit shift register (TSR).
- Transmit complete interrupt: An interrupt is generated when the transmit data register (TDR) is empty and the content of the transmit shift register (TSR) is also completely shifted.
- Receive data ready interrupt: An interrupt is generated when the content of the receive shift register RDR has been transferred to the URDR register and is ready to read.

Register Map

The following table shows the UART registers and reset values.

Table 53. UART Register Map

Register	Offset	Description	Reset Value
URDR	0x000	UART Data Register	0x0000_0000
URCR	0x004	UART Control Register	0x0000_0000
URIER	0x00C	UART Interrupt Enable Register	0x0000_0000
URSIFR	0x010	UART Status & Interrupt Flag Register	0x0000_0180
URDLR	0x024	UART Divider Latch Register	0x0000_0010
URTSTR	0x028	UART Test Register	0x0000_0000

Register Descriptions

UART Data Register – URDR

The register is used to access the UART transmitted and received data.

Offset: 0x000
Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							DB
Type/Reset								RW 0
	7	6	5	4	3	2	1	0
	DB							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[8:0]	DB	By reading this register, the UART will return a 7, 8 and 9-bit received data. The DB field bit 8 is valid for 9-bit mode only and is fixed at 0 for the 8-bit mode. For the 7-bits mode, the DB[6:0] contains the available bits. By writing to this register, the UART will send out 7, 8 or 9-bit transmitted data. The DB field bit 8 is valid for the 9-bit mode only and will be ignored for the 8-bit mode. For the 7-bit mode, the DB[6:0] contains the available bits.

UART Control Register – URCR

The register specifies the serial parameters such as data length, parity, and stop bit for the UART.

Offset: 0x004
Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved	BCB	SPE	EPE	PBE	NSB		WLS
Type/Reset		RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
		Reserved	URRXEN	URTXEN	Reserved	TRSM		Reserved
Type/Reset			RW 0	RW 0		RW 0		

Bits	Field	Descriptions
[14]	BCB	Break Control Bit When this bit is set to 1, the serial data output on the UART TX pin will be forced to the Spacing State (logic 0). This bit acts only on the UART TX output pin and has no effect on the transmitter logic.
[13]	SPE	Stick Parity Enable 0: Disable stick parity 1: Stick Parity bit is transmitted This bit is only available when the PBE bit is set to 1. If both the PBE and SPE bits are set to 1 and the EPE bit is cleared to 0, the transmitted parity bit will be stuck to 1. However, when the PBE and SPE bits are set to 1 and also the EPE bit is set to 1, the transmitted parity bit will be stuck to 0.
[12]	EPE	Even Parity Enable 0: Odd number of logic 1's are transmitted or checked in the data word and parity bits 1: Even number of logic 1's are transmitted or checked in the data word and parity bits This bit is only available when the PBE bit is set to 1.
[11]	PBE	Parity Bit Enable 0: Parity bit is not generated (transmitted data) and checked (receive data) during transfer 1: Parity bit is generated and checked during transfer Note: When the WLS field is set to "10" to select the 9-bit data format, writing to the PBE bit has no effect.
[10]	NSB	Number of "STOP bit" 0: One "STOP bit" is generated in the transmitted data 1: Two "STOP bit" is generated when 8- and 9-bit word length is selected
[9:8]	WLS	Word Length Select 00: 7 bits 01: 8 bits 10: 9 bits 11: Reserved
[5]	URRXEN	UART RX Enable 0: Disable 1: Enable
[4]	URTXEN	UART TX Enable 0: Disable 1: Enable
[2]	TRSM	Transfer Mode Selection This bit is used to select the data transfer protocol. 0: LSB first 1: MSB first

UART Interrupt Enable Register – URIER

This register is used to enable the related UART interrupt function. The UART module generates interrupts to the controller when the corresponding events occur and the corresponding interrupt enable bits are set.

Offset: 0x00C

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								

	7	6	5	4	3	2	1	0
	Reserved	BIE	FEIE	PEIE	OEIE	TXCIE	TXDEIE	RXDRIE
Type/Reset		RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[6]	BIE	Break Interrupt Enable 0: Disable interrupt 1: Enable interrupt An interrupt is generated when the break interrupt is enabled and the BII bit is set in the URSIFR register.
[5]	FEIE	Framing Error Interrupt Enable 0: Disable interrupt 1: Enable interrupt An interrupt is generated when the framing error interrupt is enabled and the FEI bit is set in the URSIFR register.
[4]	PEIE	Parity Error Interrupt Enable 0: Disable interrupt 1: Enable interrupt An interrupt is generated when the parity error interrupt is enabled and the PEI bit is set in the URSIFR register.
[3]	OEIE	Overrun Error Interrupt Enable 0: Disable interrupt 1: Enable interrupt An interrupt is generated when the overrun error interrupt is enabled and the OEI bit is set in the URSIFR register.
[2]	TXCIE	Transmit Complete Interrupt Enable 0: Disable interrupt 1: Enable interrupt An interrupt is generated when the transmit complete interrupt is enabled and the TXC bit is set in the URSIFR register.

Bits	Field	Descriptions
[1]	TXDEIE	Transmit Data Register Empty Interrupt Enable 0: Disable interrupt 1: Enable interrupt An interrupt is generated when the transmit data register empty interrupt is enabled and the TXDE bit is set in the URSIFR register.
[0]	RXDRIE	Receive Data Ready Interrupt Enable 0: Disable interrupt 1: Enable interrupt An interrupt is generated when the receive data ready interrupt is enabled and the RXDR bit is set in the URSIFR register.

UART Status & Interrupt Flag Register – URSIFR

This register contains the corresponding UART status.

Offset: 0x010

Reset value: 0x0000_0180

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							TXC
Type/Reset								RO 1
	7	6	5	4	3	2	1	0
	TXDE	Reserved	RXDR	BII	FEI	PEI	OEI	Reserved
Type/Reset	RO 1		RO 0	WC 0	WC 0	WC 0	WC 0	

Bits	Field	Descriptions
[8]	TXC	Transmit Complete 0: Either the transmit data register (TDR) or transmit shift register (TSR) is not empty 1: Both the transmit data register (TDR) and transmit shift register (TSR) are empty An interrupt is generated if this bit is set to 1 and TXCIE=1 in the URIER register. This bit is cleared by a write to the URDR register with new data.
[7]	TXDE	Transmit Data Register Empty 0: Transmit data register is not empty 1: Transmit data register is empty The TXDE bit is set by hardware when the content of the transmit data register is transferred to the transmit shift register (TSR). An interrupt is generated if this bit is set to 1 and TXEIE=1 in the URIER register. This bit is cleared by a write to the URDR register with new data.

Bits	Field	Descriptions
[5]	RXDR	RX Data Ready 0: Receive data register is empty 1: Received data in the receive data register is ready to read This bit is set by hardware when the content of the receive shift register RDR has been transferred to the URDR register. It is cleared by a read to the URDR register. An interrupt is generated if this bit is set to 1 and RXDRIE=1 in the URIER register.
[4]	BII	Break Interrupt Indicator 0: Break event is not detected 1: Break event is detected This bit is set to 1 whenever the received data input is held in the “spacing state” (logic 0) for longer than a full character transmission time, which is the total time of “start bit” + data bits + “parity” + “stop bits” duration. An interrupt is generated if this bit is set to 1 and BIE=1 in the URIER register. Writing 1 to this bit clears the flag.
[3]	FEI	Framing Error Indicator 0: Framing error is not detected 1: Framing error is detected This bit is set 1 whenever the received character does not have a valid “stop bit” which means, the stop bit following the last data bit or parity bit is detected as logic 0. An interrupt is generated if this bit is set to 1 and FEIE=1 in the URIER register. Writing 1 to this bit clears the flag.
[2]	PEI	Parity Error Indicator 0: Parity error is not detected 1: Parity error is detected This bit is set to 1 whenever the received character does not have a valid “parity bit”. An interrupt is generated if this bit is set to 1 and PEIE=1 in the URIER register. Writing 1 to this bit clears the flag.
[1]	OEI	Overrun Error Indicator 0: Overrun error is not detected 1: Overrun error is detected An overrun error will occur only after the receive data register is full and when the next character has been completely received in the receive shift register. The character in the receive shift register will be overwritten when an overrun event occurs. However, the data in the receive shift register will not be transferred to the receive data register. The OEI bit is used to indicate the overrun event as soon as it happens. An interrupt is generated if this bit is set to 1 and OEIE=1 in the URIER register. Writing 1 to this bit clears the flag.

UART Divider Latch Register – URDLR

The register is used to determine the UART clock divided ratio to generate the appropriate baud rate.

Offset: 0x024

Reset value: 0x0000_0010

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	BRD							
Type/Reset	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0	RW 0
	7	6	5	4	3	2	1	0
	BRD							
Type/Reset	RW 0	RW 0	RW 0	RW 1	RW 0	RW 0	RW 0	RW 0

Bits	Field	Descriptions
[15:0]	BRD	Baud Rate Divider The 16 bits define the UART clock divider ratio. Baud Rate = CK_UART / BRD Where the CK_UART clock is the clock connected to the UART module. BRD = 16 ~ 65535 for UART mode

UART Test Register – URTSTR

This register controls the UART debug mode.

Offset: 0x028

Reset value: 0x0000_0000

	31	30	29	28	27	26	25	24
	Reserved							
Type/Reset								
	23	22	21	20	19	18	17	16
	Reserved							
Type/Reset								
	15	14	13	12	11	10	9	8
	Reserved							
Type/Reset								
	7	6	5	4	3	2	1	0
	Reserved						LBM	
Type/Reset							RW 0	RW 0

Bits	Field	Descriptions
[1:0]	LBM	Loopback Test Mode Select 00: Normal Operation 01: Reserved 10: Automatic Echo Mode 11: Loopback Mode