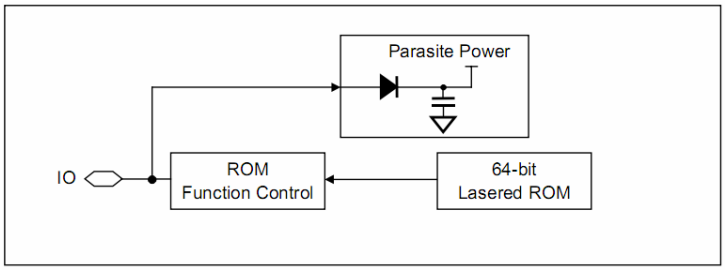
1. GENERAL DESCRIPTION

The TM1990A-F5 Serial Number iButton_ is a rugged data carrier that serves as an electronic registration number for automatic identification. Data is transferred serially through the 1-Wire (Dallas) protocol, which requires only a single data lead and a ground return. Every TM1990A-F5 is factory lasered with a guaranteed unique 64-bit registration number that allows for absolute traceability. The durable stainless-steel iButton package is highly resistant to environmental hazards such as dirt, moisture, and shock. Its compact coin-shaped profile is self-aligning with mating receptacles, allowing the TM1990A-F5 to be used easily by human operators. Accessories permit the TM1990A-F5 iButton to be mounted on almost any object, including containers, pallets, and bags.

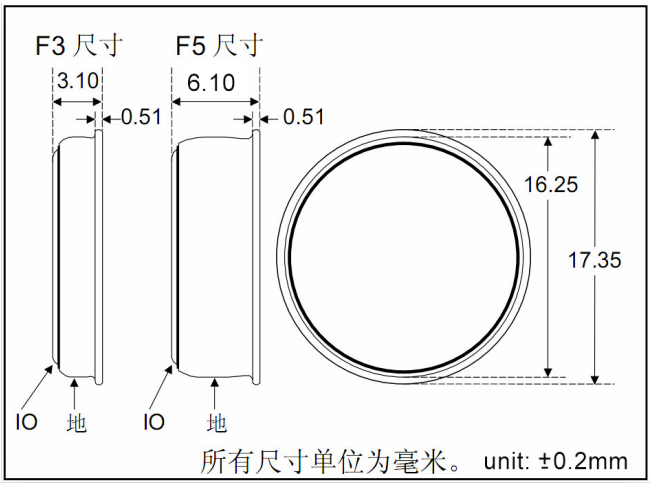
2. FUNCTION AND CHARACTERISTICS

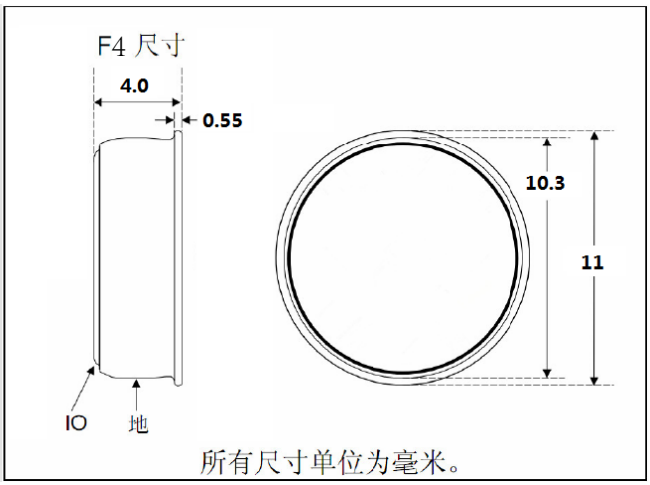
- Operating Range: 2.8V to 6.0V
- Can Be Read in Less Than 5ms
- Unique Factory-Lasered 64-Bit Registration Number Assures Error-Free Device Selection
- and Absolute Traceability Because No Two Parts are Alike
- Built-In Multidrop Controller for 1-Wire Net
- Digital Identification by Momentary Contact
- Data can be Accessed While Affixed to Object
- Economically Communicates to Bus Master with a Single Digital Signal at 16.3kbps
- Button Shape is Self-Aligning with Cup-Shaped Probes
- Durable Stainless-Steel Case Engraved with Registration Number Withstands Harsh Environments
- Easily Affixed with Self-Stick Adhesive Backing, Latched by its Flange, or Locked with a Ring Pressed Onto its Rim

3. TM1990A-F5 BLOCK DIAGRAM



4. TM1990 F3 / F4 AND F5 MicroCAN





5. THE RATINGS

5.1. ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MAXIMUM RATINGS	UNITS
IO Voltage to GND	Vio	-0.5, +6.0	V
IO Sink Current	Iio	20mA	mA
Junction Temperature	Tj	+125°C	℃
Storage Temperature Range	tstg	-55° C to +125° C	℃

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only,and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to the absolute maximum rating conditions for extended periods may affect device.

5.2. ELECTRICAL CHARACTERISTICS

(V_{PUP} = 2.8V to 6.0V, T_A = -40°C to +85°C.)			TM1990A-F5			UNITS
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	
IO Pin General Data						
1-Wire Pullup Resistance	R_{PUP}	(Notes 1, 2)	0.6		5	kΩ
Input Capacitance	C_{IO}	(Notes 3)		100	800	pF
Input Load Current	I_L	(Notes 4)		0.25		µA
Input Low Voltage	V_{IL}	(Notes 1, 5, 6)			0.8	V
Input High Voltage	V_{IH}	(Notes 6, 7)	2.2			V
Output-Low Voltage at 4mA	V_{OL}	(Notes 6)			0.4	V
Output-High Voltage	V_{OH}	(Notes 6, 8)		V_{PUP}		V
Operating Charge	Q_{OP}	(Notes 9)		30		nC
Recovery Time	t_{REC}	(Notes 1)	1			µs
Timeslot Duration	t_{SLOT}	(Notes 1)	61			µs
IO Pin, 1-Wire Reset, Presence Detect Cycle						
Reset Low Time	t_{RSTL}	(Notes 1, 10)	480			µs
Reset High Time	t_{RSTH}	(Notes 1, 11)	480			µs
Presence Detect High Time	t_{PDH}		15		60	µs
Presence Detect Low Time	t_{PDL}	(Notes 14)	60		240	µs
Presence Detect Sample Time	t_{MSP}	(Notes 1)	60		75	µs
IO Pin, 1-Wire Write						
Write-0 Low Time	t_{W0L}	(Notes 1)	60		120	µs
Write-1 Low Time	t_{W1L}	(Notes 1, 12)	1		15-ε	µs
IO Pin, 1-Wire Read						
Read Low Time	t_{RL}	(Notes 1, 13)	1		15 - δ	µs
Read SampleTime	t_{MSR}	(Notes 1, 13)	t_{RL} + δ		15	µs

Note 1: System requirement.

Note 2: Full Rpup range guaranteed by design and simulation, not production tested. Production testing performed at a fixed Rpup value. Maximum allowable pullup resistance is a function of the

number of 1-Wire devices in the system and 1-Wire recovery times. The specified value here applies to systems with only one device and with the minimum 1-Wire recovery times.

Note 3: Capacitance on the IO pin could be 800pF when power is first applied. If a 5kΩ resistor is used to pull up the IO line to Vpup, 5μs after power has been applied the parasite capacitance will not affect normal communications.

Note 4: Input load is to ground.

Note 5: The voltage on IO needs to be less or equal to V_{ilmax} whenever the master drives the line low. Under certain low voltage conditions, V_{ilmax} may have to be reduced to as much as 0.5V to always guarantee a Presence Pulse.

Note 6: All voltages are referenced to ground.

Note 7: V_{IH} is a function of the internal supply voltage.

Note 8: V_{PUP} = external pullup voltage.

Note 9: 30nC per 72 time slots at 5.0V pullup voltage with a 5kΩ pullup resistor and $t_{slot} \leq 120\mu s$.

Note 10: The reset low time (t_{RSTL}) should be restricted to a maximum of 960 μs, to allow interrupt signaling.

Note 11: An additional reset or communication sequence cannot begin until the reset high time has expired.

Note 12: ε represents the time required for the pullup circuitry to pull the voltage on IO up from V_{IL} to V_{IH}.

Note 13: δ represents the time required for the pullup circuitry to pull the voltage on IO up from V_{IL} to the input-high threshold of the bus master.

Note 14: Presence pulse is guaranteed only after a preceding Reset Pulse (t_{RSTL}).

6. DESCRIPTION

6.1. 64-BIT LASERED ROM

Each TM1990A-F5 contains a unique ROM code that is 64 bits long. The first 8 bits are a 1-Wire family code. The next 48 bits are a unique serial number. The last 8 bits are a CRC of the first 56 bits. See 6.2 for details. The 1- Wire CRC is generated using a polynomial generator consisting of a Shift and XOR gates as shown in 6.3. The polynomial is $X^8 + X^5 + X^4 + 1$

The Shift register bits are initialized to 0. Then starting with the least significant bit of the family code, one bit at a time is shifted in. After the 8th bit of the family code has been entered, then the serial number is entered. After the 48th bit of the serial number has been entered, the Shift register contains the CRC value. Shifting in the 8 bits of CRC returns the Shift register to all 0s.

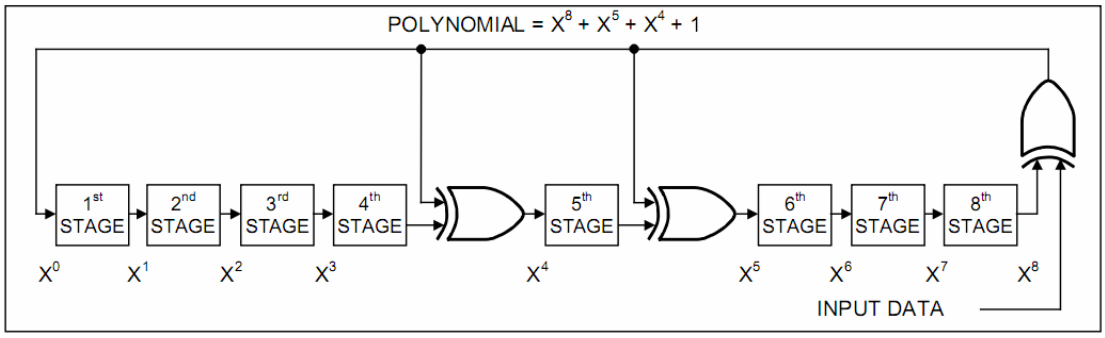
6.2. 64-BIT LASERED ROM

MSB LSB

8 BIT CRC CODE	8BIT FIX CODE（00）	8BIT FIX CODE（00）	8BIT FIX CODE（01）	24-BIT SERIAL NUMBER	8BIT FAMILY CODE（01）

MSB LSB MSB LSB MSB LSB

6.3. 1-WIRE CRC GENERATOR

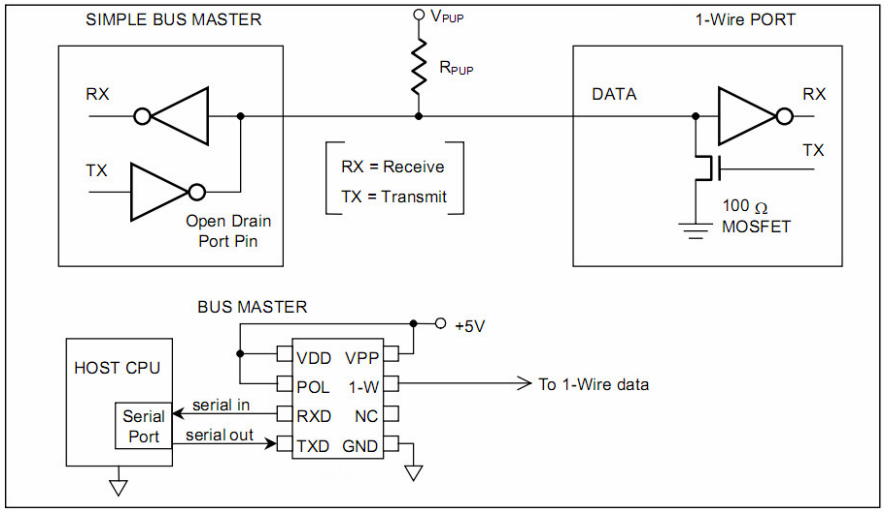


6.4. 1-Wire BUS SYSTEM

The 1-Wire bus is a system, which has a single bus master and one or more slaves. In all instances the TM1990A-F5 is a slave device. The bus master is typically a microcontroller or PC. For small configurations the 1-Wire communication signals can be generated under software control using a single port pin.This simplifies the hardware design and frees the microprocessor from responding in real-time. The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1-Wire signaling (signal types and timing). The 1-Wire protocol defines bus transactions in terms of the bus state during specific time slots that are initiated on the falling edge of sync pulses from the bus master.

6.5. HARDWARE CONFIGURATION

The 1-Wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1-Wire bus must have open drain or tri-state outputs. The 1-Wire port of the TM1990A-F5 is open-drain with an internal circuit equivalent to that shown in 6.5. A multi-drop bus consists of a 1-Wire bus with multiple slaves attached. At standard speed the 1-Wire bus has a maximum data rate of 16.3kbps. The value of the pullup resistor primarily depends on the network size and load conditions. For most applications the optimal value of the pullup resistor is approximately 2.2kΩ. The idle state for the 1-Wire bus is high. If for any reason a transaction needs to be suspended, the bus MUST be left in the idle state if the transaction is to resume. If this does not occur and the bus is left low for more than 120µs, one or more devices on the bus may be reset.



7. TRANSACTION SEQUENCE

The protocol for accessing the TM1990A-F5 through the 1-Wire port is as follows:

- Initialization
- ROM Function Command

7.1. INITIALIZATION

All transactions on the 1-Wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by presence pulse(s) transmitted by the slave(s). The presence pulse lets the bus master know that the TM1990A-F5 is on the bus and is ready to operate. For more details, see the *1-Wire Signaling* section.

7.2. 1-Wire ROM FUNCTION COMMANDS

Once the bus master has detected a presence, it can issue one of ROM function commands that the TM1990A-F5 supports. All ROM function commands are 8 bits long. A list of these commands follows (see flowchart in 7.5).

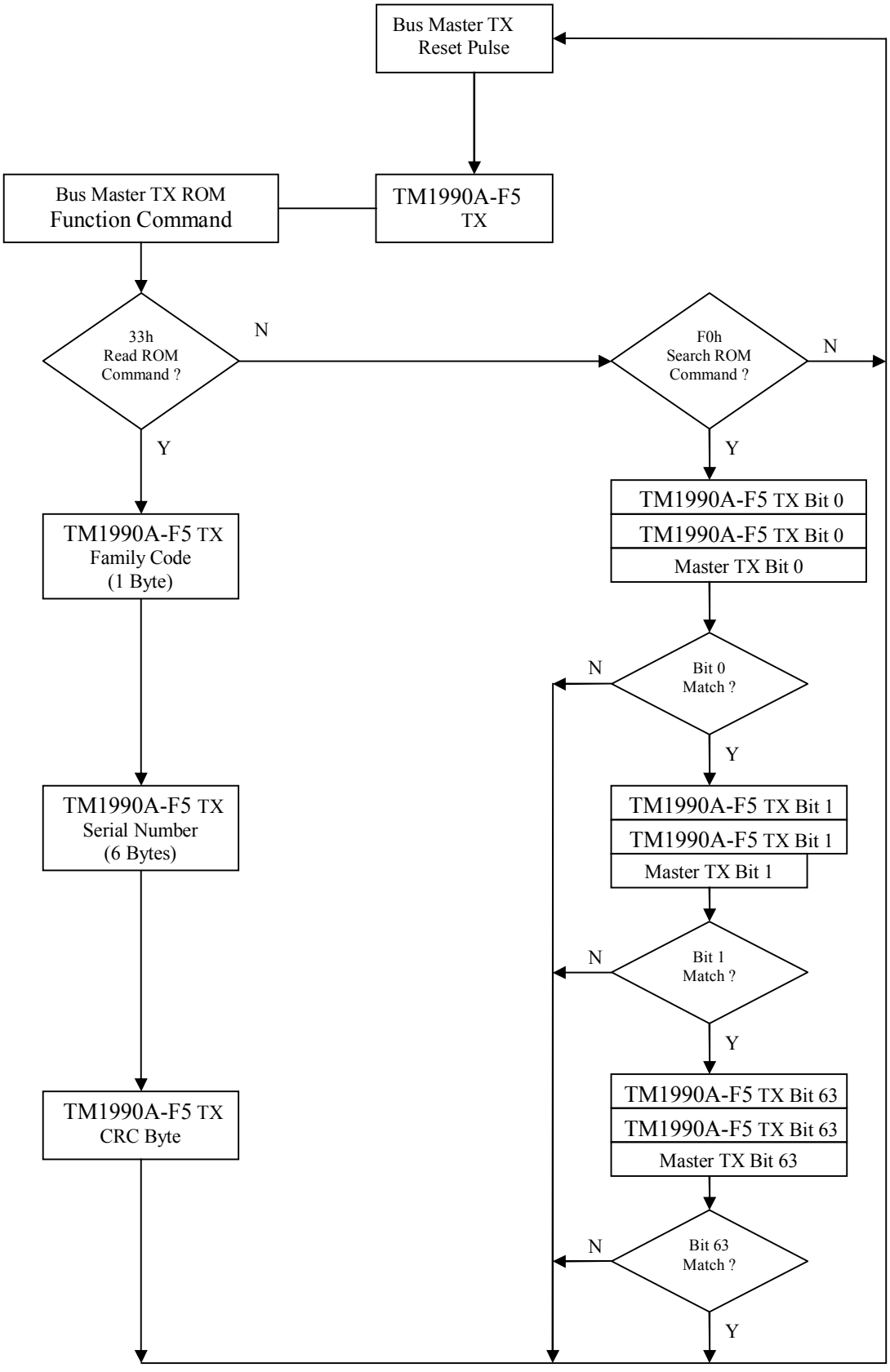
7.3. Read ROM [33h]

This command allows the bus master to read the TM1990A-F5's 8-bit family code, unique 48-bit serial number, and 8- bit CRC. This command can only be used if there is a single slave device on the bus. If more than one slave is present on the bus, a data collision will occur when all slaves try to transmit at the same time (open drain will produce a wired-AND result). The resultant family code and 48-bit serial number will result in a mismatch of the CRC.

7.4. Search ROM [F0h]

When a system is initially brought up, the bus master might not know the number of devices on the 1-Wire bus or their registration numbers. By taking advantage of the wired-AND property of the bus, the master can use a process of elimination to identify the registration numbers of all slave devices. For each bit of the registration number, starting with the least significant bit, the bus master issues a triplet of time slots. On the first slot, each slave device participating in the search outputs the true value of its registration number bit. On the second slot, each slave device participating in the search outputs the complemented value of its registration number bit. On the third slot, the master writes the true value of the bit to be selected. All slave devices that do not match the bit written by the master stop participating in the search. If both of the read bits are zero, the master knows that slave devices exist with both states of the bit. By choosing which state to write, the bus master branches in the ROM code tree. After one complete pass, the bus master knows the registration number of a single device. Additional passes identify the registration numbers of the remaining devices.

7.5. ROM FUNCTIONS FLOW CHART



7.6. Match ROM [55h] /Skip RO[CCh]

The minimum set of 1-Wire ROM function commands includes a Match ROM and a Skip ROM command. Since the TM1990A-F5 contains only the 64-bit ROM without any additional data fields, Match ROM and Skip ROM are not applicable. The TM1990A-F5 will remain silent (inactive) upon receiving a ROM function command that it doesn't support. This allows the TM1990A-F5 to coexist on a multidrop bus with other 1-Wire devices that do respond to Match ROM or Skip ROM.

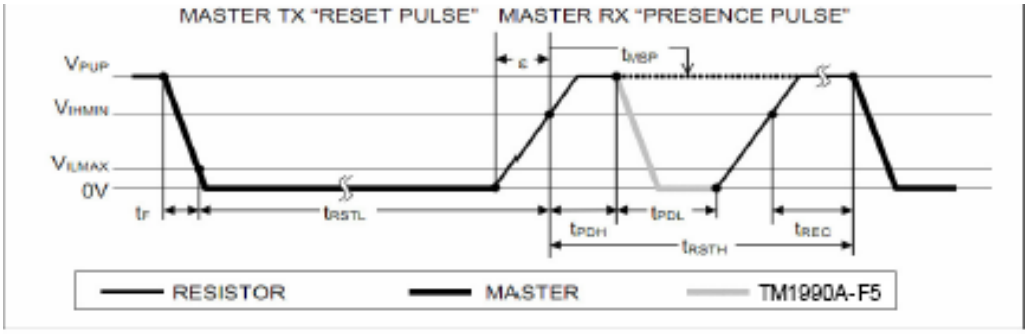
7.7. 1-Wire SIGNALING

The TM1990A-F5 requires strict protocols to ensure data integrity. The protocol consists of four types of signaling on one line: Reset Sequence with Reset Pulse and Presence Pulse, Write-Zero, Write-One, and Read-Data. Except for the presence pulse the bus master initiates all these signals.

To get from idle to active, the voltage on the 1-Wire line needs to fall from V_{PUP} to below V_{ILMAX}. To get from active to idle, the voltage needs to rise from V_{ILMAX} to above V_{IHMIN}. The time it takes for the voltage to make this rise, referenced as ε in Figure 7.8, depends on the value of the pullup resistor (R_{PUP}) and capacitance of the 1-Wire network attached.

The initialization sequence required to begin any communication with the TM1990A-F5 is shown in Figure 7.8. A Reset Pulse followed by a Presence Pulse indicates the TM1990A-F5 is ready to receive a ROM function command. If the bus master uses slew-rate control on the falling edge, it must pull down the line for $t_{RSTL} + t_F$ to compensate for the edge.

7.8. INITIALIZATION PROCEDURE “RESET AND PRESENCE PULSES”



After the bus master has released the line it goes into receive mode (RX). Now the 1-Wire bus is pulled to Vpup via the pullup resistor or, in case of driver by active circuitry. When the V_{IHMIN} is crossed, the TM1990A-F5 waits for t_{PDH} and then transmits a Presence Pulse by pulling the line low for t_{PDL}. To detect a presence pulse, the master must test the logical state of the 1-Wire line at t_{MSP}

.

7.9. READ/WRITE TIME SLOTS

Data communication with the TM1990A-F5- takes place in time slots, which carry a single bit each. Write-time slots transport data from bus master to slave. Read-time slots transfer data from slave to master. The definitions of the write and read-time slots are illustrated in Figure 7.12. All communication begins with the master pulling the data line low. As the voltage on the 1-Wire line falls below V_{ILMAX}, the TM1990A-F5 starts its internal timing generator that determines when the data line will be sampled during a write-time slot and how long data will be valid during a read-time slot.

7.10. MASTER-TO-SLAVE

For a **write-one** time slot, the voltage on the data line must have risen above V_{IHMIN} after the write-one low time t_{W1LMAX} is expired. For a **write-zero** time slot, the voltage on the data line must stay below V_{ILMAX} until the write-zero low time t_{W0LMIN} is expired. For most reliable communication the voltage on the data line should not exceed V_{ILMAX} during the entire t_{W0L} window. After the voltage has risen above V_{IHMIN}, the TM1990A-F5 needs a recovery time t_{REC} before it is ready for the next time slot.

7.11. SLAVE-TO-MASTER

A **read-data** time slot begins like a write-one time slot. The voltage on the data line must remain below V_{ILMAX} until the read low time t_{RL} is expired. During the t_{RL} window, when responding with a 0, the TM1990A-F5 will start pulling the data line low; its internal timing generator determines when this pulldown ends and the voltage starts rising again. When responding with a 1, the TM1990A-F5 will not hold the data line low at all, and the voltage starts rising as soon as t_{RL} is over.

The sum of t_{RL} +δ(rise rime) on one side and the internal timing generator of the TM1990A-F5 on the other side define the master sampling window (t_{MSRMIN} to t_{MSRMAX}) in which the master must perform a read from the data line. For most reliable communication, t_{RL} should be as short as permissible and the master should read close to but no later than t_{MSRMAX}. After reading from the data line, the master must wait until t_{SLOT} is expired. This guarantees sufficient recovery time t_{REC} for the TM1990A-F5 to get ready for the next time slot.

7.12. READ/WRITE TIMING DIAGRAM